FIC Status

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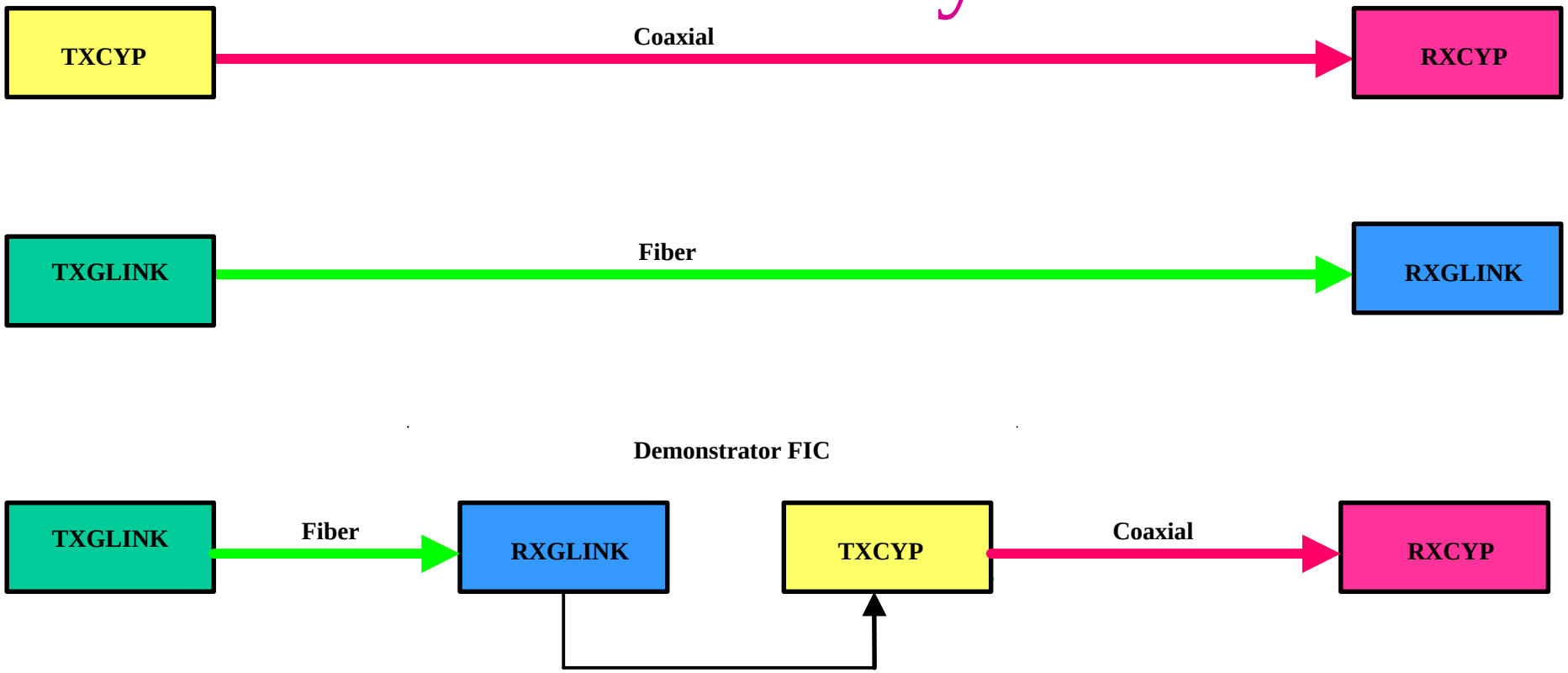
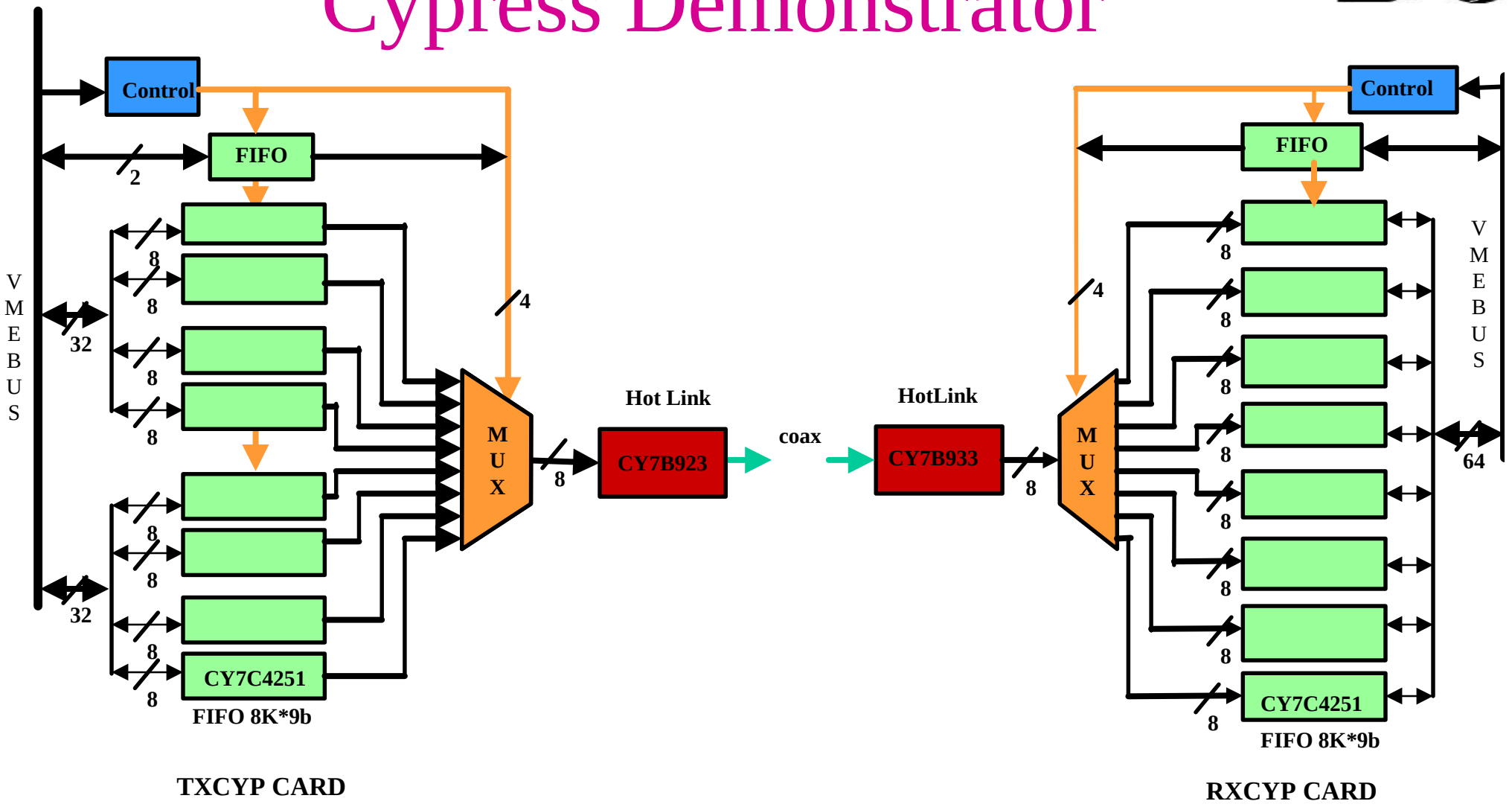
Summary

- Demonstrator Status
- Link questions
- Protocol questions
- Monitoring questions
- Schedule, Funding

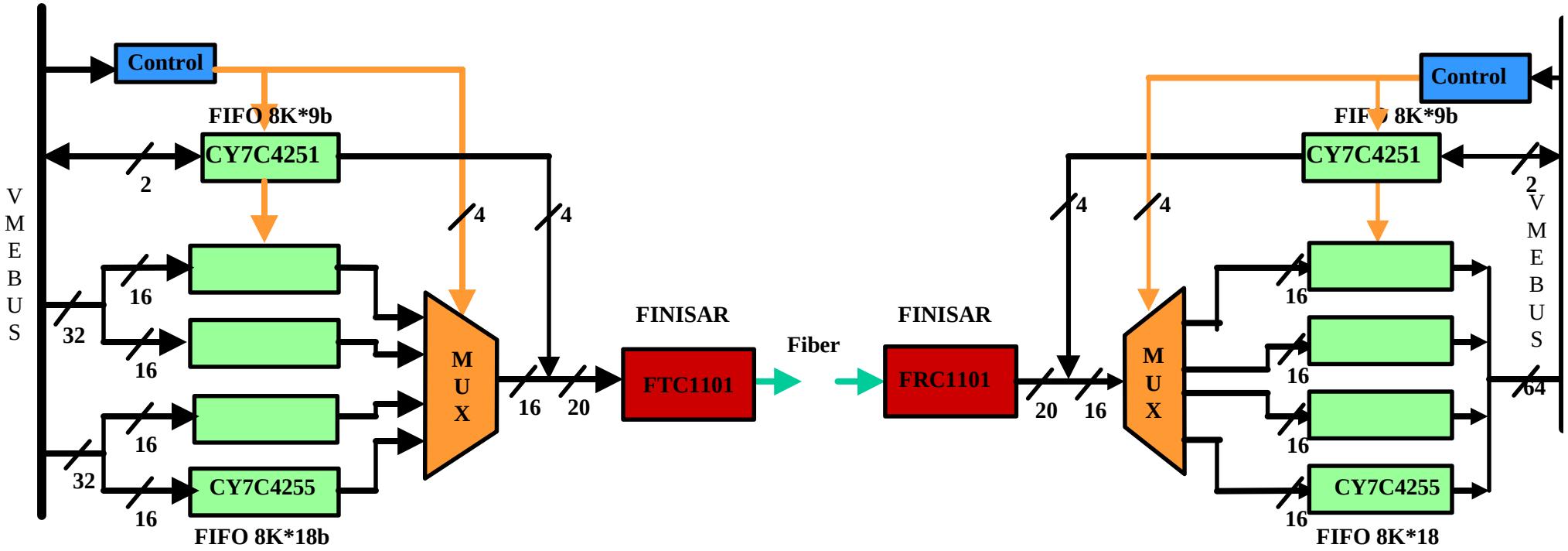
Block Diagram of FIC Demonstrator System



Cypress Demonstrator



G-Link Demonstrator



TXGLINK CARD

RXGLINK CARD

Status of Demonstrator

- The 4 VME cards are operational.
- Some tuning has still to be done : Several bugs have been identified.
- A first version of Test software exists.
- The FIC emulation is almost ready for tests.

Link Questions (1)
Choice of HP board

- FINISAR Module Vs VTM Board
  - Both options fulfil the requirements.
  - We have no preference, but we can not start the FIC design until this choice is done.
- In both options, these boards plug into the FIC.
  - There is no point in bringing these boards to Europe.
  - These boards should be assembled to the FIC during installation at D0.

Link Questions (2) Synchronisation

- General considerations
  - The link synchronisation is based on co-ordinated actions at both the transmitter and the receiver.
  - For the G-Link and the Hot Link, it is possible to define the transmitter idle state in a way allowing the link synchronisation by actions at the receiver while the transmitter is idle.
  - What is the method used in D0?

Synchronisation (2)

- The case of Hot Link
  - The Hot Link receiver can only be synchronised if the local clock is close enough (<<10Hz) to the transmitted clock.
  - The only way to achieve that is to order matched crystals.
  - We expect that FNAL will provide us with the Hot Link oscillators.
  - We need the technical description of these oscillators.

Link Questions (3)
FIFO Size

- The FIFO must be able to fit 16 events.
- Is the (max) event size dependent on link type, number?
- The FIFO is built out of standard CY7C42x5 chips (4,8,16,32,64 or 128 Ko per chip).
- These chips are externally compatible: it is easy to adapt the FIFO size by exchanging chips.
- We foresee to use only one FIFO chip per link (i.e. 4 FIFO chips per FIC board).

Link Questions (4)
Hot Link Adaptation

- The connection of an Hot Link chip to a shielded twisted pair is a delicate enterprise.
  - We are not ready to do it by lack of time.
  - We are waiting a proven design from D0.
  - We expect FNAL to provide the chosen transformers.
  - WE will not test the adaptation on our demonstrator before spring 99, we need it only for the debugging of the FIC.

Protocol questions
Event size

- The event is an integral number of 16 bits words (it is received by a G-Link).
- Is-it an even number of words?
- Is padding requested?
- What is the minimum separation between events?
  - We need about 3 clock periods.

Protocol questions
Event delimiters

- Is it allowed to interspersed idle symbols in the middle of an event?
  - **Pro** simplify the logic in the transmitter.
  - **Con** It is another error detector.
- Who needs a start of event symbol?
  - The first data symbol is a good start of event indicator.
- End of event symbol
  - It is mandatory if iddle symbols are allowed inside an event.
  - We can not translate the associated data between G-Link and Hot Link for speed reasons.

Protocol questions(2)
Error Handling

- What kind of errors should be recognised by the FIC?
  - Erroneous character received on the link.
  - FIFO overflow.
  - Idle symbols in the middle of an event.
- Is it necessary to perform a reset (and a resynchronisation) in case of any error?
- How the FIC should signal errors?
  - ECL output
  - VME interrupt

Protocol questions(3)
Test features

- The Hot Link has a nice Built In Self Test (BIST).
  - Some control characters are already foreseen to control this feature in the CFT links.
  - Shall we implement the same functionality?
- The FIFOs in the FIC are accessible through VME.
  - Shall we implement exclusion locks between VME and the serial links for FIFO access.
- Possible use of the retransmit function of the FIFOs?

Monitoring questions

- What to monitor?
  - The number of events in the FIFO.
  - The occupied size (in bytes) in the FIFO.
  - The number of errors.
- How many monitoring counters?
  - Monitoring is done in hardware, not in software. Resources are expensive: One must reduce the number of counters to the bare minimum.

Monitoring questions (2)

- Monitoring information format
  - Number of classes for event number (16 or 17)
  - Maximum count of event during a monitoring period.
  - …
- How to transmit monitoring information
  - In real-time with an ECL link.
  - Accumulate statistics between two VME interrogations.
- Important remark: we are doing the monitoring in hardware, we can not implement too complex logic.

Schedule

- It is clear that we are waiting for the answers to all the previous questions.
- This will generate a slip in schedule equal to the delay between today and the day when all these questions are settled.

Money

- The MoU foresees a Saclay contribution of 100 K$
- The cost of a FIC card is estimated to be 10 k$
  - 4 HP receivers 5 K$
  - 4 FIFOs of 128 Ko 1 K$
  - Other (Printed board,connectors…) 4 K$
- If more than 10 cards are needed (including spares and prototypes), FNAL must provide part of the hardware (e.g. the HP receivers).

Original Schedule
(April 17, 1998)

- Demonstrator → May - October 1998
- Prototypes and Test set-up → Nov. 98 - May 99
- Production → June - December 99

Revised Schedule

- Demonstrator → May - Nov. 1998
- Test set-up → Aug. 98 - May 99
- Prototype → Nov. 98 - May 99
- Production → June - Dec. 99

- Almost Done
- Under Way
- Waiting specs.