SFO Options
with decisions in RED
and new comments in
BLUE

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Criteria for Decisions

- **Meet Performance Criteria**
  bandwidth, deadtime, acceptance, rejection
    - with adequate margin (for occupancy e.g.)

- **Acceptable Schedule Risk**

  (Includes complexity)
  specification

  resources

  prototype and construction

  commissioning

- **Maintenance and Repair**
  resources, complexity, card variants...

- **Parts and Engineering Costs**
  within constraints

- **Expansion Capability**
  beyond planned scope

MBT

- 16-deep FIFOs all channels
- either G-link or Cypress
- 128b Mbus broadcast
- SCL Mezzanine
    - Send L1 to FIFO
    - Queue L2
    - SCL Initialize
- 2 Cypress Outputs
- Digital I/O (e.g. to Framework)
- VME slave (&Mbus programmed I/O)
    - download
    - control
    - monitor

SLIC

- 16 FIFO's
- either G-link or Cypress inputs
- FPGA routing
- 4 TI C6x Integer DSP's per card
- Master DSP for readout
- 2 Cypress outputs

    hope can send even L3 Unbias data via Cypress outputs

- SCL Mezzanine

    receive SCL Initialize

    send L1 SCL (e.g. Qualifiers) to FIFO

    L2 Accept/Reject?

    - Irrelevant if readout only via Worker Alpha

SCL Fanout to SLIC

- ## SCL Initialize
  force clearance of buffers,
    even if partial events
  Admin could send by VME int or write
  Admin could/should read back "all clear"

- ## L1 Qualifiers
  how to process this event
  probably needs to get in FIFO

- ## L1 Accept number
  enough to be sure event synched

- ## L2 accept/reject info?
  probably NOT needed if
    - Administrator in full control of L3 readout
    - L3 readout only from alphas, not SLIC

Classic SFO

- Special Card
    - made of blocks from MBT design
    - Fan out via Cypress
    - SCL Initialize via VME
- DECIDE: MBT output (Daisy chain OR SFO Lite) are better alternatives

+ uses simple interface (Cypress)

+ naturally FIFO'd for processing of event

- extra card to build just for SLIC crates

- cables running across cards

-? if needed to steer processing
    - treat differently from other inputs
    - read first Decide purely an advantage

SFO Lite

● **Special Card**

> Receive L1 SCL info via Cypress from MBT
>
> Fan out via Cypress
>
> SCL Initialize via VME

+ uses simple interface (Cypress)

+ naturally FIFO'd for processing of event

+ simpler than Classic SFO

> (JUST Cypress)
>
> less engineering, less delay

Decision: a Candidate, with Daisy Chain

- extra card to build just for SLIC crates

- cables running across cards

- extra output on MBT (real estate)

> can be on front

- if fiber, extra input type for SLIC

SFO Lite with Fiber

● **Special Card**

　　Receive L1 SCL info via Cypress from MBT

　　　• MBT driver is laser, not LED

　　Fan out passively or by amplifier

　　SCL Initialize via VME

+ uses simple interface (Cypress)

+ naturally FIFO'd for processing of event

+ simpler than SFO Lite

　　　　(JUST fiber, maybe passive)

　　　less engineering, less delay

DECISION: not ruled out, await Cu/Fiber
　　decision

- extra card to build just for SLIC crates

- cables running across cards

- extra output on MBT (real estate)

SFO by backplane bus

- 16b qualifiers
- 1b SCL initialize (?)
- 4b L1 Accept

DECIDE: NO, others more attractive

+ eliminate SFO card

+? Naturally different from other inputs

- more (complex) function on SLIC

- more function on MBT

- MBT MUST be in same crate

J2:

    - new source of noise

    - custom wiring

OR

    - extra front-panel cable bus

- time to negotiate bus protocol

SFO by Cypress daisy chain on SLIC transition card

- Extra output on MBT
- Special input on SLIC for L1 info
- Extra output on SLIC
- SCL Initialize via VME (Administrator)
- Decision: real option, esp if Cu Cypress

+ eliminate SFO card

+ no protocol negotiation

- more function on MBT

- more function on SLIC (simple:

    can be all on transition card)

- connector real estate on both cards

- more cables running across cards

-? time delay for arrival of inputs

SCL Receiver on SLIC

+ eliminate SFO card

- $500 per SLIC for Mezzanine

  20K$ total

- more for extra modules at hub end

- bend SCL protocol even further

- more function on SLIC

  real estate

Decision: NO