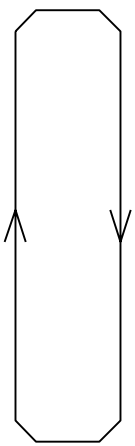
Transport and Event over the MBus

Send the next event over the MBus to the Processor Card's fancy Receiver Section input FIFO and from there, based of the mapper register contents, into the proper slot in the main memory event buffer.



A -> R "Send the Next Event"

R -> A&W "All of this event has been put on MBus""

W -> A "I have seen the end of event flag and I have completed moving the event from FIFO to main memory"

Admin decides, "Is everything all set to move the next event ?"
I.E. I know what MBus high order event address the Receiver Card will used next; the the mappers in the processor card fancy Receiver sections have this MBus address pointing at an "empty" main memory event buffer slot ?