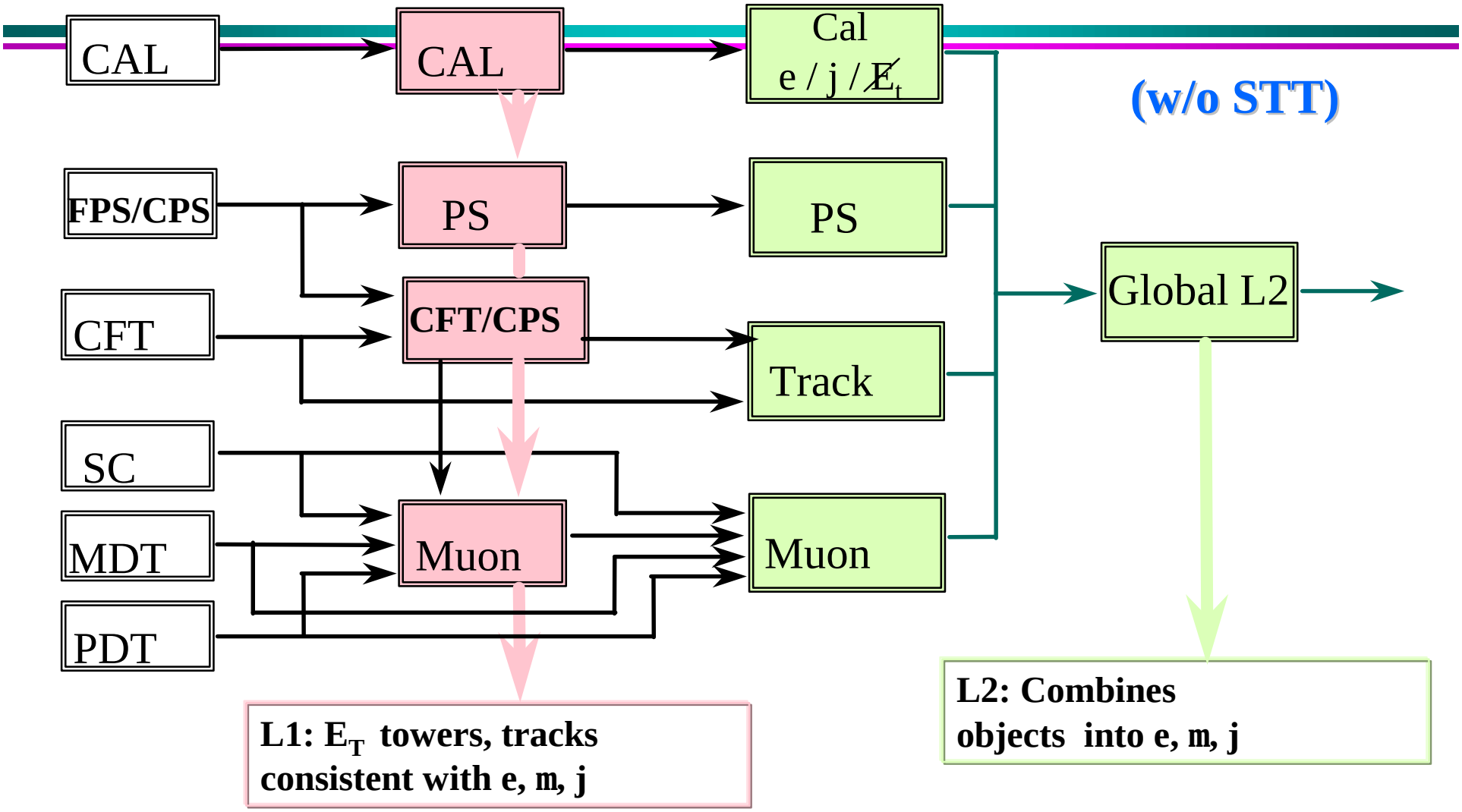
Level 2 Test Stand

James T. Linnemann
Michigan State University
FNAL L2 Meeting
Apr 14, 1999

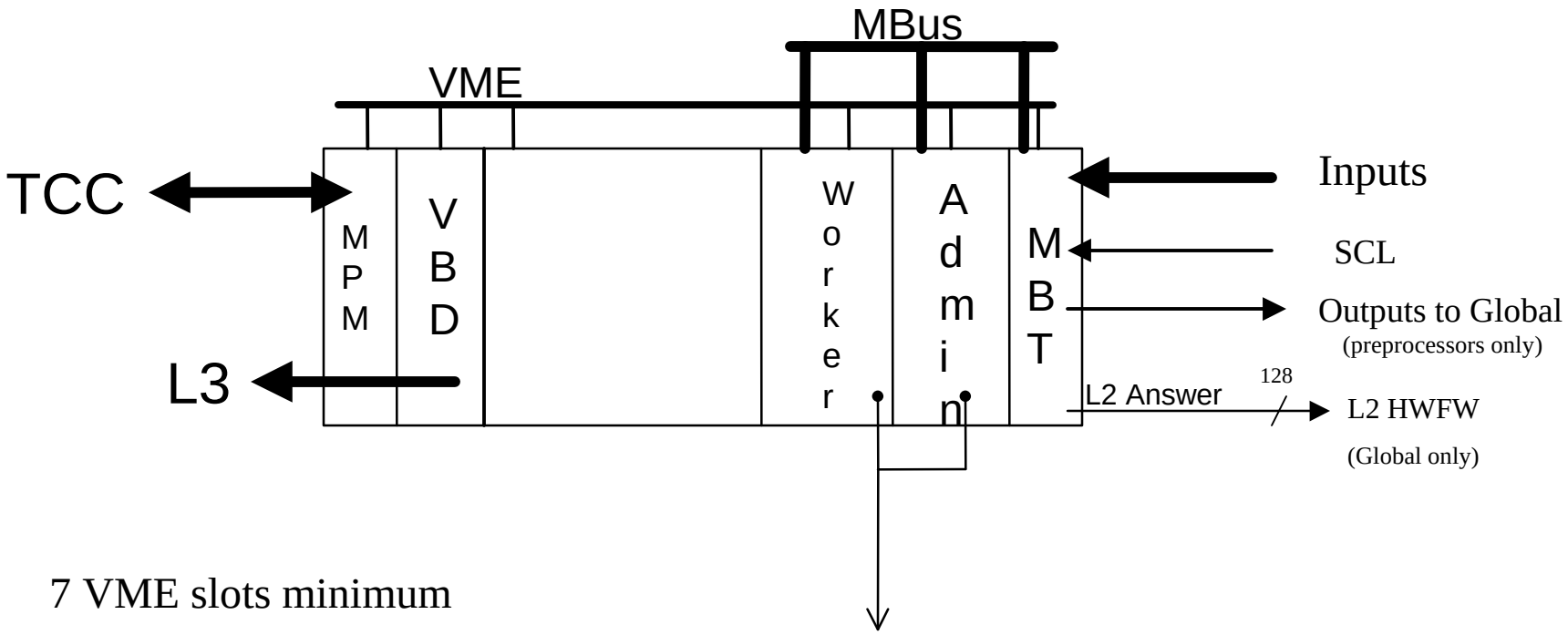
Agenda

SLIC	20	Fortner
MBT	15	Baden
Alpha	15	Martin
Test	20	Linnemann
Monitoring	15	Adams/Yasuda
Milestones	15	Moore
slack	20	

L2 Trigger


CAL
CAL
Cal
e / j / $\not{E}_t$
(w/o STT)
FPS/CPS
PS
PS
CFT
CFT/CPS
Track
Global L2
SC
MDT
Muon
Muon
PDT
L1: E_T towers, tracks consistent with e, m, j
L2: Combines objects into e, m, j

Standard Crate



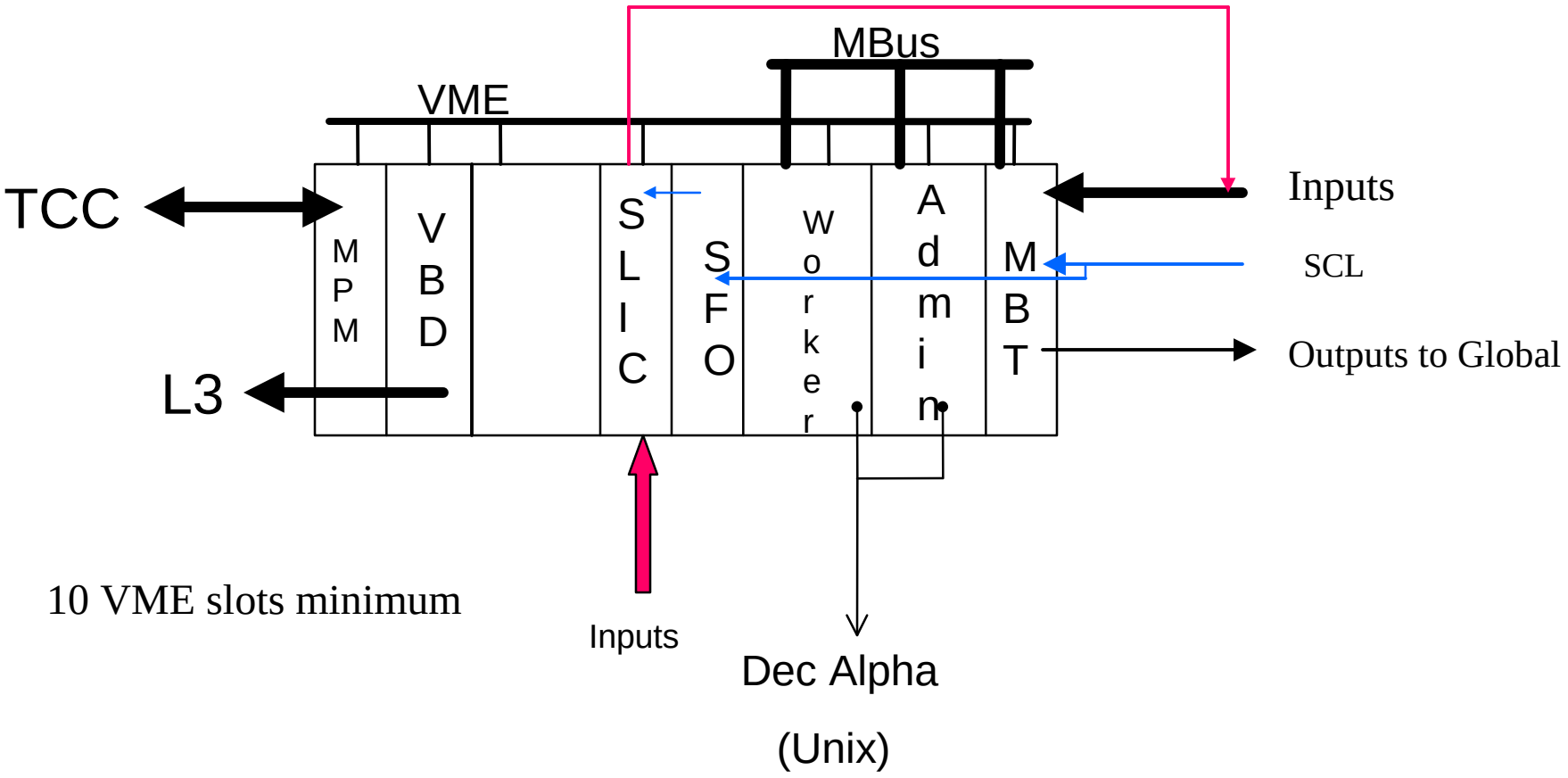
7 VME slots minimum

up to 5 workers per crate

short (non-CDF) MBus

JTL, MSU 12/18/97

Standard Crate with SLIC



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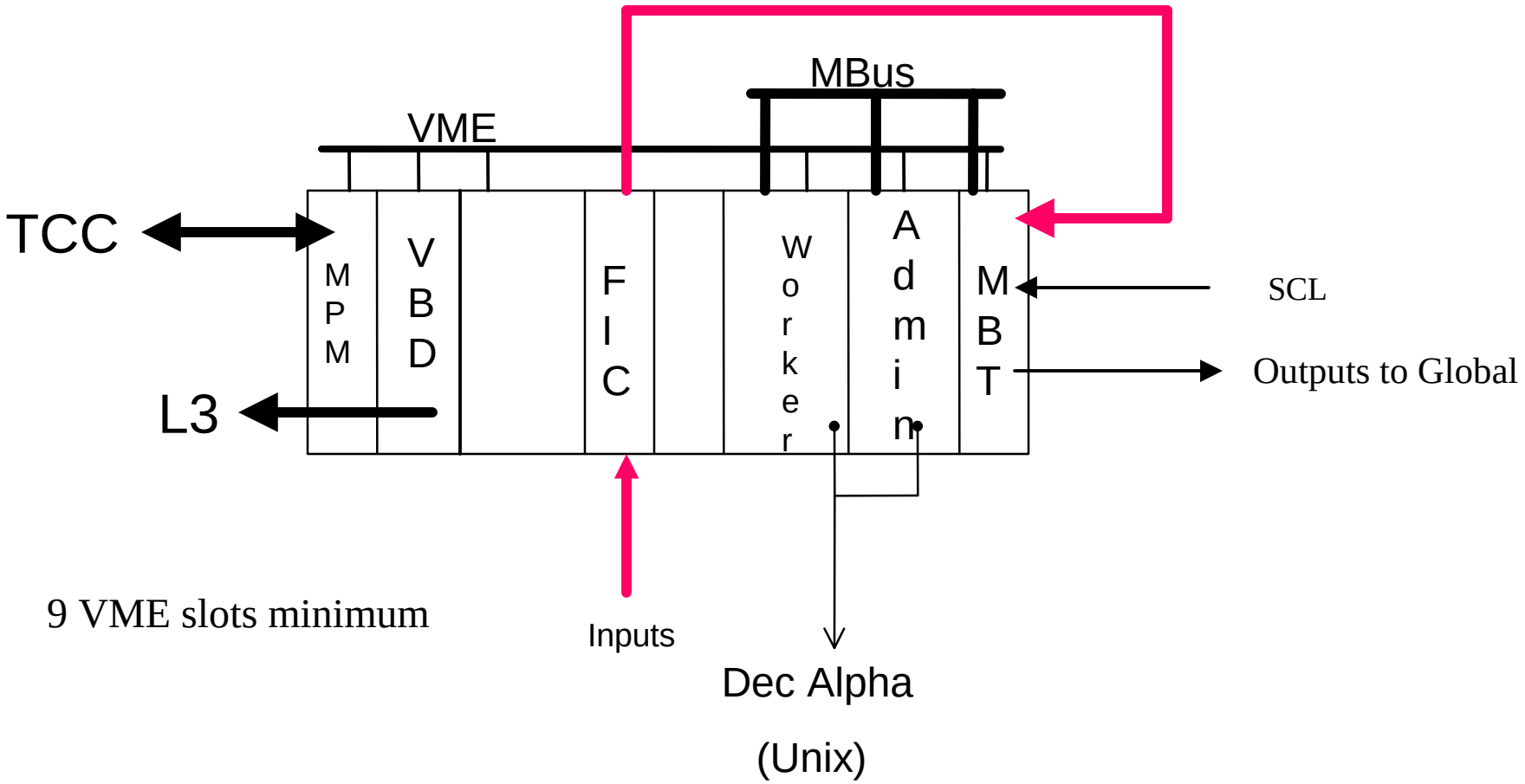
Standard Crate with FIC to MBT



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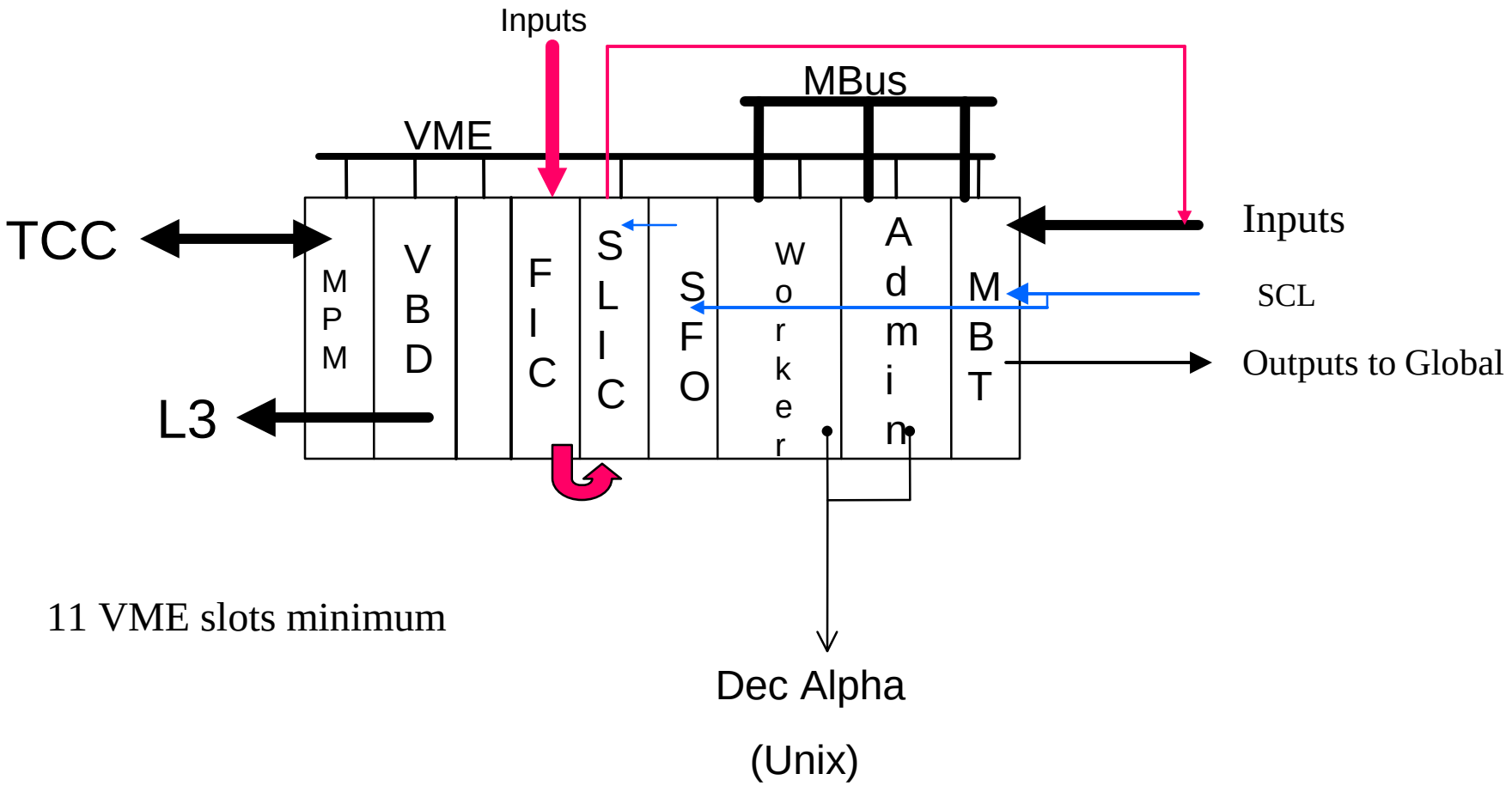
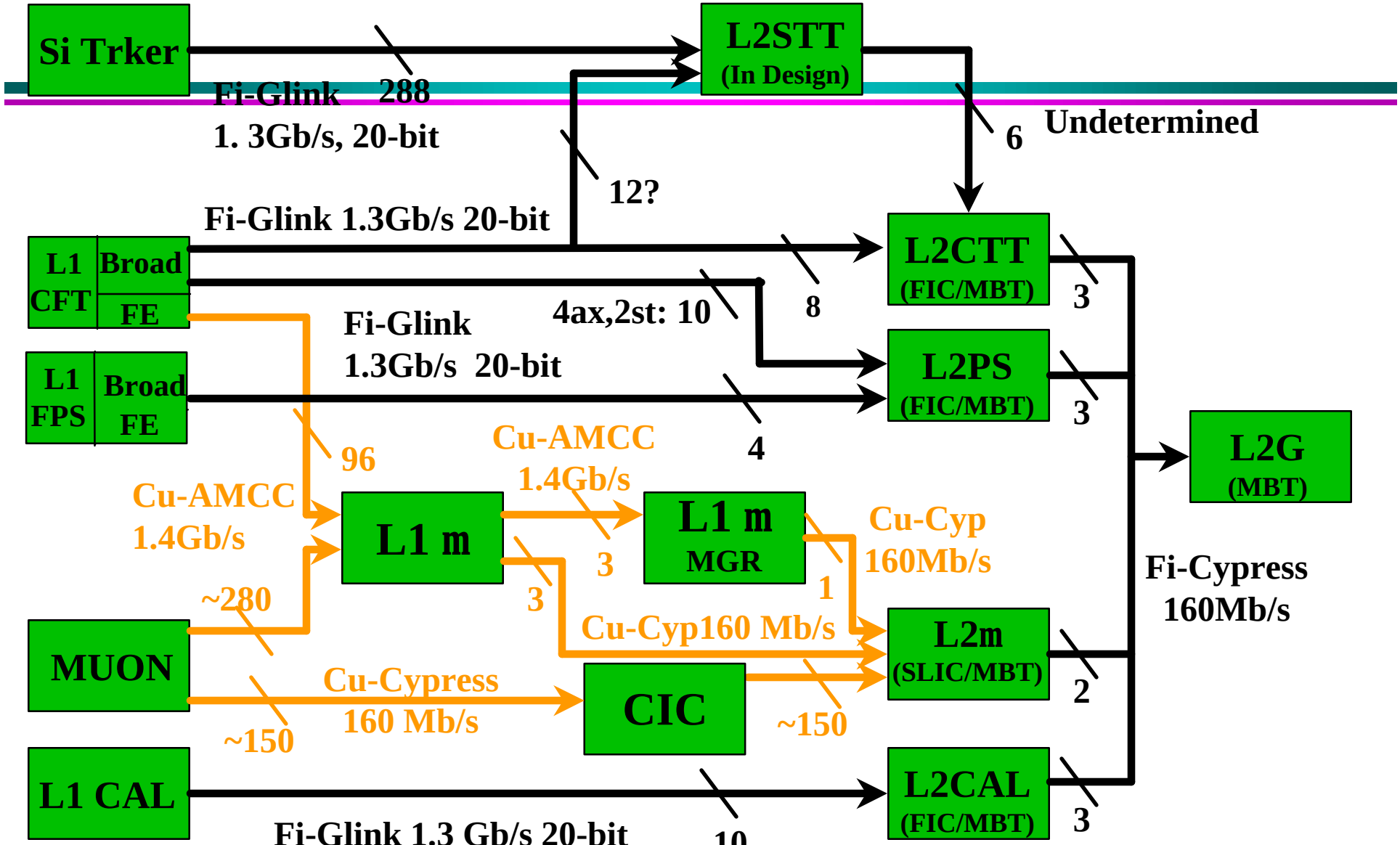
Standard Crate with FIC to SLIC



JTL, MSU 12/18/97

Trigger Connections



Test Stand at FNAL

- 4 crates:
  - Global simulator (Admin + Worker)
    - or CTT...
  - 2 preprocessor simulators (A+2W, A+W+Slic)
  - 1 data source (2alphas, MBT's; own MBus)
- Incomplete system--
  - no L1, L2
  - not enough parts for full code of any/all crates
    - except maybe full playback for Global
    - could reconfigure if need be--painful!
- Copy of some real-time inputs? (grounding!?)

Test Stand: What can it do?

- (Pre-)Commissioning/debugging (protoypes?)
  - alpha-alpha, alpha-MBT, SLIC-MBT-alpha issues
- Timing, verification of download (Alpha, SLIC)
  - run in real environment; count clock cycles
    - how good is offline simulator? (SLIC code differs…)
- Playback
  - drop data into memory (input only: cheap event dump?)
  - testing pre-release after running in simulator
- Debugging
  - event dump and restart (else debug = deadtime)
  - pretty tough to dump event unless Linux???

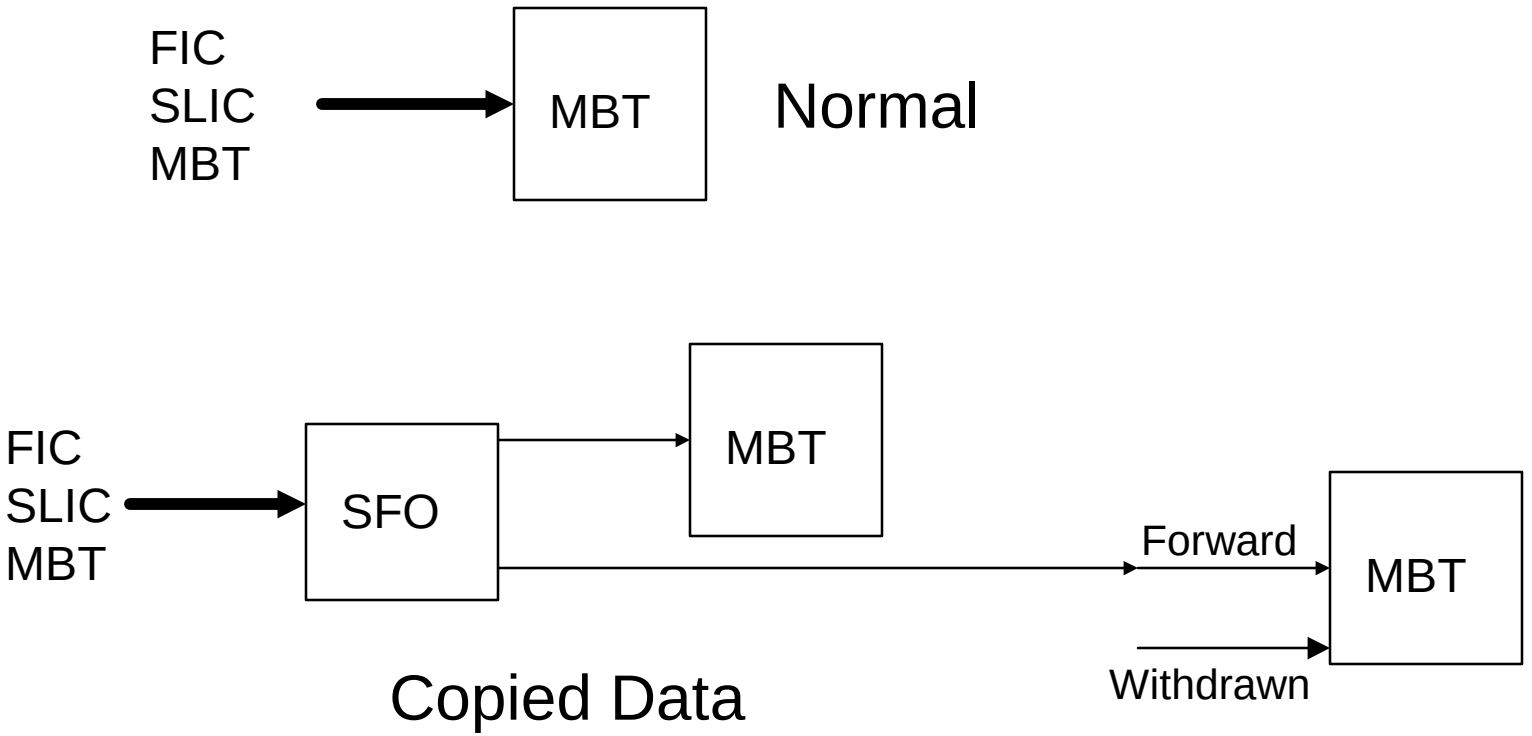
When do we want things?

- Crates on order, but 3 months
  - more spares from Marvin?
  - shuffle crates at Saclay, MSU, UIC, UMd, Nevis?
- Mbus backplane order ready to send to Myron
  - waiting on me! Hope not such a long leadtime...
- No power yet (may need design work...)
  - power requirements for cards not yet firm!
  - Need to sequence 5V vs 3V power???
  - Too much 3 V power for card pins?
    - Grab user bus?
- Bit3 617/618?
  - Order soon--618 problems traced to bad PCI crate

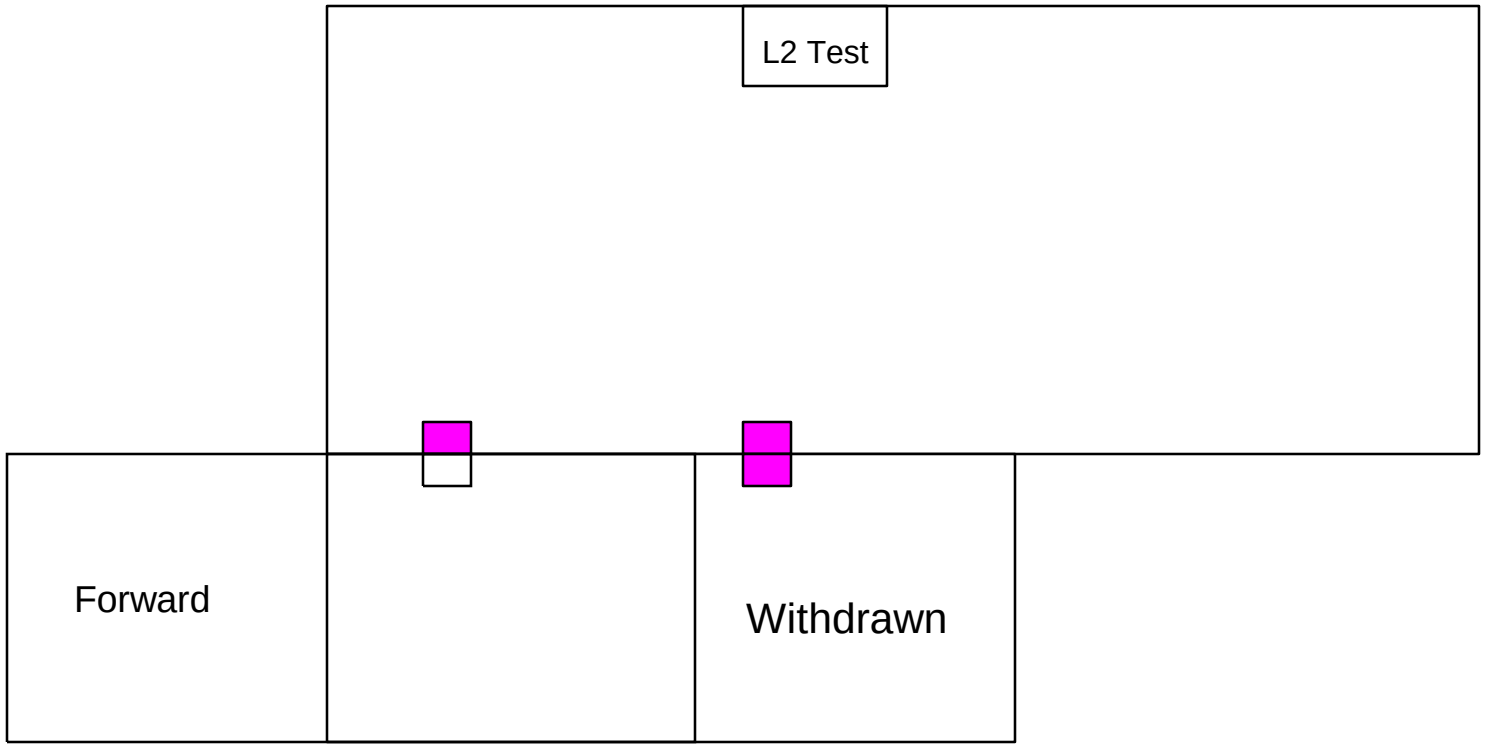
Fake Data Functionality For each(?) L2 crate in MCH:

- Copy of Alpha's or 1 SLIC's inputs
  - outputs captured at Global if needed...
- extra transmitter in or near each real crate
    - redefine SFO to 1in, 12 out, OR 6 in, 12 out
    - up to 3 slots per crate needed
  - extra cabling
    - sfo has extra input cables (female connector end??)
    - sfo has short output cables (copied input)
    - sfo has long output cables (to window in MCH)
- Recabling
  - how often can we afford to move it
  - moveable cabling vs lockable door, neat layout?

Cabling in sending crate: Logical (Alpha inputs)



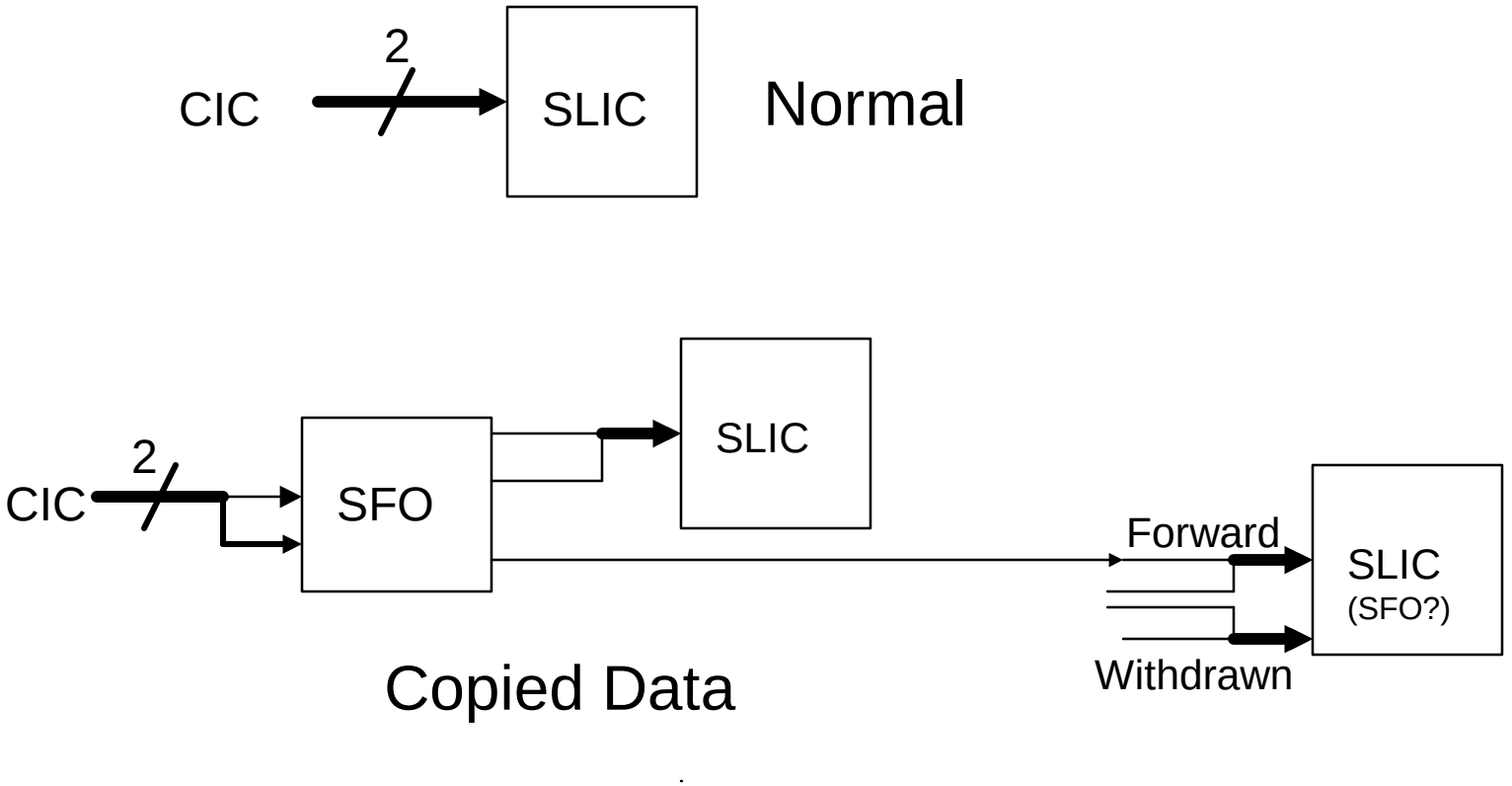
Moveable Counting House



Alpha Inputs: Physical

- Move Cable Bundles from MBT to SFO?
  - 7 inputs MBT; 6 inputs SFO
- Input cables to SFO unbundled, with female connector dangling?
- Short output cables of SFO unbundled, with male connector dangling?
- Space may be tight if > 3 workers
  - 2 to 3 SFO's needed per crate

Cabling in sending crate: Logical (SLIC inputs)



SLIC Inputs: Physical

- Cannot move Cable Bundles from SLIC to SFO
  - incompatible # inputs, 2 inputs per cable on SLIC
- short input cables to SFO unbundled, with female connector dangling?
  - Connections to SFO split 1 cable to 2 inputs
- Short output cables of SFO unbundled, with male connector dangling?
  - Connection to SFO split 1 cable to 2 outputs
- SFO needs different cable bundles for copying SLIC vs copying MBT inputs (BOTH of possible interest!)
- No spare room in central muon crate for 2-3 SFO's!
  - share with forward? SFO's in CIC crate?

Fake data receiving: Test Stand End

- Two sets of long input cables to each test stand crate
  - one for each wall window (positions of MCH)
  - SFO receiver and short cables needed too?
    - If SLIC can't receive long-haul cables…
    - at least, SLIC needs another set of short cables:
      - pairs of 1-signal female to 2-single male
  - repeat this setup for 3 (4?) test stand crates
- Assuming NOT attempting an optical split:
  - copy FIC outputs, not inputs

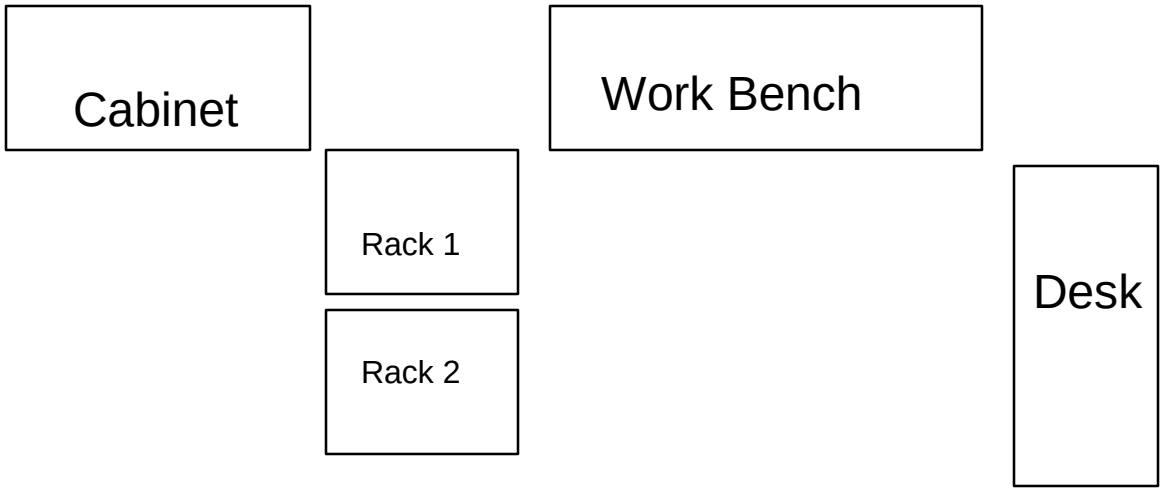
Test Stand Concerns

- Grounding
  - transformer coupling from MBT inputs
    - SLIC capacitor coupled???
      - Had assumed only short-run inputs to SLIC
      - SLIC's close to Calorimeter ADC's (analog)
      - Use SFO receiver with transformer + short cable?
- Cable Length: error rate
- Cable topology
  - MBT inputs have one input per cable
  - SLIC inputs have two channels per cable
    - get around with special forked cables?
    - Patch panel?
    - (dangerous) redefine everybody else to be 2-input?

Added functionality to support test data import

- Return busy to L2 crates (Pilot MBT)
  - stop data to resynchronize after debugging
  - otherwise, keep up, or let data fall on floor
- a branch of L3 needed to record test data?
  - And matching control system!
  - fake TCC: script from Coor or online dbase?
    - Global, or if software qualifiers for prepocessors
- Is there anything else we've forgotten?
  - SCL info? L1HWFW data? Fake these?
- Software: special/unofficial releases...

L2 Test Stand Layout?
2nd floor, North Wall



Needs coordination!

- Mario Vaz will coordinate engineering of test stand

Test Stand Data Copy Cost Estimate (ROUGH)

TEST STAND SETUP

1 crate:	number	length	cost	**Total Crates**	3	
SFO	3		1500	9	4500	needed?
cables	16	134	2144	144	6432	
short	1	10	17			needed?
in to hole1	1	75	59			
in to hole 2	1	75	59			
total			3644		10932	

Counting house setup

1 crate:				**Total Crates**	5	
SFO	3		1500	15	7500	
cables	16	81.75	1308	160	6540	
short cable	1	20	23			
wall cable	1	75	59			
			2808		14040	
			SFO	24	12000	
			cables	304	12972	
				total	24972	

Data Source Count

L2 Data Types and Source ID's

4/14/99 JTL **DRAFT** for inputs to MBT's

GS Crate/ID	Global *L2GLB 32* Contents	Data	Source	Central Mu *L2MUC 33* Contents	Data	Source	Forward Mu *L2MUF 34* Contents	Data	Source	Cal *L2CAL 35* Contents	Data	Source	Preshower *L2PSH 36* Contents	Data	Source	Tracking *L2CTT 37* Contents	Data	Source
	L1SCL*	0	0	L1SCL*	32	0	L1SCL*	64	0	L1SCL*	96	0	L1SCL*	128	0	L1SCL*	160	0
	L1HWFW	1	1	L1HWFW	33	1	L1HWFW	65	1	L1HWFW	97	1	L1HWFW	129	1	L1HWFW	161	1
	em	2	2	slic cen 1	34	2	slic fwd 1	66	2	cal 1	98	2	cps axial 1	130	2	CFT 1	162	2
Pilot MBT	jet	3	3	slic cen 2	35	3	slic fwd 2	67	3	cal 2	99	3	cps axial 2	131	3	CFT 2	163	3
	etmiss	4	4	slic cen 3	36	4	slic fwd 3	68	4	cal 3	100	4	cps axial 3	132	4	CFT 3	164	4
	pt track	5	5	slic cen 4	37	5	slic fwd 4	69	5	cal 4	101	5	cps axial 4	133	5	CFT 4	165	5
	impact track	6	6	slic cen 5	38	6	slic fwd 5	70	6	cal 5	102	6	cps axial 5	134	6	CFT 5	166	6
	mu central	7	7	slic cen 6	39	7	slic fwd 6	71	7	cal 6	103	7	cps axial 6	135	7	CFT 6	167	7
	mu forward	8	8	slic cen 7	40	8	slic fwd 7	72	8	cal 7	104	8	cps axial 7	136	8	CFT 7	168	8
Assistant	ps central	9	9	slic cen 8	41	9		73	9	cal 8	105	9	cps axial 8	137	9	CFT 8	169	9
MBT	ps north	10	10	slic cen 9	42	10		74	10	cal 9	106	10	cps stereo 1	138	10	STT 1	170	10
	ps south	11	11	slic cen 10	43	11		75	11	cal 10	107	11	cps stereo 2	139	11	STT 2	171	11
	zvtx	12	12	slic cen 11	44	12		76	12		108	12	fps north 1	140	12	STT 3	172	12
		13	13		45	13		77	13		109	13	fps north 2	141	13	STT 4	173	13
		14	14		46	14		78	14		110	14	fps south 1	142	14	STT 5	174	14
													fps south 2	143	15	STT 6	175	15
				Outputs:			Outputs:			Outputs:			Outputs:			Outputs:		
				mu central			mu forward			em			ps central			pt track		
										jet			ps north			impact track		
										etmiss			ps south			zvtx		

Crates/Test Stand Schedule

Crate #	Date	Usage	Date	Usage	Date	Usage	Date	Usage
1	Jun-98	MSU Swe						
2	Jun-98	UIC Swe	Aug-99	UIC Alpha	Jan-00	Test/Pre2		
3	Jun-98	Umd MBT					Mar-00	Mu Fwd
4	Jan-99	Saclay FIC			Jan-00	CFT		
5	Jan-99	Nevis SLIC/STT					Jul-00	Spare
6	Feb-99	BU STT?					Jul-00	Spare
7	Feb-99	SUNY STT?					Mar-00	Test/Data
8			Aug-99	Test/GL/work				
9			Aug-99	Test/Pre1				
10			Aug-99	Global				
11			Aug-99	Cal				
12					Jan-00	Mu Central		
13			Aug 99	NebraskaCIC/SFO?	Jan-00	PS		

Test Stand at FNAL:

global-like	admin+worker
Pre1	admin+2 workers
Pre2	admin+2 slic + worker + 2fic
data/testing	alpha+2 MBT's + various warm spares; useable for testing/repair with extenders

NOTE: Proposed Eventual configuration. Details may vary. nodes are scheduled among groups to carry out testing

Common Controls

- VME: 2 levels of reset for specific card
  - 1) Initialize This Card (simulate power cycle)
    - after safety catch released?
  - 2) reset this card (only) don't reload FPGA, but
    - go to state 0 and discontinue all activity
    - clear data buffers
    - need not clear control registers; let Alpha reprogram?
- VME SYSRESET:
  - would prefer this just cleared bus?? Or job of Bit3?
  - believe VBD does full reset on this, too
- VME SYSFAIL
  - prefer to do nothing (except Administrator…)
  - want to use as interrupt for SCL_INITIALIZE from MBT to Admin
- MBReset
  - drop Mbus cycle

More common stuff...

- Register to read current fpga code version(s)?
  - Not clear how important…
  - but DO want version control, maybe with code put in cvs repository, and change dates to dbase…
- geo addressing to set base address
- NO POWER ORDER DEPENDENCE
  - take care of it on your card if you have to
- front panel button: simulate power cycle