Alpha and L2 Test Stand

James T. Linnemann

MSU

Collaboration Trigger Meeting

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Alpha Production Status

- 3 pre-production prototypes
- acceptable quality EXCEPT

  L3 Cache can't be made to work *reliably (=all 3)*

  do work reliably without L3 Cache (white wire)

  - uses 96KB L2 cache on-chip
- layout problems, but simulations don't cleanly finger the problems
- can't just copy COMPAQ layout

  PCI slots must be organized differently

Is this a problem?

- L3 cache probably not needed…

  provided program and lookup fits in 96KB

  plausible: =12K instructions = 24 µsec

  - code has loops, so enough for > 50 µsec budget
- 2% timing effect for algorithms tested

  cal Etmiss, cal jet, cal em, TOY global
- × 1.8 for huge program (Linux compile)

  even that is within our safety factor...

Plan

- Partial production

  August: verify full global doesn’t need cache

  - if so, build rest of boards then

  modest financial penalty (5K or less)

  however…CDF will build all its boards

  - I would guess this decreases their motivation to participate if we must redo layout

How many to build?

- DØ 38; spare parts 10; CDF 10
- Assume likeliest scenario:

  wait a few months, build rest in same design
- BUT want to survive if:

  need new layout: December earliest
- some possible strategies:

  enough to run March 2000 (prefer)

  as few as possible now
  - in case we need LOTS of new layout
  - but clumsy for commissioning

	baseline	1st year		"minimum"	min commission	
Test Stand Crate 1	2	2		2	2	"global"
Test Stand Crate 2	3	3		3	3	"multiprocessor"
Test Stand Crate 3	2	2		0	0	2nd preprocessor test
Test Stand Crate 4	0	0		0	0	data source uses prototypes
Global	2	2		2	2	
Cal	4	4		4	0	L1: Aug
PS	3	3		2	0	L1: Sept
CTT	4	2		2	0	L1 Sept; STT 2001
Mu	4	4		2	2	one crate: L1 June
total	**24**	**22**		**17**	**9**	**imaginable partial production**
spare/extra power	14	16		21	29	
	38	38		38	38	
pre-production	2	2		2	2	as good as final cards
spare parts	10	10		10	10	but some needed by CDF too
old prototypes	2	2		2	2	OK for data sources or some testing
We don't have enough parts to build the system twice.						
Could build all baseline workers twice						
Administrators:						
test stand	3					
real system	6					
total admin	9	9		7	4	
workers	15	13		10	5	

Suggested Production

- 24 boards = 1st year + 2 more spares

  (can use current prototypes as well)

  test stand for extra power, more spares
- leaves 14 more for 2nd round if needed

  baseline has 11 workers in L2 crates
  - 3 for spares, extra power, or test stand

Test Stand Activities: Hardware dominated

- Pre-production prototype integration OK for
  - **MBT ® Alpha (and Mbus backplane)**
  - **FIC ® MBT ® Alpha**
  - **SLIC ® MBT ® Alpha**
- Currently testing SFO:
  - **FIC ® SFO ® MBT ® Alpha**
  - **FIC ® SFO ® SLIC ® MBT ® Alpha**
- no cables to real data sources yet
- coming: **Alpha-Alpha**, VBD/L3

L2 in MCH

- **CIC** Bit Error Rate tests (II) next week
- no connections yet to real DAQ

  cables; crates/power in MCH needed
- need to integrate Global, L2HWFW

  power, cables, adapt MBT prototype(?)

  when needed?
- connections of Alpha to L1 Scalers

  new cables, and adapter card design needed
- Production boards in July: Commissioning

  Consistent with L1, L3 expectations?