Alpha and L2 Test Stand

James T. Linnemann
MSU
Collaboration Trigger Meeting
May 11, 2000
Alpha Production Status

• 3 pre-production prototypes

• acceptable quality EXCEPT
  
  L3 Cache can’t be made to work reliably (=all 3) do work reliably without L3 Cache (white wire)
  
  • uses 96KB L2 cache on-chip

• layout problems, but simulations don’t cleanly finger the problems

• can’t just copy COMPAQ layout
  
  PCI slots must be organized differently
Is this a problem?

• L3 cache probably not needed…
  provided program and lookup fits in 96KB
  plausible: =12K instructions = 24 µsec
    • code has loops, so enough for > 50 µsec budget
• 2% timing effect for algorithms tested
  cal Etmiss, cal jet, cal em, TOY global
• × 1.8 for huge program (Linux compile)
  even that is within our safety factor...
Plan

- **Partial production**
  
  August: verify full global doesn’t need cache
  
  - if so, build rest of boards then
  
  modest financial penalty (5K or less)
  
  however…CDF will build all its boards
  
  - I would **guess** this decreases their motivation to participate if we must redo layout
How many to build?

- DØ 38; spare parts 10; CDF 10
- Assume likeliest scenario:
  wait a few months, build rest in same design
- BUT want to survive if:
  need new layout: December *earliest*
- some possible strategies:
  enough to run March 2000 (prefer)
  as few as possible now
    - in case we need LOTS of new layout
    - but clumsy for commissioning
<table>
<thead>
<tr>
<th></th>
<th>baseline</th>
<th>1st year</th>
<th>&quot;minimum&quot; min commission</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Stand Crate 1</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Test Stand Crate 2</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Test Stand Crate 3</td>
<td>2</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>Test Stand Crate 4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Global</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Cal</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>PS</td>
<td>3</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>CTT</td>
<td>4</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Mu</td>
<td>4</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td><strong>total</strong></td>
<td><strong>24</strong></td>
<td><strong>22</strong></td>
<td><strong>17</strong></td>
</tr>
<tr>
<td><strong>spare/extra power</strong></td>
<td><strong>14</strong></td>
<td><strong>16</strong></td>
<td><strong>21</strong></td>
</tr>
<tr>
<td><strong>pre-production</strong></td>
<td><strong>38</strong></td>
<td><strong>38</strong></td>
<td><strong>38</strong></td>
</tr>
<tr>
<td><strong>spare parts</strong></td>
<td><strong>2</strong></td>
<td><strong>2</strong></td>
<td><strong>2</strong></td>
</tr>
<tr>
<td><strong>old prototypes</strong></td>
<td><strong>10</strong></td>
<td><strong>10</strong></td>
<td><strong>10</strong></td>
</tr>
<tr>
<td><strong>We don't have enough parts to build the system twice.</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Could build all baseline workers twice</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Administrators:</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>test stand</td>
<td><strong>3</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>real system</td>
<td><strong>6</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>total admin</strong></td>
<td><strong>9</strong></td>
<td><strong>9</strong></td>
<td><strong>7</strong></td>
</tr>
<tr>
<td><strong>workers</strong></td>
<td><strong>15</strong></td>
<td><strong>13</strong></td>
<td><strong>10</strong></td>
</tr>
</tbody>
</table>
Suggested Production

• 24 boards = 1st year + 2 more spares
  (can use current prototypes as well)
  test stand for extra power, more spares
• leaves 14 more for 2nd round if needed
  baseline has 11 workers in L2 crates
  • 3 for spares, extra power, or test stand
Test Stand Activities:
Hardware dominated

• Pre-production prototype integration OK for
  MBT → Alpha (and Mbus backplane)
  FIC → MBT → Alpha
  SLIC → MBT → Alpha

• Currently testing SFO:
  FIC → SFO → MBT → Alpha
  FIC → SFO → SLIC → MBT → Alpha

• no cables to real data sources yet
• coming: Alpha-Alpha, VBD/L3
L2 in MCH

- **CIC** Bit Error Rate tests (II) next week
- no connections yet to real DAQ
cables; crates/power in MCH needed
- need to integrate Global, L2HWFWpower, cables, adapt MBT prototype(?)when needed?
- connections of Alpha to L1 Scalersnew cables, and adapter card design needed
- Production boards in July: CommissioningConsistent with L1, L3 expectations?