The D0 Upgrade Level 2 Trigger

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Overview

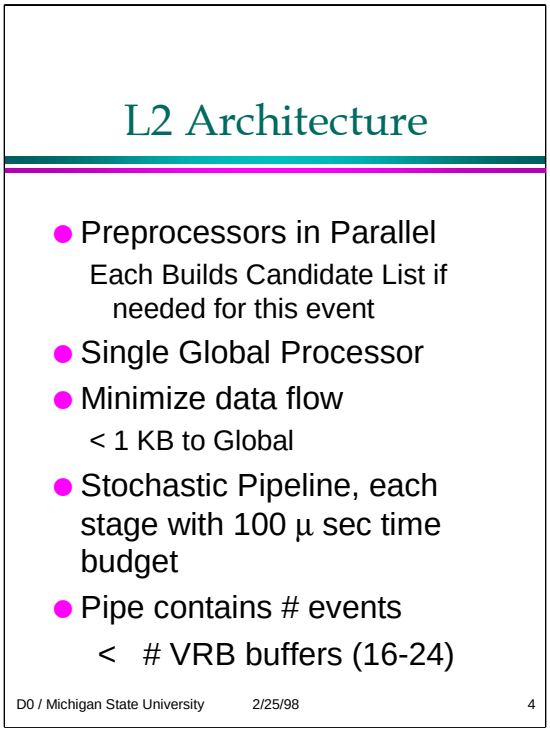
- L2 Requirements
- Architecture Chosen
- Cal e, μ Preprocessor as examples: Algorithm, Timing
- Global Processor
- RISC Vs. DSP
- Queuing Simulations
- Costs
- Summary

Level 2 Requirements

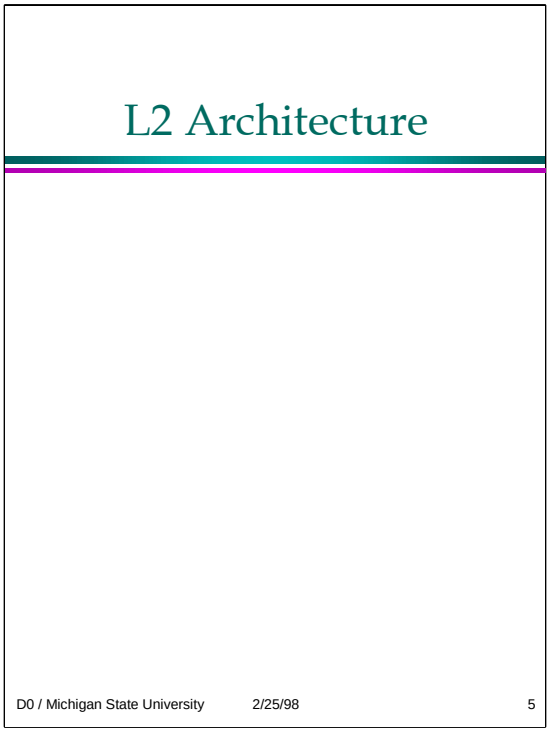
- Level 1, Level 3 (Approved)
  - Level 1: 10 K Hz Output
  - Level 3: 1 K Hz Input
- Level 2 (Approved in Principle)
  - Details today
- L2 Requirements
  - 10 K Hz @ deadtime < few %
    - => 100 μ sec to handle event
  - Rejection X 10

What is projected L3 output

10 - 20 Hz



how many KB to each preprocessor?



SVX under study

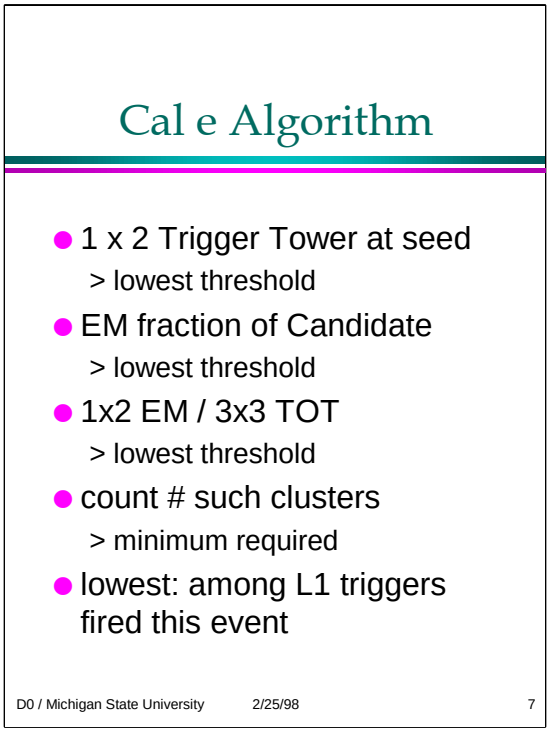
fits into scheme without new problems to face

Steps to L2 Decision: Calorimeter e Example

- Input Preprocessor Data
- Unpack L1 seed locations
- Apply electron algorithm
- Make candidate list for Global and L3
  - » Preprocessor is Single RISC

- Global will match Cal with Track
  - » spatial and p_T matches

Rejection from Cal alone is about 4 using 10 -> 15 GeV threshold and ISO; then independent factor from phi match at 1 TT to track boosts to rejection of 9

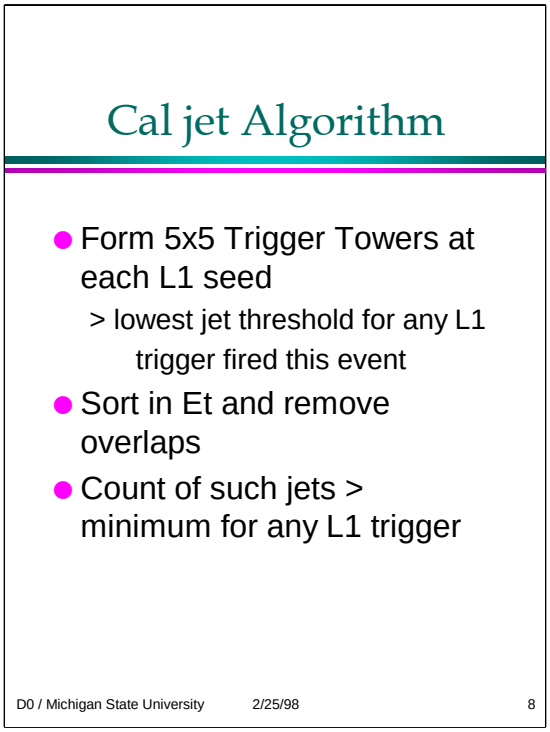


what is efficiency, rejection? about 4 at 98% on Z's

timing on Mon stream at 3 luminosity's

7 GeV Em ET from L1 10 GeV 1X2 cluster
em fract > .8, iso , .01

1 usec overhead, 2.8 average
2.1 usec per speed
multiplicity 1-2 seeds/event
slow with luminosity



jet efficiency, rejection???

no Etmiss: since no new info (at 396 anyway) est 50 usec just to tower scan. Without IF's, there might be hope to do etmiss; no Zv in any case

3 GeV L1 to 15 GeV

3 usec

2.2/seed, 1.1 /cluster

average seeds is 3 -> 6 at high lum

more lum dependent than electron

therefore, distribution is broader than for electrons

Cal Preprocessor Timing (μ sec)

	Electrons	Jets
Buffer Fill	13-50	13-50
Unpack L1 Seeds	2	2
Algorithm	3-10	8-30
Output	5	5

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2nd figure is for 132 nsec bunch spacing

Data input speed independent of processor; other factors scale

Times scaled from a model 300 Alpha, about 100 MIPS / 2 ~ M700

should be at least 1.5 X latest chip Vs. M700

in addition, UNIX C faster than VMS C

I have applied that scaling factor here

L2 μ Preprocessor

- Capture data in L2 buffers
- transfer nonzero to DSPs
  128 per commercial VME card
- DSP for each region
  does fixed # of combinations
- Segment before, after Toroid
  Joined by Global Processor
- Runs in Constant time
- Does not use L1 seeds
  so better ε for untriggered μ

CENTRAL

Rejection is 7.8 track, 5 for scint (tho not indep)

efficiency on Run 1 data is 95% track, 99% scint

L2 μ Layout

μ Algorithm

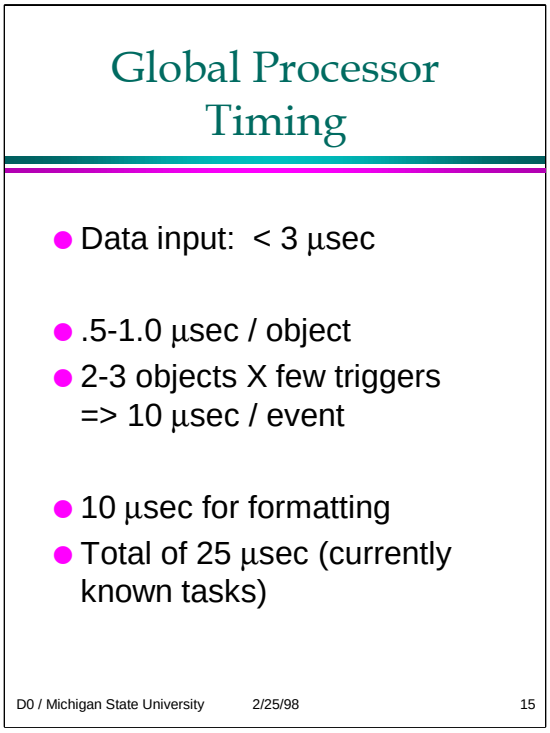
- capture data <20 μ sec>
- transfer to DSP <20 μ sec>
- Histogram all combinations of hits in region local straight line coordinates (r- ϕ, r- z)
- pick best position, slope if any (fixed 30 μ sec)
- format output <20 μ sec>

Details of L2 μ

- Segment carries scintillator time
- Delta-times used for r-ϕ
- Efficiency:
  95% for tracks, 99% for scint
- Rejection:
  7.8 for track, 5 for scint
- Algorithm tested on Run 1
- Forward: similar, but resolution from tubes, not T

Global Processor

- Fill Buffers during Processing
  test Preprocessor candidates
  lists for each L1 trigger fired:
- validate candidates, e.g..
  μ segments -> tracks ; p_T > cut
  e > thresholds for this L1 trigger
- e = cal+track+preshower
- combine e, jet, μ
- cut on masses, $\Delta\eta$, $\Delta\phi$...
- Single RISC processor
  2 on same event if needed



256 B/80 MB/sec = 3 usec or so (u is worst case)

Here timing is on M300/2, VMS C, so really expect * 1.5 better

but beware, this is 2* as fast as CDF saw for real

room for expansion here

mu track matching NOT included so far

L2 Global Data Inputs (per "typical" event)

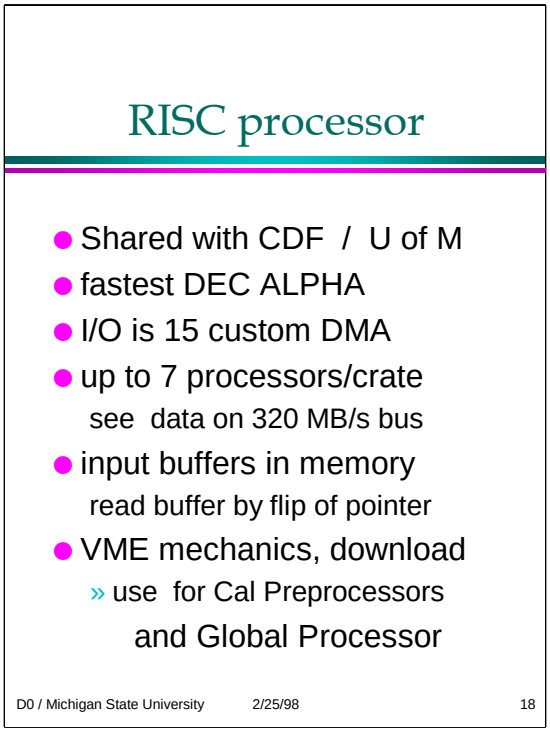
e: 2 X12 B =	24 B
j: 4 X 8B =	32 B
CFT: 10 X 8B =	80 B
includes preshower	
muon: 16 X 16B =	256B
FPS: 5 X 4B =	20B
CPS: 5 X 4B =	20B
SVX(?) 10 * 16B =	160B
Total	450-600B
	= 5 MB/sec

Put Dan Owen's list here

This is still 5-10 MB/sec

Processor Choices

- RISC
  - if need code flexible
  - if a few processors enough
    - » CAL e, CAL jet
    - » Global
- DSP
  - if massive parallelism needed
  - fixed execution time, candidates
    - » μ, r-ϕ, u-v



CDF is 21064 at 150 MHz 7 ns/instruction cycle, 2 inst/cycle

equiv to M400 workstation, so faster than our M300 by perhaps 1.3 - 1.5

our M300 was in the 80-90 Specint range I think

next is 21164 at 400 MHz, 2.5 / inst cycle, 4 instructions/cycle,

L2 cache on chip

500 Specint92

Therefore about 5* faster than our M300 times

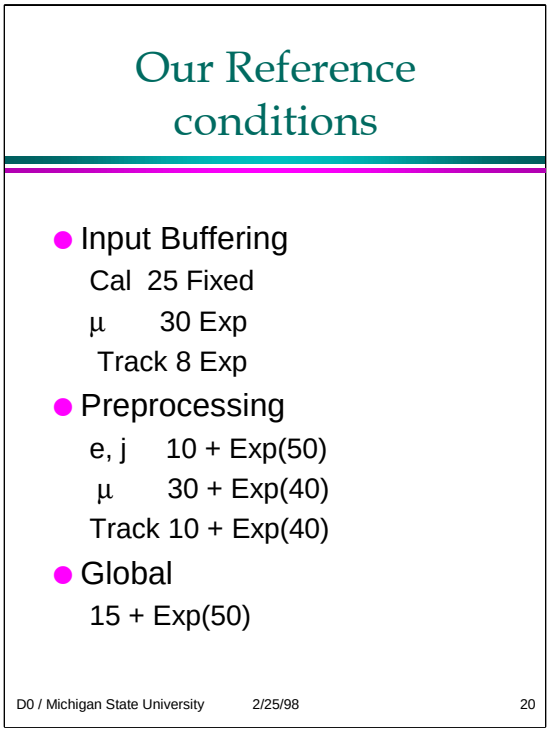
we have taken a factor of 2 of out of this 5

SO SHOULD STILL BE X 2.5 faster than these numbers!!!!!

guess 80 MB/ DMA engine; if 100 ns/xfer, 4B/xfer would be 40 MB/s each

Queuing Simulations

- Main Tool is RESQ
- For Exponential Processing time:
  - Check with Analytical results for single queues
  - Check with Numerical results for coupled queues
- Fixed times give lower deadtimes than Exponential for same mean time
  - » Actual: Fixed + Exponential



at 396, CAL could go up to 50, a problem unless more buffering applied

e and j are probably both pessimistic

mu is probably about right, tho exponential is perhaps harsh for both track and mu

50 seems pretty generous for Global

Queuing Results

- Nominal budget: 100 μsec
- Preprocessors: several: interplay => stay further from budget, or more buffers
  - » 12 buffers, 50-70 μsec max
- Global: single => can go closer to budget
  - » 4 buffers, 60-70 μsec max

L2 Cost Estimate

Muon Preprocessor	$340 K
e, jet Preprocessors	$270 K
r-ϕ Track Preproc.	$170 K
u-v Track Preproc.	$450 K
Global Processor	$170 K
Total	$1400 K

additional RISC board is about 20K

15 year FTE engineering

put detailed costs here

Commercial DSP

Shared VME/RISC with large I/O bandwidth

L2 Summary

- Architecture Chosen
  - minimize data flow
  - timing, buffer limits understood
  - timing studies show achievable
- RISC shared with CDF
  - flexible code, a few processors
    - Global, Cal Preprocessors
- DSP commercial (CNAPS ?)
  - fixed time parallel algorithms
  - μ, tracking Preprocessors

L2 Summary, 2

- Preprocessors
  12 -16 buffers, 50-70 μsec
- Global processor
  4-16 buffers, 50-70 μsec
- Budget: $1.4 M

Conclusion

- L2 studied with enough detail to understand problems and their solutions
- L2 already approved in principle
- L2 necessary, given D0 bandwidth goals

SVX L2 trigger: Physics motivation

- Group studying (Winer et al)
  - » Improve p_T resolution (e, μ)
  - » soft multileptons (SUSY)
  - » tau, all Jets (H_T cut)
  - » Single Top (and Γ_t)
  - » single μ reduce to b -> μ or b, μ on opposite sides
  - » similarly for μ μ
  - » stop -> jets with b tag
  - » b bbar jet or dijet
- Fits smoothly into L2 design

CFT uv Algorithm

- buffer in uv data, r-ϕ L1 info
- form xuv combinations
- find z of uv pairs
- buffer r-z hits
- send each combination of z hits/layers to a DSP
- DSP farm calculates
  χ^2, z intercepts in parallel

rejects combinatorics by factor of 20

efficiency of 95% for < 4 interactions, 85-90% for lum-wtd

maybe better if allow more tracks than 2/region: slower than for L1

trigger on 2-tracks at 8 X 3 GeV of L1 < 1 KHz if L1 device