L2 Review Summary

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Synopsis

- Try to highlight items not already assumed or emphasized in L2 plans

Fragility Concerns: Debugging

- Yes to all methods…(symptom of concern)
  - root concern: not a farm, so debug online = dead
    - event dump
      - pretty tough, must try (Linux to rescue?)
    - extract Linux memory protection (avoid re-d/l of .exe?)
      - seems VERY ambitious; will consult with Guru Scott
    - realtime copies of (subsets of data) to test stand
      - looks promising, will cost money
- version control for all FPGA's
  - to database every run?
  - Software version is assumed requirement…

Fragility: People

- understudies for experts
- new groups for manpower
  - in addition to grad students in present institutions
  - clearly needed for upcoming tasks (many offline!)
    - underestimated?
      - schedule/manpower not reviewed in detail
- Documentation:
  - introductory, so people can join
    - web site is already rather large
      - perhaps not so easy to enter
      - committee probably read only TDR's under review?
  - plan structure for software docs

Hardware Fragility

- Alpha board parts going obsolete
  - parts stockpiling for those going obsolete
    - under way
  - next generation boards: start planning? (cost?)
  - fund repair site (where? PREP not interested)
    - curious: other boards not given similar emphasis...
- Cypress testing
  - more links, longer term
  - “realistic noise”

Error recovery

- timeouts and auto-repair code desired
- concern (and some confusion) on SCL_INIT
  - worry about speed (Why?)
    - SCL_INIT rate MUST be kept small
  - .exe download, run start (Why for SCL_INIT?)
  - can it cure all hangups? (No…need other means)
- I interpret: want time estimates for
  - resets of various severity
  - reload code + parameters after crash
    - avoid begin/end run

Alpha

- Make boards identical to CDF
  - redesign to make driver section a mezzanine
    - is this so critical we should take a delay? (how long?)
    - Cf. Recommedation to start production asap
    - 15 min to convert
- large insertion force (all VME64 cards)
  - crate design currently frozen; insertion tab design?
- Buy 3 spares “just in case”
  - enough to cure a single Alpha X2 time overrun
    - beyond existing safety factors

SLIC

- Need timing of realistic muon algorithms
- add FIFO to increase output BW
- flexibility to be used in other processors?

Recover ability to run RESQ!

- a little help from FNAL?
- More work on schemes for a slow Global
  - probably awaits better input:
    - measurements of response times
    - simulator timings of real algorithms (with tails)
- STT design optimization

Monitoring

- More interaction with online group
  - beginning: monitoring session display wish list
- document contents of monitoring data
- automated verification critical
  - requires simulator
    - foreseen...

Other general concerns

- Jet efficiency low?
  - MC scale problems make this murky
  - Inherent limitation is probably L1 E calibration?
- 128 bit limitation in L2
- further reviews of algorithms needed
- do software release tools meet L2 needs
  - in process of learning this…
- SIMULATOR
  - for experts, and user friendly too…
- purchasing with STT in view? (…budget)