ID	Task Name	Duration	Start	Finish	Predecessors	% Compl	Cc	WI	Resource Names
1	**Trigger System**	**237 w**	**Mon 10/2/95**	**Mon 7/10/00**		**55%**	**As**		
2									
3	**Framework**	**165.4 w**	**Tue 1/2/96**	**Fri 4/30/99**		**91%**	**As**		
4	Foundation Module Board Design	36 w	Tue 1/2/96	Thu 9/12/96		100%	St	1.4	k$[39%],k$c[2%]
5	Design the Derivative Boards	78 w	Wed 6/19/96	Wed 1/21/98	4SS+24 w	100%	As	1.4	EEU141,k$[39%],k$c[2%]
6	***Circuit Board Layout Finished***	***0 w***	***Wed 1/21/98***	***Wed 1/21/98***	***5***	***100%***	***As***		
7	FPGA Code for Foundation Module	16 w	Wed 6/19/96	Thu 10/10/96	4SS+24 w	100%	As	1.4	EEU141,k$[39%],k$c[2%]
8	FPGA Code for the Derivative Boards	97 w	Fri 9/13/96	Fri 8/28/98	7SS+12 w	100%	As	1.4	EEU141,k$[39%],k$c[2%]
9	L1/L2 Support Equipment	102 w	Tue 1/2/96	Wed 1/21/98	4SS	100%	St	1.4	EEU141[50%],k$[201%],k$c[11%]
10	Serial Command Link Receiver	101 w	Tue 12/10/96	Wed 1/6/99		80%	St	1.4	EEF141
11	Serial Command Link Transmitter	101 w	Tue 12/10/96	Wed 1/6/99	10SS	80%	As	1.4	ETF141[60%]
12	Build Cards and Assemble L1 Framework	86 w	Fri 2/28/97	Mon 11/16/98	5SS+50 %	100%	As	1.4	EEU141[50%],k$[572%],k$c[13%]
13	L1 Framework Testing	4 w	Tue 11/17/98	Wed 12/16/98	12	0%	As		
14	***L1 Framework Delivered to Fermilab***	***0 w***	***Wed 12/16/98***	***Wed 12/16/98***	***13***	***0%***	***As***		
15	Commission L1 Framework for First User	4 w	Thu 1/7/99	Wed 2/3/99	14,10,11	0%	As		
16	Build Cards for L2 Framework	32 w	Thu 4/2/98	Mon 11/16/98		100%	St	1.4	EEU141[50%],k$[327%],k$c[8%]
17	Assemble L2 Framework	4 w	Mon 3/1/99	Fri 3/26/99	16	0%	St		
18	L2 Framework Testing	1 w	Mon 3/29/99	Fri 4/2/99	17	0%	As		
19	***L2 Framework Delivered to Fermilab***	***0 w***	***Fri 4/2/99***	***Fri 4/2/99***	***18***	***0%***	***As***		
20	Commission L2 Framework at Fermilab for First User	4 w	Mon 4/5/99	Fri 4/30/99	19	0%	As		PhysU141[50%],EEU141[50%]
21									
22	**Trigger Control Software**	**213.4 w**	**Tue 1/2/96**	**Fri 4/21/00**		**59%**	**As**		
23	Implement L1 Exerciser/Diagnostics with NT	36 w	Tue 1/2/96	Thu 9/12/96		100%	St	1.4	EEU141[50%],k$[39%],k$c[2%]
24	Operate L1 Frame with Trg Mon	90 w	Fri 2/28/97	Wed 12/16/98	12SS,23	80%	As	1.4	EEU141,k$[39%],k$c[2%]
25	Operate L1 Framework at FNAL	4 w	Thu 12/17/98	Wed 1/27/99	24,13	0%	As	1.4	EEU141,k$[39%],k$c[2%]
26	Operate L2 Framework at FNAL	4 w	Mon 4/5/99	Fri 4/30/99	25,18	0%	As		
27	Operate Frameworks, L1 Calor, L2 Trigger	24 w	Mon 5/3/99	Wed 10/20/99	26	0%	As		EEU141
28	Operate with Rate Control, Servers, Data Logging	24 w	Thu 10/21/99	Fri 4/21/00	27	0%	As		
29									
30	**Level 1 Calorimeter Trigger**	**174.8 w**	**Tue 10/1/96**	**Thu 4/20/00**		**55%**	**As**		
31	Determine Specifications	99 w	Tue 10/1/96	Wed 9/30/98		100%	As	1.4	PhysU143[50%],EEU143,k$[13%],k$c[3%]
32	Design and Build Cal to L3 Readout	16 w	Thu 10/1/98	Fri 2/5/99	31	10%	As	1.4	
33	Design and Build Cal to L2 Readout	16 w	Mon 5/31/99	Tue 9/21/99	31,121	10%	As		
34	***M3-Complete Cal Readout to L2***	***0 w***	***Tue 9/21/99***	***Tue 9/21/99***	***33***	***0%***	***As***		
35	Design and Build Quadrant Signal Readout	16 w	Thu 10/1/98	Fri 2/5/99	31	10%	As	1.4	
36	Design and Build And/Or Readout	16 w	Thu 10/1/98	Fri 2/5/99	31	10%	As	1.4	
37	Modify Analog Input Cirucuits	8 w	Wed 9/22/99	Tue 11/16/99	32,33,35,36	0%	As	1.4	
38	Design and Build TCC Interface	8 w	Wed 11/17/99	Thu 1/27/00	37	0%	As	1.4	
39	Commission L1 Cal Trigger	12 w	Fri 1/28/00	Thu 4/20/00	38	0%	As	1.4	PhysU143[50%],EEU143[50%],k$[62%],k$(
40	***M3-Calorimeter Level 1 Trigger Commissioned***	***0 w***	***Thu 4/20/00***	***Thu 4/20/00***	***39***	***0%***	***As***		
41									
42	**Level 1 Muon Trigger**	**201.8 w**	**Tue 1/2/96**	**Tue 2/1/00**		**38%**	**As**		
43									
44	**Level 1 Central Fiber Tracker**	**114.8 w**	**Mon 11/3/97**	**Fri 3/10/00**		**33%**	**As**		**PhysF143[150%],EEU143**
45	Specification Stage	23.8 w	Mon 11/3/97	Fri 5/1/98		100%	St		
46	***Acceptance of Specifications***	***0 d***	***Fri 5/1/98***	***Fri 5/1/98***	***45***	***100%***	***As***		
47	Preliminary Design	18 w	Sun 2/1/98	Mon 6/8/98		100%	As		
48	Final Design	26 w	Tue 6/9/98	Fri 12/11/98	47	90%	As		
49	Final Design Review	4 w	Mon 12/14/98	Fri 1/22/99	48	0%	As		
50	***Final Design Review Completed***	***0 d***	***Fri 1/22/99***	***Fri 1/22/99***	***49***	***0%***	***As***		
51	Design Firmware	10 w	Mon 12/14/98	Fri 3/5/99	48	0%	As		
52	Software Emulation	20 w	Mon 12/14/98	Fri 5/14/99	48	0%	As		
53	Design PCB Layouts	8 w	Mon 1/25/99	Fri 3/19/99	50	0%	As		
54	***Layouts Accepted***	***0 w***	***Fri 3/19/99***	***Fri 3/19/99***	***53***	***0%***	***As***		
55	Procure Parts	20 w	Mon 1/25/99	Mon 6/14/99	50	0%	As	1.4	k$[198%],k$c[35%]
56	Procure Programmable Logic Devices	8 w	Mon 1/25/99	Fri 3/19/99	50	0%	As	1.4	
57	Test Cable	10 w	Mon 1/25/99	Fri 4/2/99	50	0%	As		ETF143[20%]
58	Produce Boards	8 w	Tue 6/15/99	Tue 8/10/99	56,55,53,57	0%	As	1.4	
59	Assemble and Test 10% of PCBs	8 w	Wed 8/11/99	Wed 10/6/99	58	0%	As		ETF143
60	***Acceptance of PCB Performance***	***0 w***	***Wed 10/6/99***	***Wed 10/6/99***	***59***	***0%***	***As***		
61	Assemble and Test Remaining PCBs	16 w	Thu 10/7/99	Fri 2/11/00	60	0%	As		
62	Commission CTT	20 w	Thu 10/7/99	Fri 3/10/00	61SS	0%	As		
63									
64	***M3 L1 Commissioned***	***0 w***	***Thu 4/20/00***	***Thu 4/20/00***	***30,42,44***	***0%***	***As***		
65									
66	**Level 2 Trigger**	**237 w**	**Mon 10/2/95**	**Mon 7/10/00**		**56%**	**As**		
67									
68	**Develop Conceptual Design**	**104 w**	**Mon 10/2/95**	**Fri 10/24/97**		**100%**	**As**		
69	Design Overall Architecture	104 w	Mon 10/2/95	Fri 10/24/97		100%	St		PhysU144[10%]
70	Deadtime Queuing Simulations	104 w	Mon 10/2/95	Fri 10/24/97		100%	St		PhysU144[20%]

ID	Task Name	Duration	Start	Finish	Predecessors	% Compl	Cc	WI	Resource Names
71	Overall L2 Rate Simulations	104 w	Mon 10/2/95	Fri 10/24/97		100%	St		PhysF144[20%],PhysU144[20%]
72	***Conceptual Design Complete***	***0 w***	***Fri 10/24/97***	***Fri 10/24/97***	***69,70,71***	***100%***	***As***		
73									
74	**Prepare Common Software Items**	**100.2 w**	**Fri 1/2/98**	**Fri 1/14/00**		**19%**	**As**		
75	Set up Library Procedures	8 w	Fri 1/2/98	Thu 2/26/98		80%	St		PhysU144[20%]
76	Unpack L2 Output into L3 Structures	14 w	Thu 10/1/98	Fri 1/22/99		25%	Fir		PhysU144[40%]
77	Code Online Verfiication Frame	30 w	Tue 6/1/99	Fri 1/14/00		0%	St		PhysU144[50%]
78									
79	**Manufacture Components**	**188 w**	**Fri 3/1/96**	**Mon 12/13/99**		**72%**	**As**		
80	**Build Processor**	**182 w**	**Fri 3/1/96**	**Thu 10/28/99**		**88%**	**As**		
81	**Initial Design**	**151.9 w**	**Fri 3/1/96**	**Mon 3/29/99**		**96%**	**As**		
82	Select Prototype Processor	52 w	Fri 3/1/96	Tue 3/18/97		100%	As	1.4	EEU144[10%],PhysU144[20%],k$[12%],k$(
83	Simulate Timing Performance	93.2 w	Fri 3/1/96	Tue 1/20/98	82SS	100%	As		PhysU144[20%]
84	Test Code Downloading	15 w	Wed 3/19/97	Wed 7/2/97	82	100%	As		PhysU144[50%]
85	Choose Monitoring Data Path	28 w	Wed 3/19/97	Fri 10/3/97	82	100%	As		PhysU144[10%]
86	Define COOR Communication	78.6 w	Mon 4/21/97	Fri 11/13/98		90%	Fir		PhysU144[20%]
87	Define Input, Output Formats	83 w	Mon 4/21/97	Thu 12/17/98		90%	As		PhysU144[10%]
88	Prepare Global TDR	40.2 w	Mon 4/21/97	Fri 2/13/98		100%	St	1.4	PhysU144[20%],k$[16%],k$c[8%]
89	***Global Processor TDR Submitted***	***0 w***	***Fri 2/13/98***	***Fri 2/13/98***	***84,88***	***100%***	***As***		
90	***Level 2 Programming and I/O Defined***	***0 w***	***Mon 3/29/99***	***Mon 3/29/99***	***86,87,154,182,183,184,218,234***	***0%***	***As***		
91	**Processor Development/Production**	**111.8 w**	**Mon 7/28/97**	**Thu 10/28/99**		**50%**	**As**		
92	Receive Prototype PCI Interfaces to Processor	30.2 w	Mon 7/28/97	Wed 3/11/98	82	100%	St	1.4	k$[7%],k$c[2%]
93	Receive and Install VME Prototype Processor	3 w	Tue 12/1/98	Mon 1/4/99	89,92	100%	St	1.4	EEU144,k$[29%],k$c[6%]
94	**Debug VME Prototype Processor**	**9 w**	**Tue 1/5/99**	**Mon 3/8/99**	**93,129FF,130FF**	**50%**	**As**	**1.4**	**EEU144,PhysU144[20%],ETF144[25%],k**
95	**Alpha Production**	**33 w**	**Tue 3/9/99**	**Thu 10/28/99**	**94**	**0%**	**As**	**1.4**	**ETF144[25%],k$[367%],k$c[102%]**
96	***Alpha Cards Received***	***0 w***	***Thu 10/28/99***	***Thu 10/28/99***	***95***	***0%***	***As***		
97	**Build Magic Bus Transciever**	**171.6 w**	**Fri 3/1/96**	**Mon 8/16/99**		**73%**	**As**		
98	Conceptual Design of Transceiver Card	90.6 w	Fri 3/1/96	Fri 12/19/97	82SS	100%	As		PhysU144[20%]
99	MBT Specification	54 w	Fri 1/2/98	Thu 2/4/99	98	77%	As	1.4	EEU144[10%],PhysU144[25%],k$[34%],k$(
100	***Finalize MBT Design***	***0 w***	***Thu 2/4/99***	***Thu 2/4/99***	***99***	***0%***	***St***		
101	Build First Prototype MBT	32 w	Tue 7/7/98	Thu 3/4/99		39%	As	1.4	EEU144,k$[65%],k$c[13%]
102	Build Second Prototype MBT	6 w	Fri 3/5/99	Thu 4/15/99	101	0%	As		
103	MBT Production	17 w	Fri 4/16/99	Mon 8/16/99	133,100,102	0%	As	1.4	k$[110%],k$c[22%]
104	***MBTs Received***	***0 w***	***Mon 8/16/99***	***Mon 8/16/99***	***103***	***0%***	***As***		
105	**Build Second Level Input Computer**	**112.8 w**	**Tue 9/2/97**	**Mon 12/13/99**		**67%**	**As**		
106	SLIC Specification and TDR	67 w	Tue 9/2/97	Tue 1/19/99		100%	St	1.4	EEU144[50%],PhysU144[25%],k$[40%],k$(
107	***Finalize SLIC Conceptual Design***	***0 w***	***Mon 2/1/99***	***Mon 2/1/99***	***106,114***	***100%***	***As***		
108	Design/Prototype SLIC Mezzanine	32 w	Thu 7/2/98	Tue 3/2/99		56%	Fir	1.4	EEU144,k$[80%],k$c[22%]
109	**Design/Prototype SLIC Motherboard**	**23 w**	**Mon 1/4/99**	**Mon 6/14/99**		**54%**	**St**		
110	**SLIC Mezzanine Production**	**12 w**	**Fri 9/17/99**	**Mon 12/13/99**	**188**	**0%**	**As**	**1.4**	**k$[240%],k$c[48%]**
111	**SLIC Motherboard Production**	**12 w**	**Fri 9/17/99**	**Mon 12/13/99**	**188**	**0%**	**As**		
112	***SLICs Received***	***0 w***	***Mon 12/13/99***	***Mon 12/13/99***	***111,110***	***0%***	***As***		
113	**Build Serial Command Link Fanout and Cable Input Cc**	**74 w**	**Fri 5/1/98**	**Tue 10/26/99**		**36%**	**As**		
114	Specificy Fanout and CIC	21 w	Fri 5/1/98	Tue 9/29/98	89	100%	St	1.4	EEU144[30%],PhysU144[25%],k$[10%],k$(
115	Design/Prototype Fanout and CIC	29 w	Wed 9/30/98	Thu 5/6/99	114	20%	St	1.4	EEU144[30%],k$[20%],k$c[5%]
116	***Prototype and design complete***	***0 w***	***Thu 5/6/99***	***Thu 5/6/99***	***115,107***	***0%***	***As***		
117	Test Fanout and CIC Prototypes	12 w	Fri 5/7/99	Mon 8/2/99	116	0%	As	1.4	EEU144[30%],k$[5%],k$c[1%]
118	Fanout/CIC Production	12 w	Tue 8/3/99	Tue 10/26/99	117	0%	As	1.4	k$[30%],k$c[6%]
119	**Build Fiber Input Converter**	**79 w**	**Fri 5/1/98**	**Thu 12/2/99**		**14%**	**As**		
120	**Specify Converter**	**12 w**	**Fri 5/1/98**	**Mon 7/27/98**	**89**	**90%**	**As**	**1.4**	**EEU144[30%],PhysU144[25%],k$[10%],k**
121	**Design,Prototype Converter**	**41 w**	**Tue 7/28/98**	**Fri 5/28/99**	**120**	**0%**	**As**	**1.4**	**EEU144[30%],k$[30%],k$c[7%]**
122	Converter Production	26 w	Mon 5/31/99	Thu 12/2/99	121	0%	As	1.4	k$[40%],k$c[8%]
123	***Level 2 Component Specs Complete***	***0 w***	***Thu 2/4/99***	***Thu 2/4/99***	***93,99,106,114,120***	***0%***	***As***		
124									
125	**Build Global Processor System**	**135.2 w**	**Mon 6/2/97**	**Thu 3/2/00**		**22%**	**As**		
126	**Develop Control Software/Prototype System**	**105.6 w**	**Thu 7/3/97**	**Mon 8/23/99**		**44%**	**As**		
127	Prepare/Test V1 Download/Script Runner	32.6 w	Thu 7/3/97	Thu 3/5/98	84	100%	St		PhysU144[50%]
128	***V1.0 Script Runner in non-VME Prototype***	***0 w***	***Thu 3/5/98***	***Thu 3/5/98***	***127***	***100%***	***St***		
129	Prepare V2 of Script Runner	40.2 w	Fri 3/6/98	Tue 12/22/98	75,128	40%	Fir		PhysU144[50%]
130	Prepare V1 of Administrative Master Code	35 w	Mon 6/15/98	Thu 3/4/99		58%	Fir		PhysU144[70%]
131	Establish Communication with L1FW	9 w	Fri 3/5/99	Thu 5/6/99	10,11,93,101	0%	As	1.4	EEU144,k$[24%],k$c[5%]
132	***M3-Install Level 2 Trigger Operating System***	***0 w***	***Thu 5/6/99***	***Thu 5/6/99***	***129,130,131***	***0%***	***As***		
133	Establish Communication with L2 FW	4 w	Fri 3/5/99	Thu 4/1/99	16,93,101	0%	As		EEU144
134	Establish Communication with L3	19 w	Sat 8/1/98	Wed 12/16/98		5%	As		PhysU144[30%]
135	Prepare V2 Administrative Master Code	6 w	Fri 3/5/99	Thu 4/15/99	101,130	0%	As	1.4	PhysU144,k$[6%],k$c[1%]
136	Prepare Final Script Runner	3 w	Fri 5/7/99	Fri 5/28/99	132	0%	As	1.4	PhysU144,k$[6%],k$c[1%]
137	Prepare Final Admin Master Code	12 w	Mon 5/31/99	Mon 8/23/99	136	0%	As	1.4	PhysU144[50%],k$[6%],k$c[1%]
138	***L2 Operating Code Complete***	***0 w***	***Mon 8/23/99***	***Mon 8/23/99***	***137***	***0%***	***As***		
139	**Develop Simulation/Monitoring System**	**135.2 w**	**Mon 6/2/97**	**Thu 3/2/00**		**2%**	**As**		
140	Specify/Establish Monitoring Data Extraction	14 w	Fri 5/7/99	Mon 8/16/99	132	0%	As		PhysU144

ID	Task Name	Duration	Start	Finish	Predecessors	% Compl	Cc	WI	Resource Names
141	Prepare Monitoring Display	26 w	Tue 8/17/99	Thu 3/2/00	140	0%	As		PhysU144
142	Develop/Simulate Trigger Algorithm	77 w	Mon 6/2/97	Wed 12/16/98		5%	Sta		PhysU144[50%]
143	***Preprocessor, Global Timing OK in Hdwe***	***0 w***	***Fri 10/15/99***	***Fri 10/15/99***	***142,325SS+28 w***	***0%***	***Sta***		
144	Tune Algorithms with Data,L3,Offline	40 w	Thu 12/17/98	Mon 10/11/99	142	0%	As		PhysU144
145	Develop Monitoring Histograms	6 w	Thu 12/17/98	Wed 2/10/99	142	0%	As		PhysU144
146	**Build/Commission Final System**	**8 w**	**Fri 10/29/99**	**Mon 1/10/00**		**0%**	**As**		
147	Assemble	4 w	Fri 10/29/99	Mon 11/29/99	95,103,138	0%	As	1.4	PhysU144,EEU144,k$[18%],k$c[4%]
148	Installation at FNAL	4 w	Tue 11/30/99	Mon 1/10/00	147,17	0%	As		PhysU144,ETF144
149	***Global Installation Complete***	***0 w***	***Mon 1/10/00***	***Mon 1/10/00***	***148***	***0%***	***Sta***		
150									
151	**Build Calorimeter Preprocessors**	**162 w**	**Wed 10/30/96**	**Mon 2/21/00**		**49%**	**As**		
152	**Design Calorimeter Processor**	**96.8 w**	**Wed 10/30/96**	**Wed 10/14/98**		**100%**	**As**		
153	Simulate Time Performance	72.8 w	Wed 10/30/96	Fri 4/24/98		100%	As		PhysU144[20%]
154	Define Input, Output	63.8 w	Wed 10/30/96	Fri 2/20/98	153SS	100%	As		PhysU144[10%]
155	Prepare TDR	24 w	Mon 4/27/98	Wed 10/14/98	88,153,154,164,166	100%	As		PhysU144[30%]
156	***Cal TDR Submitted***	***0 w***	***Wed 10/14/98***	***Wed 10/14/98***	***155***	***100%***	***As***		
157	**Build Test Calpp System**	**48 w**	**Tue 1/5/99**	**Mon 12/13/99**		**15%**	**As**		
158	**Debug and Operate Alpha Processor**	**20 w**	**Tue 1/5/99**	**Tue 5/25/99**	**93,129,155**	**35%**	**As**		**PhysU144[50%]**
159	**Assemble Test Crate**	**4 w**	**Wed 5/26/99**	**Tue 6/22/99**	**101,158**	**0%**	**As**	**1.4**	**PhysU144,EEU144,ETF144,k$[12%],k$c[**
160	Operate Test Crate	12 w	Wed 6/23/99	Thu 9/16/99	132,159	0%	As		PhysU144
161	***Global /Calpp Communication***	***0 w***	***Thu 9/16/99***	***Thu 9/16/99***	***160***	***0%***	***As***		
162	Prepare V3 Admin Master (multiple workers)	12 w	Fri 9/17/99	Mon 12/13/99	160	0%	As		PhysU144
163	**Develop L2Cal Algorithms**	**112.2 w**	**Wed 10/1/97**	**Thu 1/20/00**		**35%**	**As**		
164	Develop/Simulate Jet Alg.	43 w	Mon 12/1/97	Tue 10/13/98		100%	Sta		
165	Develop/Simulate Electron Alg.	64 w	Mon 12/1/97	Thu 3/25/99		20%	Sta		
166	Develop/Simulate Missing Et Alg.	51 w	Wed 10/1/97	Mon 10/12/98		100%	As		
167	Tune Jet Alg. With MonteCarlo	52 w	Wed 10/14/98	Tue 11/2/99	164	0%	As		
168	Tune Electron Alg. With MonteCarlo	40 w	Fri 3/26/99	Thu 1/20/00	165	0%	As		
169	Tune Missing Et Alg. With MonteCarlo	52 w	Tue 10/13/98	Mon 11/1/99	166	0%	As		
170	**Develop Cal Monitoring System**	**40 w**	**Fri 3/5/99**	**Thu 12/16/99**		**0%**	**As**		
171	Develop Monitoring Histograms	6 w	Fri 3/26/99	Thu 5/6/99	164,165,166	0%	As		PhysU144
172	Specify/Establish Monitoring Data Extraction	14 w	Fri 3/5/99	Fri 6/11/99	130	0%	As		PhysU144
173	Prepare Monitoring Display	26 w	Mon 6/14/99	Thu 12/16/99	172,171	0%	As		PhysU144
174	**Build/Commission Final System**	**8 w**	**Tue 12/14/99**	**Mon 2/21/00**		**0%**	**As**		
175	Assemble and Commission	4 w	Tue 12/14/99	Mon 1/24/00	95,103,162,33	0%	As	1.4	PhysU144,EEU144,k$[30%],k$c[6%]
176	Installation at FNAL	4 w	Tue 1/25/00	Mon 2/21/00	175	0%	As		PhysU144,ETF144
177	***L2Cal Installation Complete***	***0 w***	***Mon 2/21/00***	***Mon 2/21/00***	***176***	***0%***	***Sta***		
178									
179	**Build Muon Preprocessor**	**158.4 w**	**Sat 2/1/97**	**Mon 4/17/00**		**39%**	**As**		
180	**Design/Build Test System**	**130.4 w**	**Sat 2/1/97**	**Thu 9/16/99**		**66%**	**As**		
181	Select/Receive Test Card	17 w	Sat 2/1/97	Mon 6/2/97		100%	As	1.4	PhysU144[20%],k$[20%],k$c[4%]
182	Define Inputs	8.6 w	Tue 6/3/97	Fri 8/1/97	181	100%	As		PhysU144[10%]
183	Define Communication	15 w	Thu 7/2/98	Fri 10/16/98		100%	Sta		PhysU144[10%]
184	Define Outputs	4 w	Mon 9/29/97	Fri 10/24/97	82	100%	Sta		PhysU144[10%]
185	Prepare Muon Processor TDR	30 w	Thu 7/2/98	Tue 2/16/99	89	50%	As		PhysU144[25%]
186	***Muon TDR Submitted***	***0 w***	***Mon 6/7/99***	***Mon 6/7/99***	***107,182,183,184,185,196,209***	***0%***	***As***		
187	Extend NIU/ UIC Test Crate Design	4 w	Mon 2/1/99	Fri 2/26/99	107,114,183	0%	As	1.4	PhysU144[10%],EEU144[25%],k$[8%],k$c[
188	**Operate In NIU/UIC Shared Test Crate**	**12 w**	**Wed 6/23/99**	**Thu 9/16/99**	**108,187,159,107,109**	**0%**	**As**		**PhysU144,ETF144[25%]**
189	**Assemble Final System**	**16 w**	**Tue 12/14/99**	**Mon 4/17/00**		**0%**	**As**		
190	**Assemble Central Crate**	**12 w**	**Tue 12/14/99**	**Mon 3/20/00**	**95,103,110,118,186,188,111**	**0%**	**As**	**1.4**	**PhysU144,EEU144,k$[47%],k$c[9%]**
191	Installation at FNAL	4 w	Tue 3/21/00	Mon 4/17/00	190	0%	As		PhysU144,ETF144
192	**Assemble Forward Crate**	**12 w**	**Tue 12/14/99**	**Mon 3/20/00**	**190SS**	**0%**	**As**		**PhysU144**
193	**Installation at FNAL**	**4 w**	**Tue 3/21/00**	**Mon 4/17/00**	**192**	**0%**	**As**	**1.4**	**PhysU144,ETF144**
194	***L2 Muon Installation Complete***	***0 w***	***Mon 4/17/00***	***Mon 4/17/00***	***193***	***0%***	***As***		
195	**Develop Processor Algorithm**	**138.4 w**	**Mon 2/3/97**	**Thu 11/11/99**		**63%**	**As**		
196	Draft Version of Central Algorithm	28 w	Mon 2/3/97	Tue 8/19/97	181SS	100%	As		PhysU144
197	***Receive Evaluation DSP***	***0 w***	***Fri 1/15/99***	***Fri 1/15/99***		***0%***	***Sta***		
198	Complete Central Algorithm on Digital Signal Proc.	4 w	Fri 1/15/99	Thu 2/11/99	197,196	0%	As		PhysU144
199	Draft Forward Algorithm	12 w	Mon 6/1/98	Mon 8/24/98	196	100%	As		PhysU144
200	Complete Forward Algorithm	4 w	Fri 1/15/99	Thu 2/11/99	199,197	0%	As		PhysU144
201	Develop Alpha Algorithm	8 w	Fri 4/16/99	Fri 6/11/99	199,135	0%	As		
202	Assemble Full Algorithm	8 w	Fri 9/17/99	Thu 11/11/99	198,188,201,200	0%	As		PhysU144
203	**Build Simulator**	**60.8 w**	**Fri 10/30/98**	**Fri 2/4/00**		**1%**	**As**		
204	Design L1 Muon Simulator	6 w	Fri 10/30/98	Mon 12/14/98		10%	As		
205	Implement L1 Muon Simulator	4 w	Mon 1/18/99	Fri 2/12/99	204,319	0%	As		
206	Integrate Central L2 Alg into Framework	4 w	Mon 1/18/99	Fri 2/12/99	196,319	0%	As		
207	Study Efficiency of Central Trigger	8 w	Mon 2/15/99	Fri 4/9/99	206	0%	As		PhysU144
208	Integrate Forward L2 Algorithm into Framework	4 w	Mon 1/18/99	Fri 2/12/99	199,319	0%	As		PhysU144
209	Study Full Efficiencies	8 w	Mon 4/12/99	Mon 6/7/99	207,208,205	0%	As		PhysU144
210	Tune Simulator on Online Implementation	26 w	Tue 6/8/99	Fri 12/10/99	209	0%	As		PhysU144

ID	Task Name	Duration	Start	Finish	Predecessors	% Compl	Cc	WI	Resource Names
211	Simulate Offline Verification	4 w	Mon 12/13/99	Fri 1/21/00	210	0%	As		
212	Develop Online Monitoring Histograms	3 w	Mon 12/13/99	Fri 1/14/00	210	0%	As		PhysU144
213	Develop Online Verification	2 w	Mon 1/24/00	Fri 2/4/00	77,211	0%	As		PhysU144
214									
215	**Build CTT Preprocessor**	**145 w**	**Sun 6/1/97**	**Wed 5/10/00**		**55%**	**As**		
216	**Design Preprocessor**	**115.2 w**	**Sun 6/1/97**	**Tue 9/28/99**		**72%**	**As**		
217	Develop and Time Trigger Algorithm	81 w	Sun 6/1/97	Wed 1/27/99		80%	Sta	1.4	PhysU144[25%],k$[3%]
218	Establish Specifications	23 w	Thu 7/2/98	Tue 12/15/98		100%	Sta	1.4	PhysU144[25%],EEU144[50%],k$[6%],k$c[
219	Establish Crate Content	4 w	Mon 10/19/98	Fri 11/13/98	218	100%	As		PhysU144[50%]
220	***Submit CTT TDR***	***0 w***	***Wed 1/27/99***	***Wed 1/27/99***	***217,219***	***0%***	***As***		
221	Operate Alpha	20 w	Fri 5/7/99	Tue 9/28/99	132,220	0%	As		PhysU144[50%]
222	**Build Final System**	**16 w**	**Fri 12/3/99**	**Thu 4/6/00**		**0%**	**As**		
223	Assemble Crate	12 w	Fri 12/3/99	Thu 3/9/00	95,103,221,122	0%	As	1.4	PhysU144[50%],EEU144[50%],k$[24%],k$(
224	Installation at FNAL	4 w	Fri 3/10/00	Thu 4/6/00	138,223	0%	As		PhysU144,ETF144
225	***L2 CTT Installation Complete***	***0 w***	***Thu 4/6/00***	***Thu 4/6/00***	***224***	***0%***	***As***		
226	**Build Algorithm/Simulator**	**145 w**	**Sun 6/1/97**	**Wed 5/10/00**		**47%**	**As**		
227	Integrate Algorithm in Simulator	101 w	Sun 6/1/97	Thu 6/17/99		70%	As		PhysU144[20%]
228	Tune Algorithm on Physics, L3, Offline	44 w	Fri 6/18/99	Wed 5/10/00	227	0%	As		PhysU144[60%]
229	Incorporate in Global Algorithms	4 w	Fri 6/18/99	Fri 7/16/99	227	0%	As		PhysU144
230									
231	**Build PS Preprocessor**	**145 w**	**Sun 6/1/97**	**Wed 5/10/00**		**33%**	**As**		
232	**Design Preprocessor**	**121.5 w**	**Sun 6/1/97**	**Thu 11/11/99**		**63%**	**As**		
233	Develop and Time Trigger Algorithm	81 w	Sun 6/1/97	Wed 1/27/99		100%	As	1.4	PhysU144[25%],k$[3%]
234	**Establish Specifications**	**29.5 w**	**Mon 8/17/98**	**Mon 3/29/99**	**233**	**29%**	**As**	**1.4**	**PhysU144[25%],EEU144[25%],k$[3%]**
235	Establish Crate Content	12 w	Mon 3/29/99	Tue 6/22/99	234	0%	As		PhysU144[50%]
236	***Submit PS TDR***	***0 w***	***Tue 6/22/99***	***Tue 6/22/99***	***235***	***0%***	***As***		
237	Operate Alpha	20 w	Tue 6/22/99	Thu 11/11/99	132,236	0%	As		PhysU144[50%]
238	**Build Final System**	**16 w**	**Fri 12/3/99**	**Thu 4/6/00**		**0%**	**As**		
239	Assemble Crate	12 w	Fri 12/3/99	Thu 3/9/00	95,103,237,122	0%	As	1.4	PhysU144[50%],EEU144[50%],k$[30%],k$(
240	Installation at FNAL	4 w	Fri 3/10/00	Thu 4/6/00	138,239	0%	As		PhysU144,ETF144
241	***L2 PS Installation Complete***	***0 w***	***Thu 4/6/00***	***Thu 4/6/00***	***240***	***0%***	***As***		
242	**Build Algorithm/Simulator**	**145 w**	**Sun 6/1/97**	**Wed 5/10/00**		**8%**	**As**		
243	Integrate Algorithm in Simulator	101 w	Sun 6/1/97	Thu 6/17/99		12%	As		PhysU144[20%]
244	Tune Algorithm on Physics, L3, Offline	44 w	Fri 6/18/99	Wed 5/10/00	243	0%	As		PhysU144[60%]
245	Incorporate in Global Algorithms	4 w	Fri 6/18/99	Fri 7/16/99	243	0%	As		PhysU144
246									
247	**Integrate L2 System**	**69.8 w**	**Tue 2/16/99**	**Mon 7/10/00**		**0%**	**As**		
248	***Level 2 Review***	***0 w***	***Tue 2/16/99***	***Tue 2/16/99***	***89,156,185,220***	***0%***	***Sta***		
249	Commission Global/Calpp Combination	6 w	Tue 2/22/00	Mon 4/3/00	148,176,173	0%	As		PhysU144[80%],EEU144[40%]
250	**Commission L2 Muon**	**6 w**	**Tue 4/18/00**	**Mon 5/29/00**	**194,202**	**0%**	**As**		**PhysU144[200%]**
251	***M3-Trigger Level 2 Commissioned***	***0 w***	***Mon 5/29/00***	***Mon 5/29/00***	***249,250***	***0%***	***As***		
252	**Commission L2 CTT,FPS**	**6 w**	**Tue 5/30/00**	**Mon 7/10/00**	**225,241,250**	**0%**	**As**		**PhysU144[200%]**
253									
254									
255	**Level 3 Trigger**	**197.2 w**	**Mon 6/3/96**	**Tue 5/30/00**		**46%**	**As**		
256	**Purchase Components**	**184.8 w**	**Mon 6/3/96**	**Fri 3/3/00**		**44%**	**As**		
257	Upgrade 40 Extended VBD Cards	122.2 w	Mon 6/3/96	Fri 11/13/98		80%	Fir	1.4	k$[14%]
258	Upgrade 60 Regular VBD Cards	70.8 w	Fri 7/18/97	Thu 12/31/98		49%	Fir	1.4	k$[14%]
259	Purchase Readout Control	32 w	Thu 10/1/98	Mon 5/31/99		0%	Sta	1.4	k$[229%],k$c[46%]
260	Purchase High Speed Output	24 w	Tue 12/1/98	Tue 6/1/99		0%	Sta	1.4	k$[15%],k$c[2%]
261	Purchase Commissioning Processors	50 w	Mon 2/1/99	Fri 2/4/00		0%	Sta	1.4	k$[130%],k$c[26%]
262	Purchase Run II Processors	4 w	Mon 2/7/00	Fri 3/3/00	261	0%	Sta	1.4	k$[130%],k$c[26%]
263	***L3 Acquisition Complete***	***0 w***	***Fri 3/3/00***	***Fri 3/3/00***	***258,259,260,262,257***	***0%***	***As***		
264	**Develop/Install Readout Control**	**190.8 w**	**Mon 6/3/96**	**Fri 4/14/00**		**65%**	**As**		
265	**Data Path Operation with Old System**	**45.2 w**	**Mon 6/3/96**	**Wed 4/30/97**		**100%**	**As**		
266	With New MCH Position	16 w	Mon 6/3/96	Tue 9/24/96	257SS	100%	As		PhysU145[50%]
267	With Upgraded VME Readout Boards	20 w	Mon 12/2/96	Wed 4/30/97		100%	Sta		PhysU145[50%]
268	**Readout Control R&D**	**167.4 w**	**Fri 11/15/96**	**Fri 4/14/00**		**62%**	**As**		
269	Initial Design	50 w	Fri 11/15/96	Tue 11/18/97		100%	Sta	1.4	k$[70%],k$c[5%]
270	Simulation	124 w	Fri 11/15/96	Thu 5/27/99	269SS	75%	As		PhysU145[50%]
271	Develop First Data Path Prototype(VBD,MPM)	78 w	Fri 5/16/97	Wed 12/9/98	269SS+24 w,284	74%	Fir		PhysU145[50%]
272	First System Test at D0 (VBD,MPM,NT)	14 w	Wed 11/19/97	Wed 3/11/98	269	100%	As		
273	***M3-Trigger Level 3 System Test Complete***	***0 w***	***Wed 3/11/98***	***Wed 3/11/98***	***272***	***100%***	***As***		
274	Final Design	39 w	Thu 3/12/98	Wed 12/16/98	273	80%	As	1.4	
275	***M3-Trigger Level 3 TDR Submitted***	***0 w***	***Wed 12/16/98***	***Wed 12/16/98***	***274***	***0%***	***As***		
276	Design Hardware Components	45 w	Thu 12/17/98	Mon 11/15/99	275	0%	As	1.4	k$[72%],k$c[5%]
277	Develop Second Data Path Prototype	8 w	Thu 12/17/98	Wed 2/24/99	271,275	0%	As		PhysU145[50%]
278	First Hardware System Test at D0	20 w	Thu 2/25/99	Fri 7/16/99	277	0%	As		PhysU145[50%],EEF145[10%]
279	Second Hardware Test	13 w	Mon 7/19/99	Mon 10/18/99	278	0%	As		
280	Install Full System	6 w	Mon 3/6/00	Fri 4/14/00	279,276,263,287	0%	As		PhysU145[50%],EEF145[50%]

ID	Task Name	Duration	Start	Finish	Predecessors	% Compl	Cc	WI	Resource Names
281	***M3-L3 Operational***	***0 w***	***Fri 4/14/00***	***Fri 4/14/00***	***280***	***0%***	***As***		
282	**Develop Operation Software**	**181 w**	**Mon 6/3/96**	**Mon 2/7/00**		**53%**	**As**		
283	Support Continuous Data Collection at D0	172 w	Mon 6/3/96	Thu 11/18/99	257SS	56%	As		PhysU145[50%]
284	Establish New Protocol	24 w	Mon 6/3/96	Tue 11/19/96	257SS	100%	As		PhysU145[50%]
285	Develop L3/DAQ Framework	148 w	Mon 6/3/96	Tue 6/1/99	257SS	80%	As		PhysU145[50%]
286	Develop Monitoring/Diagnostic Control	181 w	Mon 6/3/96	Mon 2/7/00	257SS	20%	As		PhysU145[50%]
287	***M3-L3 Online Software Complete***	***0 w***	***Thu 11/18/99***	***Thu 11/18/99***	***283,284,285***	***0%***	***As***		
288									
289	**Level 3 Filtering Software**	**164.6 w**	**Mon 2/3/97**	**Tue 5/30/00**		**21%**	**As**		
290	Develop L3 Filtering Framework	36 w	Tue 6/3/97	Thu 2/26/98		70%	Sta		PhysU145[125%]
291	Development of L3 Data Base (Constants,Trigger)	38 w	Fri 10/2/98	Wed 7/14/99		0%	Sta		
292	**Platform Support for Code**	**34 w**	**Mon 6/1/98**	**Thu 2/11/99**		**44%**	**As**		
293	NT Release Procedures	30 w	Mon 6/1/98	Thu 1/14/99		50%	Sta		PhysU145[40%]
294	Port Code to NT	4 w	Fri 1/15/99	Thu 2/11/99	293	0%	As		PhysU145[10%]
295	**Geometry/Constant**	**8 w**	**Wed 11/18/98**	**Thu 1/28/99**		**0%**	**As**		**PhysU145[25%],PhysF145[25%]**
296	Define Download Method	8 w	Wed 11/18/98	Thu 1/28/99		0%	Sta		
297	**Unpacking Issues**	**107.8 w**	**Mon 8/18/97**	**Thu 10/21/99**		**30%**	**As**		**PhysU145**
298	Unpack Base Classes	68 w	Mon 8/18/97	Tue 1/12/99		50%	Sta		
299	***L2 Inputs Into L3 Defined***	***0 w***	***Tue 1/12/99***	***Tue 1/12/99***	***87,298***	***0%***	***As***		
300	Availability of MC Raw Data	12 w	Tue 12/1/98	Mon 3/8/99		0%	Sta		
301	Implement Subdector Unpacking	32 w	Tue 3/9/99	Thu 10/21/99	298,300,290	0%	As		
302	**Develop Filter Tools**	**156 w**	**Mon 2/3/97**	**Thu 3/30/00**		**13%**	**As**		**PhysU145[800%]**
303	Tool Parameter Format	21 w	Mon 2/3/97	Mon 6/30/97		100%	As		
304	***Tool Parameter Format Defined***	***0 w***	***Mon 6/30/97***	***Mon 6/30/97***	***303***	***100%***	***Sta***		
305	Develop algorithms	26 w	Wed 11/18/98	Fri 6/4/99	304	5%	Sta		
306	Implement L3 Algorithms	40 w	Mon 6/7/99	Thu 3/30/00	305,293,290	0%	As		
307	Optimize, test, tune parameters	40 w	Mon 6/7/99	Thu 3/30/00	305	0%	As		
308	Code Maintenance	40 w	Mon 6/7/99	Thu 3/30/00	305	0%	As		
309	**Provide Executables**	**44.6 w**	**Wed 6/2/99**	**Thu 4/27/00**		**0%**	**As**		**PhysU145[150%]**
310	First Downloadable Executable Available	6 w	Wed 6/2/99	Wed 7/14/99	285,290,294	0%	As		
311	***M3-First Downloadable Executable Available***	***0 w***	***Wed 7/14/99***	***Wed 7/14/99***	***310***	***0%***	***As***		
312	Cosmic Ray Executable Available	12 w	Thu 7/15/99	Thu 10/7/99	310,291	0%	As		
313	Runtime Executable Available	4 w	Fri 3/31/00	Thu 4/27/00	312,306,301	0%	As		
314	**Hit finding/Event size reduction**	**45 w**	**Thu 7/1/99**	**Tue 5/30/00**		**0%**	**Sta**		**PhysU145[25%]**
315									
316	**L1/L2/L3 Simulator**	**47.2 w**	**Fri 10/2/98**	**Fri 9/17/99**		**10%**	**As**		
317	Development of Trigparse Replacement	23 w	Fri 10/2/98	Mon 3/29/99		0%	Sta		PhysU145[25%]
318	Develop COOR_SIM	17 w	Mon 11/16/98	Tue 3/30/99	86	0%	As		PhysU145[25%]
319	Design Simulation Framework	11 w	Thu 10/15/98	Fri 1/15/99		50%	Sta		PhysU145
320	Design and Implement Data Chunks	11 w	Thu 10/15/98	Fri 1/15/99	319SS	50%	Sta		PhysU145[200%]
321	***Simulation Shells with Data Chunks Implemented***	***0 w***	***Fri 1/15/99***	***Fri 1/15/99***	***320,319***	***0%***	***As***		
322	Finalize Ntuple, Chunks, and Monte Carlo Inputs	9 w	Mon 1/18/99	Fri 3/19/99	321	0%	As		PhysU145[200%]
323	First Version Simulation	9 w	Mon 1/18/99	Fri 3/19/99	322SS	0%	As		PhysU145[200%]
324	***Individual Package and Shell Prototypes Complete***	***0 w***	***Fri 3/19/99***	***Fri 3/19/99***	***323,322***	***0%***	***As***		
325	Integrate L1 and L2 Simulation Prototypes with I/O	12 w	Wed 3/31/99	Wed 6/23/99	317,318,324	0%	As		PhysU145
326	***Integrated L1 and L2 Simulation Prototype Complete***	***0 w***	***Wed 6/23/99***	***Wed 6/23/99***	***325***	***0%***	***As***		
327	Finalize L1 and L2 Simulations	12 w	Thu 6/24/99	Fri 9/17/99	326	0%	As		PhysU145
328	Integrate L3 Algorithms	4 w	Fri 8/20/99	Fri 9/17/99	326SS+8 w	0%	As		PhysU145
329	***M3-Full Simulator Available***	***0 w***	***Fri 9/17/99***	***Fri 9/17/99***	***328,327***	***0%***	***As***		