ADF-2 PAL VME Invalid Cycle Timing Diagram

PAL_BX_CLOCK
VME_DS1_B
RCVD_DS1
VME_LTCH_CLOCK
VME_ADDR
OCB_ADDR
VME_AM
LTCHD_AM
VME_WRITE_B
LTCHD_WRITE_B
OCB_DIRECTION
OCB_CHIP_SELECT_B
OCB_WRITE_STROBE_B
DAC_SERIAL_DATA_CLOCK
CNFG_CLOCK
DATA_BUF_ENB_B
DATA_BUF_DIR
OCB_DATA
VME_DATA
DTACK

1. IDLE
2. LATCH_1
3. LATCH_2
4. IDLE

* * * This signal represents the assertion of 1 pulse on write clock signals OCB_WRITE_STROBE_B and DAC_SERIAL_DATA_CLOCK are active on the falling edge and CNFG_CLOCK is active on the rising edge.

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