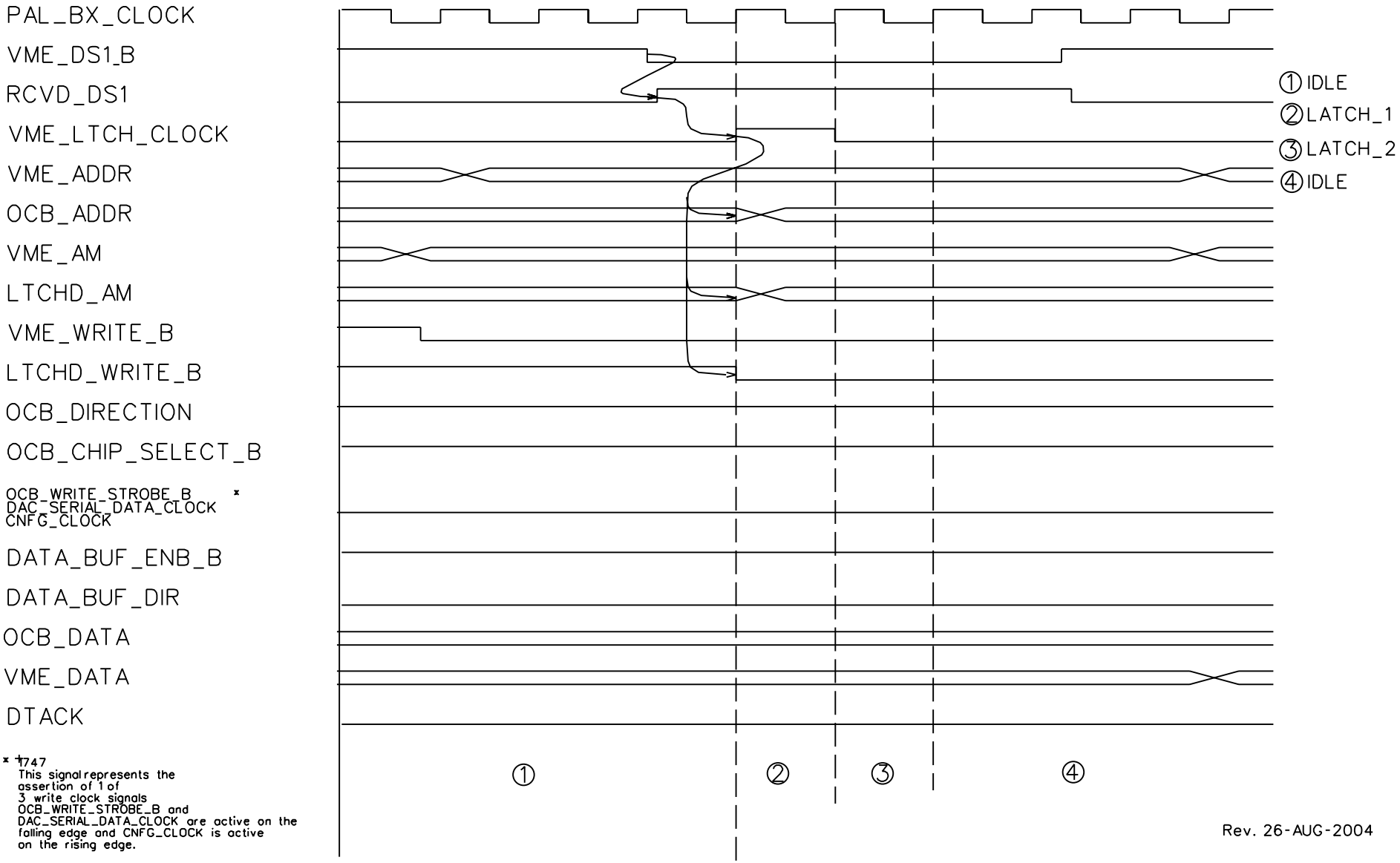
ADF-2 PAL VME Invalid Cycle Timing Diagram



* 1747
This signal represents the assertion of 1 of 3 write clock signals OCB_WRITE_STROBE_B and DAC_SERIAL_DATA_CLOCK are active on the falling edge and CNFG_CLOCK is active on the rising edge.

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