ADF-2  Board Control PAL  Board Level Control

Board Level
Control Registers

U1071

Signals from Maestro
ADF-2 to SLD

U1071

DRV_CRATE
TO_SCLD_0

CRATE_TO_SCLD_0_P

CRATE_TO_SCLD_0_N

DRV_CRATE
TO_SCLD_1

CRATE_TO_SCLD_1_P

CRATE_TO_SCLD_1_N

U1031

INV

OC

DRV_CRATE_STATUS(0:3)

CRATE_STATUS_B(0:3)

FPGA Status Signals
FPGA_0_STATUS(0:3)
FPGA_1_STATUS(0:3)

Crate Status Signals on the
VME Backplane

Inverted in the
Receiving I/O Blobk

Read-Write
Registers

Board Control
PAL
U1101

Read Only
Registers

Board Level
Status Registers

Revised as of
11-JUNE-2004

Channel Link
SER_DESKEW_B
SER_DC_BALANCE
Trigger Tower ADC's
ADC_ENABLE
Pedestal DAC's
DATA_TO_FIRST_DAC_INPUT
DAC_SERIAL_DATA_CLOCK
DAC_CHIP_SELECT_B
Internal Control Signals
ENABLE_FPGA_CONFIGURATION
ENABLE_LOADING_DACS

On Card Bus

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On Card Bus