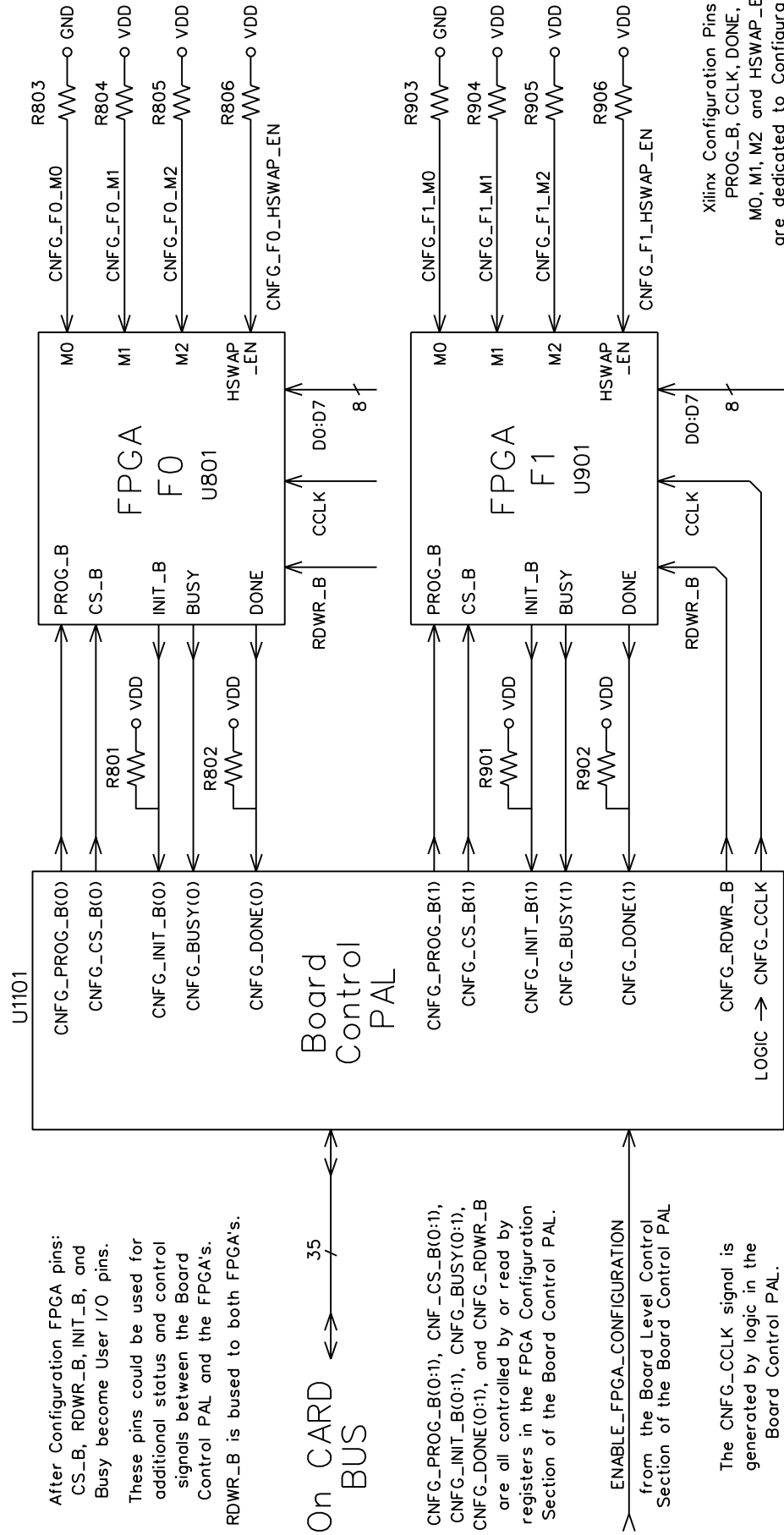


ADF-2 Board Control PAL FPGA Configuration



After Configuration FPGA pins: CS_B, RDWR_B, INIT_B, and Busy become User I/O pins.

These pins could be used for additional status and control signals between the Board Control PAL and the FPGA's.

RDWR_B is used to both FPGA's.

On CARD BUS

CNFG_PROG_B(0:1), CNF_CS_B(0:1), CNFG_INIT_B(0:1), CNFG_BUSY(0:1), CNFG_DONE(0:1), and CNFG_RDWR_B are all controlled by or read by registers in the FPGA Configuration Section of the Board Control PAL.

ENABLE_FPGA_CONFIGURATION from the Board Level Control Section of the Board Control PAL

The CNFG_CCLK signal is generated by logic in the Board Control PAL.

OCB_DATA(0:7) ← Configuration Data is carried on OCB_DATA(0:7) of the On Card Bus

Xilinx Configuration Pins
 PROG_B, CCLK, DONE,
 M0, M1, M2 and HSWAP_EN
 are dedicated to Configuration
 and are not available after
 Configuration for User I/O.