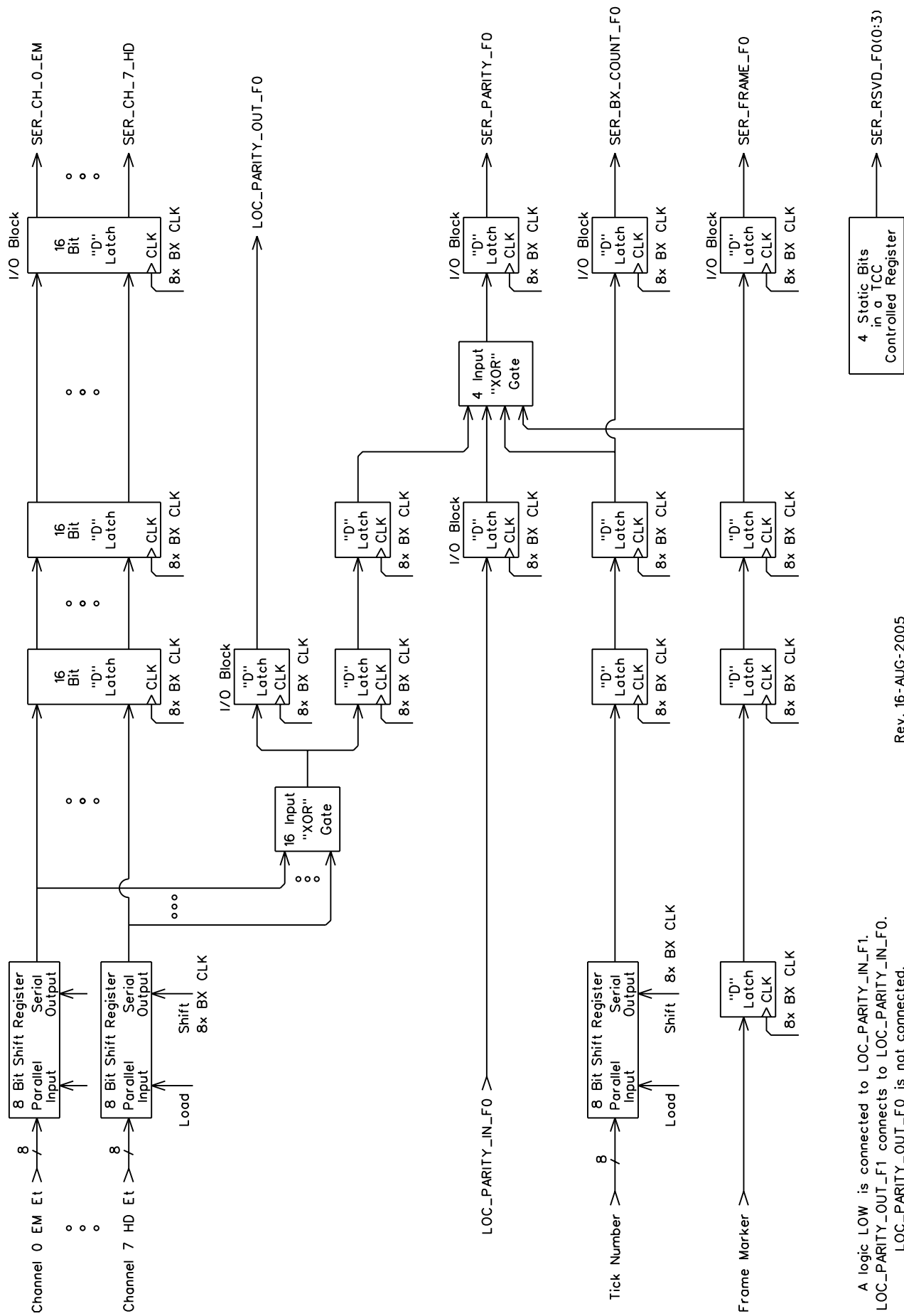


Data Path FPGA F0 Output to Channel Link



A logic LOW is connected to LOC_PARITY_IN_F1.
 LOC_PARITY_OUT_F1 connects to LOC_PARITY_IN_F0.
 LOC_PARITY_OUT_F0 is not connected.