SCLD Control Signal Distribution

Receive from SCLD then Distribution over Backplane and on Card

The Jumpers to Drive the VME-64X Reserved Bus Lines are only Installed on the ADF-2 that Connects with the SCLD.

LVDS to Open Collector TTL Drivers

SCLD_BX_CLOCK

Connections to the VME-64X Reserved Bus Lines

U1021, U1031
U1051, U1052

BX Clock Receiver LVDS to 3.3V CMOS

U1052

Narrow Band 8x PLL

U1071
Low Skew Fan Out

BX_CLOCK to the Board Control PAL

FIRST_X8_EDGE
To the FPGA's

BX_X8_CLOCK

BX_X8_CLOCK
Channel Link Chips

The BX_X8_CLOCK signals are carried on low skew point to point traces.

The Control Signals: RCVD_BE&END_TURN, RCVD_LIVE_BX,
RCVD_SAVE_MONIT_DATA, RCVD_SCL_INIT, and RCVD_SPARE
connect to both FPGA's in parallel. These signals are latched at the FPGA Input I/O Block by the First BX_X8_CLK Edge of the Tick.

Receive SCLD and Drive Backplane

Receive from Backplane and Distribute on ADF-2 Card

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