SCLD to ADF-2 Timing and Control Signals

Signals from the SCL Receiver Going into the SCLD's FPGA

CLK_53

CLK_7

FIRST_PERIOD
BEAM_PERIOD
INIT_SECTION

Output Register Clock Enable Signals Internal to the SCLD's FPGA

BX_CLOCK Output Register Clock Enable

Control Signals Output Register Clock Enable

Signals from the SCLD's FPGA Outputs Going to the ADF-2's

BX_CLOCK from SCLD to ADF-2's

Control Signals from SCLD to ADF-2's

Rev. 1-JULY-2004