DØ L1CAL Trigger ADF PRR

introduction
personnel
costs
contingency

1. if the design and prototype technical performance meet the requirements of the baseline design. (Dan and Philippe)

2. if the resources are adequate to produce the ADF boards on schedule and on budget. As part of this, you are asked to determine if the technical, financial, and personnel contingency are adequate to provide reasonable assurance of successful project completion. If additional money could be used to speed up the production or testing of the boards, please comment on this. (Dan, Philippe, and Chip)

Specifically, items we would like to cover are:

Hardware: Review the design and determine if it meets specifications. (Dan)

What tests have been done to prove it meets specifications and what changes, if any, are needed from existing to production modules? (Philippe and Jorge)

Check the grounding and shielding plans, cooling needs and plans, and power supplies, as well as the adequacy of spare boards and parts. (Dan)

Comment on the test stand planning and needs. (Philippe)

Interfaces: (to SCL, TAB, TCC, …) hardware, designs and tests or plans for tests. (Dan)

Personnel: for production and testing. (Chip)

Timeline: for production and testing. (Dan and Philippe)

Engineers:	**Dan Edmunds, Philippe Laurens, Jason Biel**
Grad Students:	**Jorge Benitez (here), Rahmi Unalan (FNAL)**
Faculty:	**Maris Abolins, Chip Brock, Harry Weerts (FNAL)**
Technical:	**mechanical: Mike Nila**
	programming: Tom Rockwell

Budgeting:

- All engineers are full-time on the project, Dan at a department-subsidized rate.
- Nila is budgeted at 50% to start after production - available for testing
- Rockwell is budgeted at 25% to start after production - available for testing/coding
  both are shared HEP personnel
- Invoicing of charge-back and salaries is behind

PRR Charge: are "…financial, and personnel contingency [are] adequate"?

- We have no need of contingency for salary
  indeed, since production comes late…Nila/Rockwell budgeted salaries were not used
- We have no need of technical contingency

Materials

- Roughly, one design was costed and approved and a different design was built:

All production parts have been purchased and total $ is under the original

Protoype costs were just over the original estimate

So,the result is that parts/crates/prototype/production costs…roughly even out

We can go over more numbers if needed later

item	estimated ($k)	actual ($k)	comments	status
parts	147.24	135.8	2 fewer fpga's	in hand
crates	64.98	40.63	4 plus spare supplies rather than 5 full	in hand at FNAL
prototype	17.53	13.1	ADCO cheaper	done
production	33.09	33.39		quote
total	262.84	222.92		

PRR Charge: "…if the resources are adequate to produce the ADF boards on schedule and on budget."

Yes.

Production

- We are dealing with ADCO in Detroit now - they are ready to go with 10 day turn-around

  PRR Charge: "If additional money could be used to speed up the production or testing of the boards, please comment on this." Good idea

  we've already done it: already let the PO for raw board production

  - *saved 2 weeks at minimal risk ($10k)*
  - *delivery expected next week*
  - *then they will hold for our approval to assemble*

  So, expect first production boards inside of a couple of weeks

Testing

- Good news: 6 prototype boards ≡ production boards (soon, 10)
- So, "integration testing" could begin very soon using prototype boards

  December schedule for Director's Review didn't show this possibility, right?

  Testing schedule could be broken from production schedule now as independent track

  Like all things: seeing the first production board will allow for an accurate prediction of MSU-based testing
- but, if first boards arrive ~3/1…

  Current schedule calls for 18 weeks MSU bench testing => completed delivery, by 7/1

  18 weeks is 1 banker's day per board…which is likely extreme by some factor >2

  But, let's see the first production boards before changing anything

schedule for the day - any modifications requested?

0930-0945....

- Chip: Introductions, overall sketch of schedule, issues of budget, contingency (just finished)

0945-1030

- Dan: ADF card design, specifications, firmware topics

1030-1045 coffee

1045-1115

- Philippe, Jorge: control software, tests done, sketch of production testing planning

1115-1200

- tour, questions

1200-1300

- working lunch in 3208

1300-1430

- committee meets, drafts bulleted comments (projector available)...MSU people on-call

1430-1500

- closeout discussion with engineers/committee

adjourn no later than 1500