# ADF-2 Production Readiness Review

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The ADF-2 circuit board is part of the new Run IIB Level 1 Calorimeter Trigger. The purpose of this note is to provide the ADF-2 Production Readiness Review Committee with technical information about the design, firmware, and use of the ADF-2 card.

Outline of this note

- History of the ADF-2 project
- Block diagram and the 4 main sections of the ADF-2 card
  - Board Control
  - Analog ADC
  - Channel Link Output
  - SCLD Control
- Power Supplies and Safety
- BLS Analog Input Signals
- Firmware and Et Filtering

As a quick introduction to the ADF project it is useful to have a look at where the time was spent during the last year while MSU was working on the ADF-2 card. The purpose is to understand which jobs take what fraction of the time and how to do this kink of work better on future projects.

- Oct-2003 MSU took on the "production and testing" of the ADF card. The intent was that MSU would be supplied with a design that was "fully debugged and tested and ready for production".
- 22-Dec-2003 Receive an ADF card and 50 pages of schematics and a pile of vhdl.
- 1-Jan-2004 : 14-MAR-2004 Learn about ADF, discover a number of problems including fatal problems.
- 15-MAR-2004 : 14-JUN-2004 Study what must change and what ideas can be saved. Work carefully to control how far out from the ADF card itself the changes will spread. Don't change things just because of personnel design preference. Do the bulk of the ADF-2 design entry.
- 15-JUN-2004 : 6-AUG-2004 Work on "geometries" and the board layout (component placement). The intent is to make it an easy board for error free manufacturing. The design is made 100 percent metric. Finish the design entry.
- 7-AUG-2004 : 4-NOV-2004 Actual pcb routing, talk with assembly vendors, make draft assembly data for bids and write the bid documents.
- 5-NOV-2004 : 22-NOV-2004 "Cool Down", Design rule checks, clean up, tune the silk, prepare the final artwork and assembly data.
- 23-NOV-2004 Release for production of 10 cards.
- 4-JAN-2005 Receive the first 10 cards.
- 5-JAN-2005 until now 5 weeks of testing on 6 of the first 10 cards.

An overall block diagram of the ADF 2 card is presented in the drawing located in the ADF-2 web documents at /drawings/adf-2-card-block-diagram.pdf

The ADF-2 card can be viewed from its 4 major sections which are: Board Control, Analog ADC, Channel Link Outputs, and Timing and Control from SCLD.

The first section to look at is the Board Control. The Board Control section itself is divided into 3 sub-sections: VME Interface, Board Level Control and Status, and FPGA Configuration.

VME Interface

- VME to a defined On Card Bus /general/on-card-bus-description.txt
- Defined VME Map /general/adf-2-vme-addressing.txt
- By design it is a simple VME A24 only D16 only Slave only interface.
- By design keep all digital noise off of P2.
- VME is used only for cold starting the system, slow control, monitoring, and testing.
- /drawings/board-control-pal-vme-interface.pdf

Board Level Control and Status

- Control and Status of the "board level" resources, e.g. set DC Balanced mode of Channel Link transmission.
- Provide extra communications paths if needed
- /drawings/board-control-pal-board-level-control.pdf

FPGA Configuration

- Provide independent or simultaneous Configuration over VME of the 2 Data Path FPGAs on each ADF-2 card.
- Provide full and independent monitoring of the Configuration process.
- Provide protection against accidental loss of FPGA configuration.
- /drawings/board-control-pal-fpga-configuration.pdf

Analog ADC Section

- Provide the correct termination for the Pleated Foil cables.
- Provide at least 1/4 GeV Et LSBit resolution
- Provide an Analog Dynamic Range that spans a "Calibration Range" in eta.
- Provide noise and crosstalk levels below that of the inherent noise on the BLS signals.
- Provide "Pedestal Control" that is absolutely stable and that gives a way of checking the bulk of the analog signal path at DC speed.
- Keep high frequency noise out of the ADC's.
- Keep the Analog ADC Section quiet digitally.
- All analog components are run right down the middle of their operating range - nothing is pinned up against a common mode limit or something like that.
- Provide a rational manufacturable layout.
- /drawings/adf-2-differential-amp.pdf
- /drawings/adf-2-ped-dacs.pdf
- /drawings/adf-2-adc-10-bit.pdf

Channel Link Output Section

- The ADF-2 Channel Link output is is the connection to the "digital section" of the L1 Cal Trig i.e. the TAB GAB cards.
- Channel Link is the only high speed output data from the ADF-2 card.
- From each ADF-2 card its Channel Link Output is used to carry Filtered Et data for 16 EM and 16 HD channels every 132 nsec.
- The Filtered Et data is 8 bit with 1/4 GeV Et per LSBit offset so that zero energy deposited in the Calorimeter results in a code of 08 hex being transfered to the TAB.
- There are 8 Channel Link Transfers per Frame of ADF to TAB data.
- Each ADF to TAB Frame contains the BX Number of the Tevatron BX that caused the energy deposit in the Calorimeter that is being reported in this ADF to TAB Frame.
- All cards in all 4 ADF crates are synchronous with each other, they begin ADF to TAB Frames within a few nsec of each other and in a given Frame all channels are carrying data from the same Tevatron BX.
- Each Channel Link Transfer contains a Parity Bit.
- A Channel Link Transfer that is the beginning of an ADF to TAB Frame is marked with an asserted Frame Bit.
- ADF-2 Channel Link Output can run continuously and the TAB can "lock on" at any point.

SCLD Timing and Control

- A central timing distributor card, the SCLD, holds an SCL Receiver and sends timing and control signals in a very simple way to each ADF-2 Crate.
- In each ADF-2 Crate the timing and control signals from the SCLD are received by the "Maestro" ADF-2 card and then sent out over Reserved Bused VME-64X open collector backplane lines.
- The Maestro ADF card provides no other special functions. Any ADF-2 card can serve as the Maestro by having some jumpers installed.
- All 20 ADF-2 cards in the crate receive their timing and control signals from the Reserved Bused VME-64X open collector backplane lines mentioned above.
- The control signals received from the backplane are "slow" and change only once per 132 nsec maximum. These signals travel the whole way from the SCLD to the Data Path FPGA before being re aligned with the clock.
- The timing signal from the backplane is a BX rate clock, 7.59 MHz. It is carried differentially on the backplane. It is received differentially and multiplied by X8 by a narrow band PLL.
- The SCLD to ADF Crate signal path contains spare lines. We also have lines that can send signals from the ADF Crate to the SCLD card (from where such a signal can be distributed to all ADF-2 cards.
- /drawings/scld-control-signal-distribution.pdf
- /drawings/clock-bx-x8-generation.pdf

Power Supplies and Safety

The intent of this section is to give the committee enough information about this aspect the ADF-2 card so that they can estimate whether or not the ADF-2 is likely to obtain a safety operating permit.

- All 4 supplies entering the ADF-2 card are fused at the point of entry.
- I know of no special design problems that should be an issue with getting the ADF-2 card through a safety review.
- The ADF-2 card operate in a high quality Wiener commercial crate.
- To provide the analog power supplies of the differential amplifiers in the Analog ADC Section the crate manufacturer has replaced the VME +- 12V supplies with +- 5V supplies. This uses the manufacturer's standard modules in their flexible power supply chassis design.
- /drawings/power-entry-and-dc-dc-converters.pdf
- The ADF-2 cards are sequenced so that after the power supplies are stable they wake up one at a time with 0.2 sec between.

ADF-2 Match to the BLS Signals

The intent of this section is to give the committee information about how the ADF-2 analog input range will match up with the BLS trigger pickoff signals that it must process.

- The original ADF plan was for one species of ADF card with 10 bit ADCs that could span the approximate 3:1 scale range in each eta calibration region and still provide 1/4 GeV Et LSBit output.
- The "single species" idea is doomed because of the incorrect resistor values that Dean was given for eta 1:8 HD.
- The best current understanding is that the full scale input range of the BLS signals actually span a 6:1 scale as one moves through the full eta range.
- Making the ADF-2 input not sensitive enough for the BLS signal that it receives is a disaster because the raw ADC data has more than 1/4 GeV per LSBit.
- Making the ADF-2 input too sensitive for the BLS signal that it receives would cut the full scale range of that channel to something less than 62 GeV.
- Picking the number of species has the normal trade offs: more species guarantees a match to the input signal, fewer species makes the management easier and gives more spare cards of each type.
- The different species will differ only in the value of a resistor in the Differential Amplifier section.
- In addition to all the 'normal' ADF-2 cards there will be a number of 'special' cards made for specific eta,phi locations where the BLS signal is single-ended because of broken BLS crate backplane pins.

ADF-2 Board Control PAL and Data Path FPGA Firmware

The intent of this section is to give the committee some information about how we are handling the firmware for the ADF-2 card.

- General Strategy:
  - Building block approach
  - Fully synchronous designs with a limited number of clock domains e.g. 1.
  - All signals sent and received from clocked IO Blocks
  - Full set of constraints
  - Separation of "test" firmware from "Physics Production" firmware.
  - Very tight version control of "Physics Production" firmware.
- Board Control PAL firmware is, by design, straight forward and fixed in function. The strong intent is that there will never be a change in the Board Control PAL firmware.
- Data Path FPGA firmware is also, by design, straight forward
  - Most of the Data Path FPGA does not need to change when the filtering algorithm changes.
  - Maintain a consistent interface to the Trigger Control Computer control software.
  - Start with a very simple filtering algorithm and prove that is all OK and understood.
  - /general/adf-2-data-path-fpga-description.txt
  - /drawings/data-path-fpga-signal-processing.pdf
  - The strategy for providing test data to TAB and collecting data for analysis is on the per turn basis without the need for tight "one shot" synchronization for testing.
- Et Filtering Plans
  - The first filter design will provide as the Et Filter output the value of the single ADC sample that was taken at the time of the BLS signal peak. The intent of this filter is that one must be able to understand its output data and verify the timing of this data.
  - The 2nd filter design will provide as the Et Filter output the average of the 4 ADC samples that were taken nearest to the time of the peak of the BLS signal. The intent of this filter is to use this high frequency filtering to improve the Et signals sent to TAB.

– The 3rd filter design will provide as its Et Filter output the difference between the average of 4 samples taken right before the beginning of the rise of the BLS signal and the average of the 4 samples taken at the peak of the BLS signal. The intent of this filter is to add low frequency filtering to remove the effect of BLS baseline shifts from the Et signals that are sent to the TAB.