L1CAL Control Software and ADF-2 Testing

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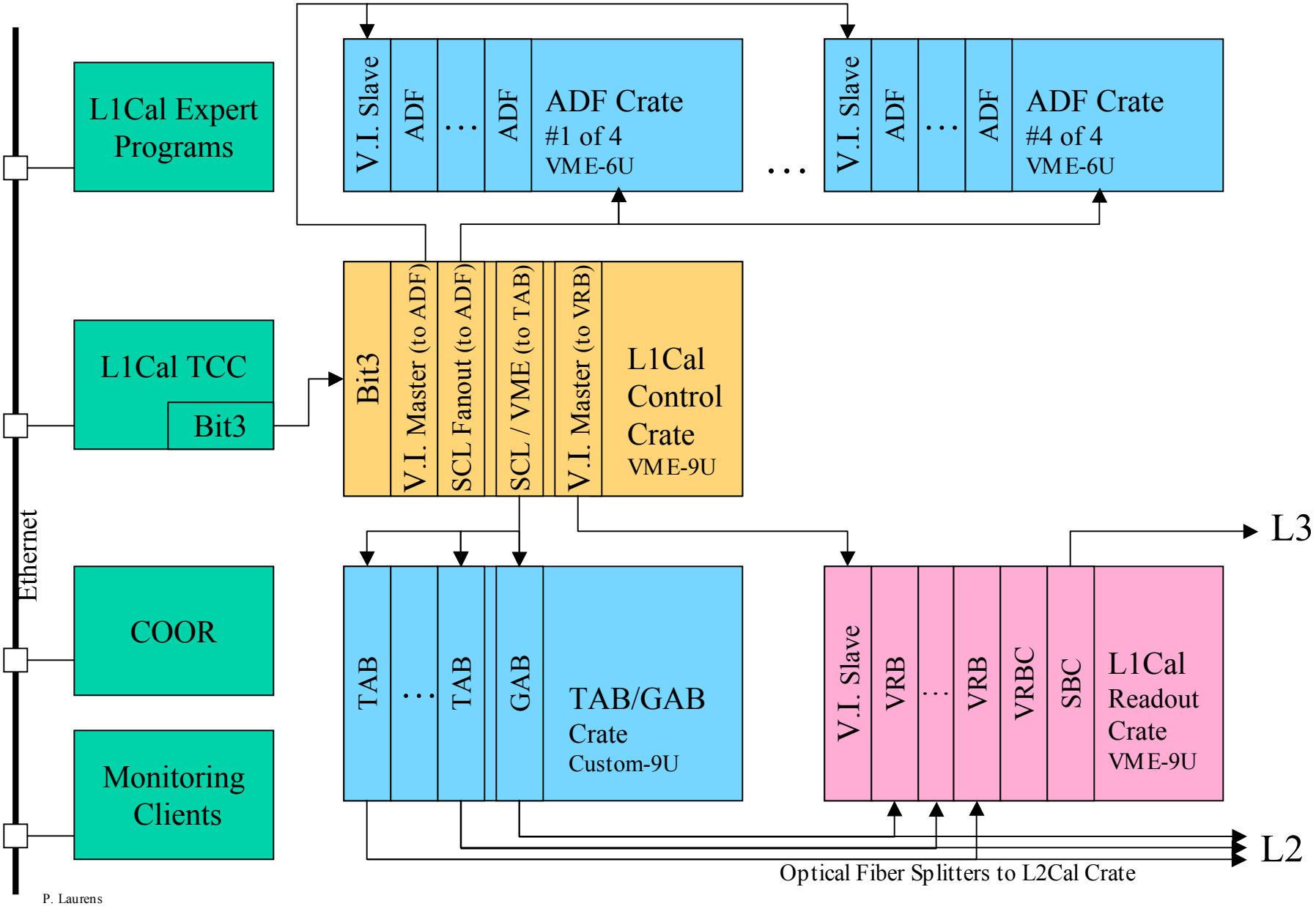
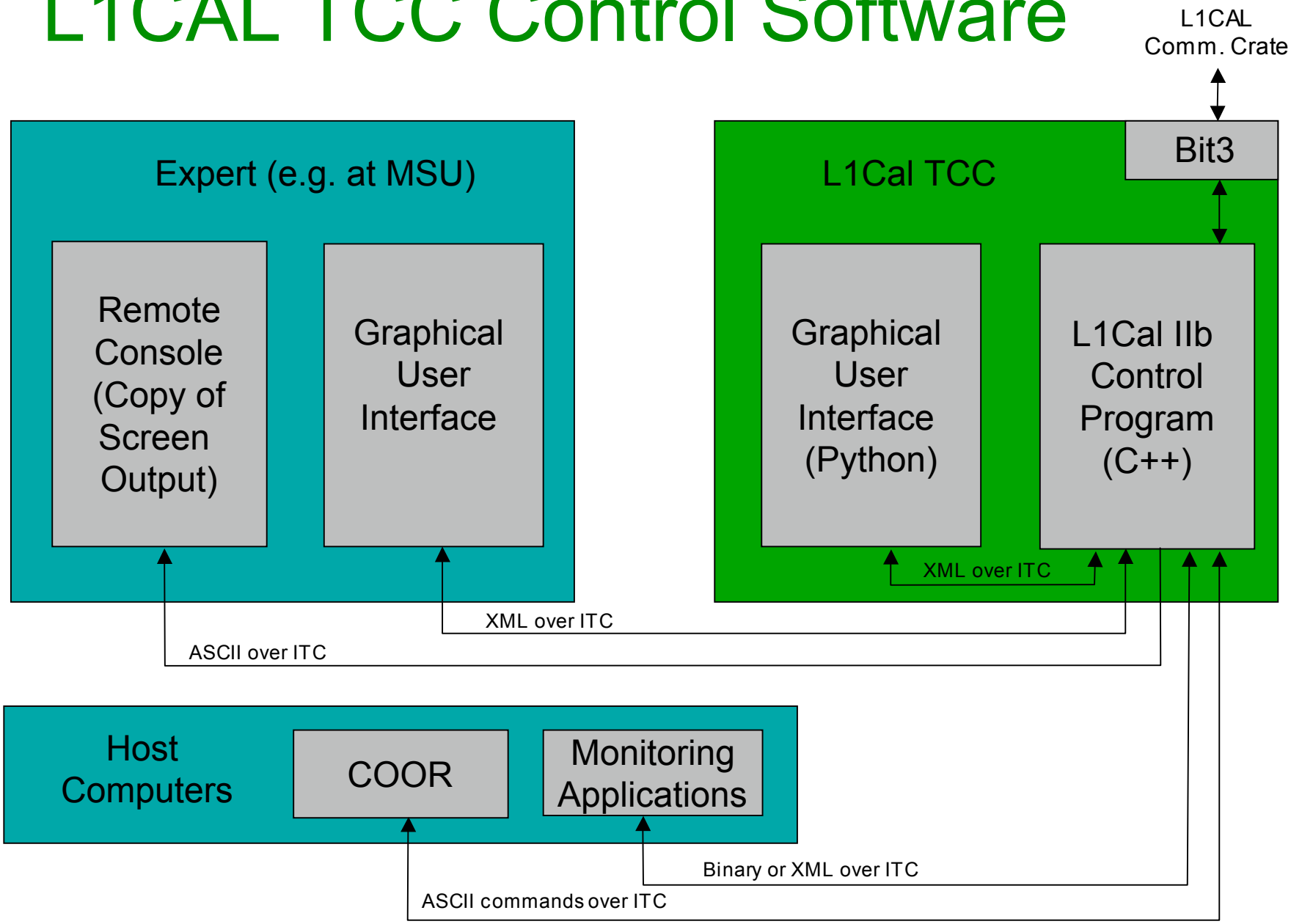
11-Feb-2005

Run IIb L1 Calorimeter Trigger Control Path

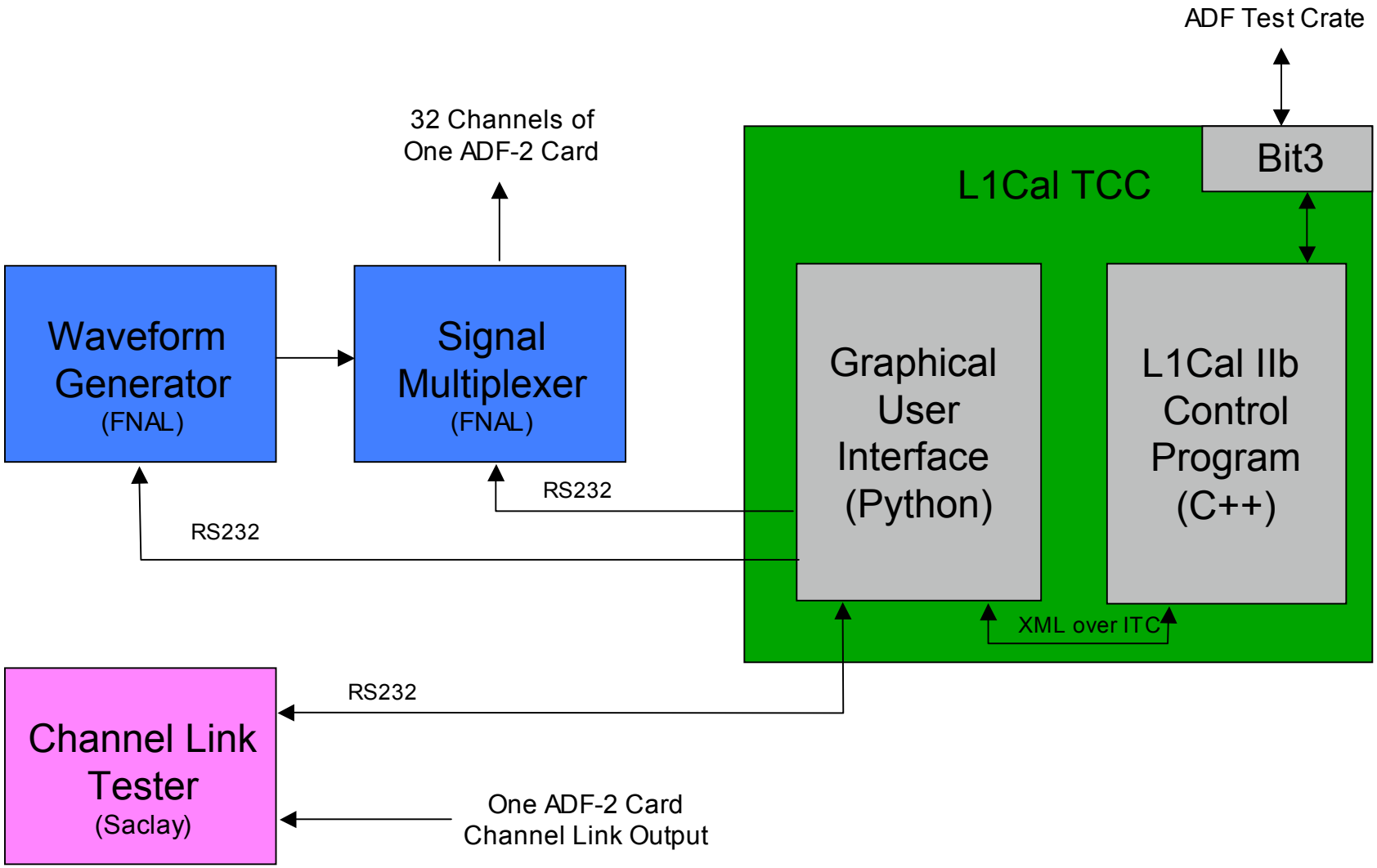


P. Laurens
Rev: 08-Oct-2003

L1CAL TCC Control Software



MSU ADF Test Setup



L1Cal IIb Control Software

- Partitioned
  - Control Code vs. GUI
- Operating System Independent
  - Windows & Linux
  - Python & C++
  - Use D0 products ITC and Thread_Util

L1Cal IIb Control Software

- L1CAL IIb Control Program

  - Use C++ for robustness and execution speed
  - Control and monitor both ADF and TAB/GAB
  - Only software actually performing VME IOs
  - Interface presenting one L1CAL system to COOR
  - Serve Monitoring Information to Host Monit Clients
  - Ported in large part from current L1FW+L1CAL TCC
  - Allow local command files
  - Keep running Logfile of all actions

L1Cal IIb Control Software

- Py_VME GUI
  - All new for IIb
  - Use Python with Tkinter for coding flexibility
  - Zero, One, or more GUI connected at given time
  - Not needed for COOR control
  - Not needed for monitoring operation
  - On Same or Remote computer
  - Greatly extendable with external python command files (of arbitrary complex)

L1Cal IIb Control Software

- Extensions with Python Command Files
  - Call functions to perform any action the GUI supports: R/W, Config FPGA, program DAC,...
  - Retrieve and use the reply from the Control Program (e.g. value read)
  - Recursive call to lower level command files while passing parameters (e.g. card address)
  - Control Waveform Generator and Multiplexer
  - Request interactive user input (e.g. card S/N)
  - Write test logfiles, any other files e.g. plot files
  - Execute OS commands, e.g. view plots

ADF-2 Production Testing

- Visual Inspection & Ohm meter
- Final Assembly (front panel, screws, etc)
- First Power Up: Configure Board Control PAL over JTAG
- A few VME IO to BC PAL registers
- Check PLL for Frequency Locking to SCLD
- Configure Data Path FPGAs over VME to load test firmware [.5 MB]
- Random Register Test: VME IO reliability with on multiple boards [no error in 1E10]
- Program Pedestal DAC: Measure DAC to ADC ratio [~7]
- "Find_DAC": DAC/ADC sanity check and tune ADC to mid-scale
- Channel Noise measurements (no input signal) [< 1/4 LSB]
- Measure Frequency Response of all channels (in-band, below and above)
- Crosstalk tests 32 input x 32 output channels [< 1/4 LSB worst case at 2 MHz]
- Channel Link tests (~5mn @MSU, extensively w/TAB @Fnal) [no error in 1E15]

- Misc Problems found so far: a few shorted or open traces on ADC data to FPGA

Frequency Response of multiple ADF-2 Cards

(Waveform Generator set at 1800mV)