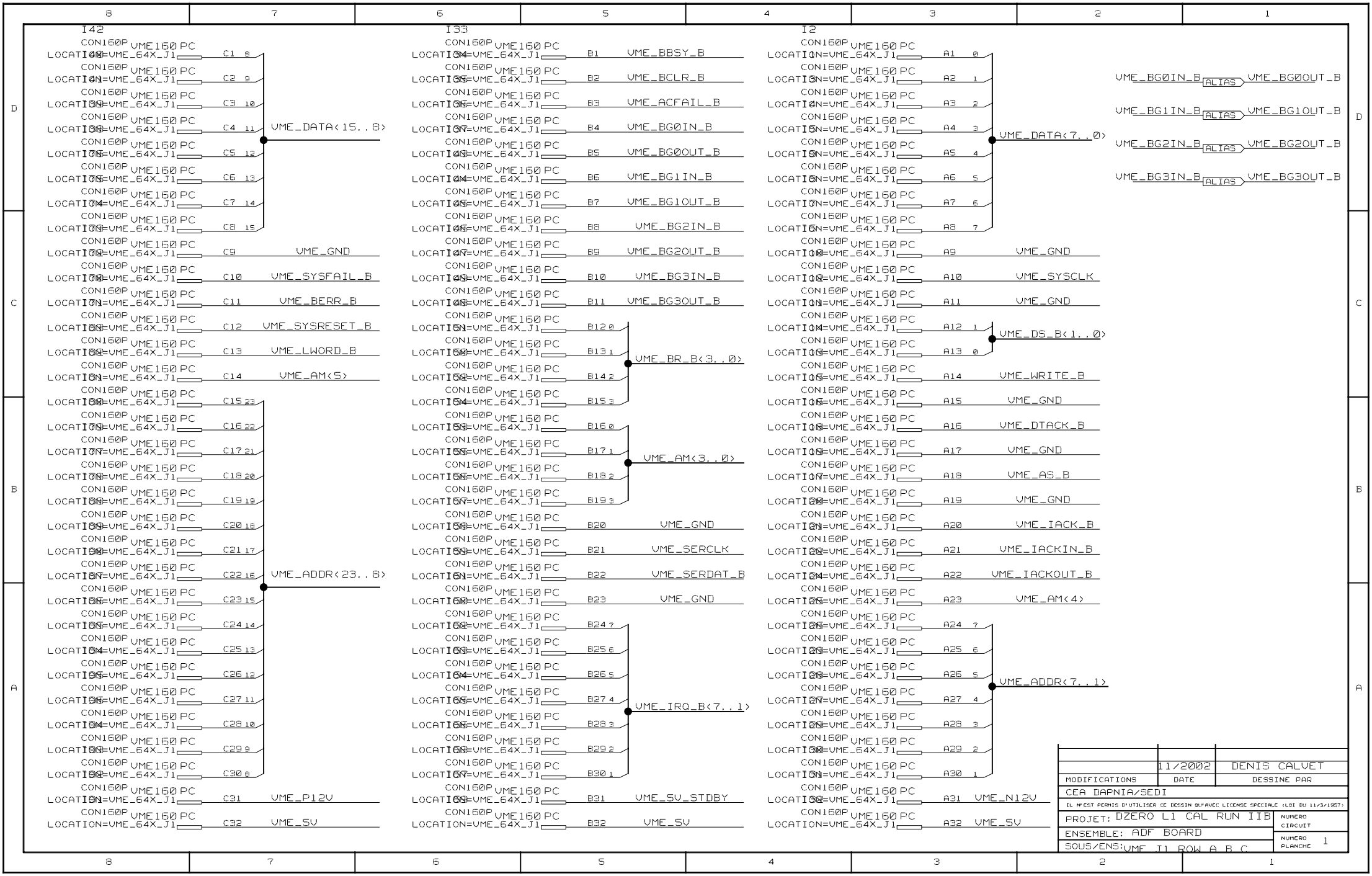
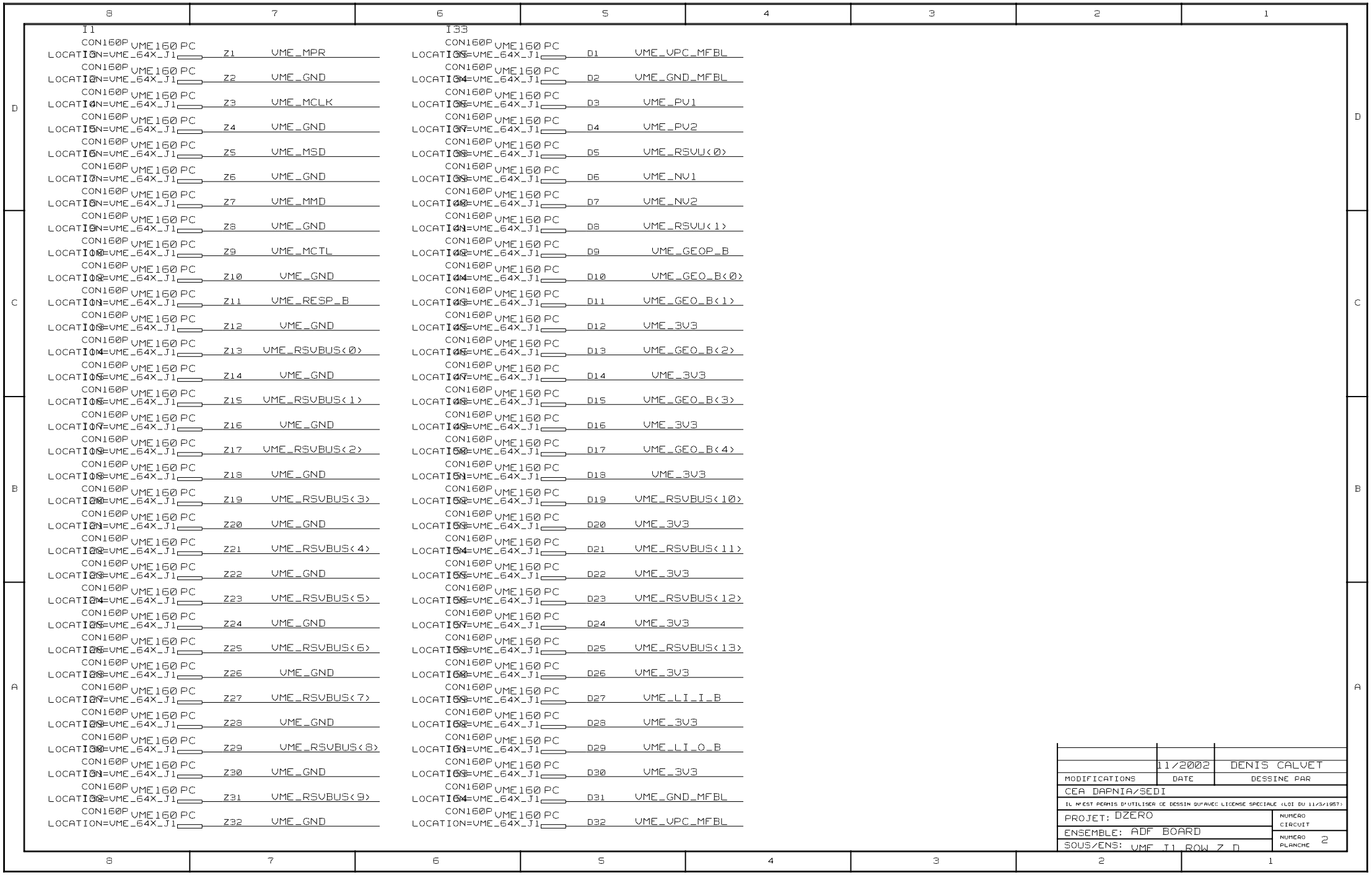
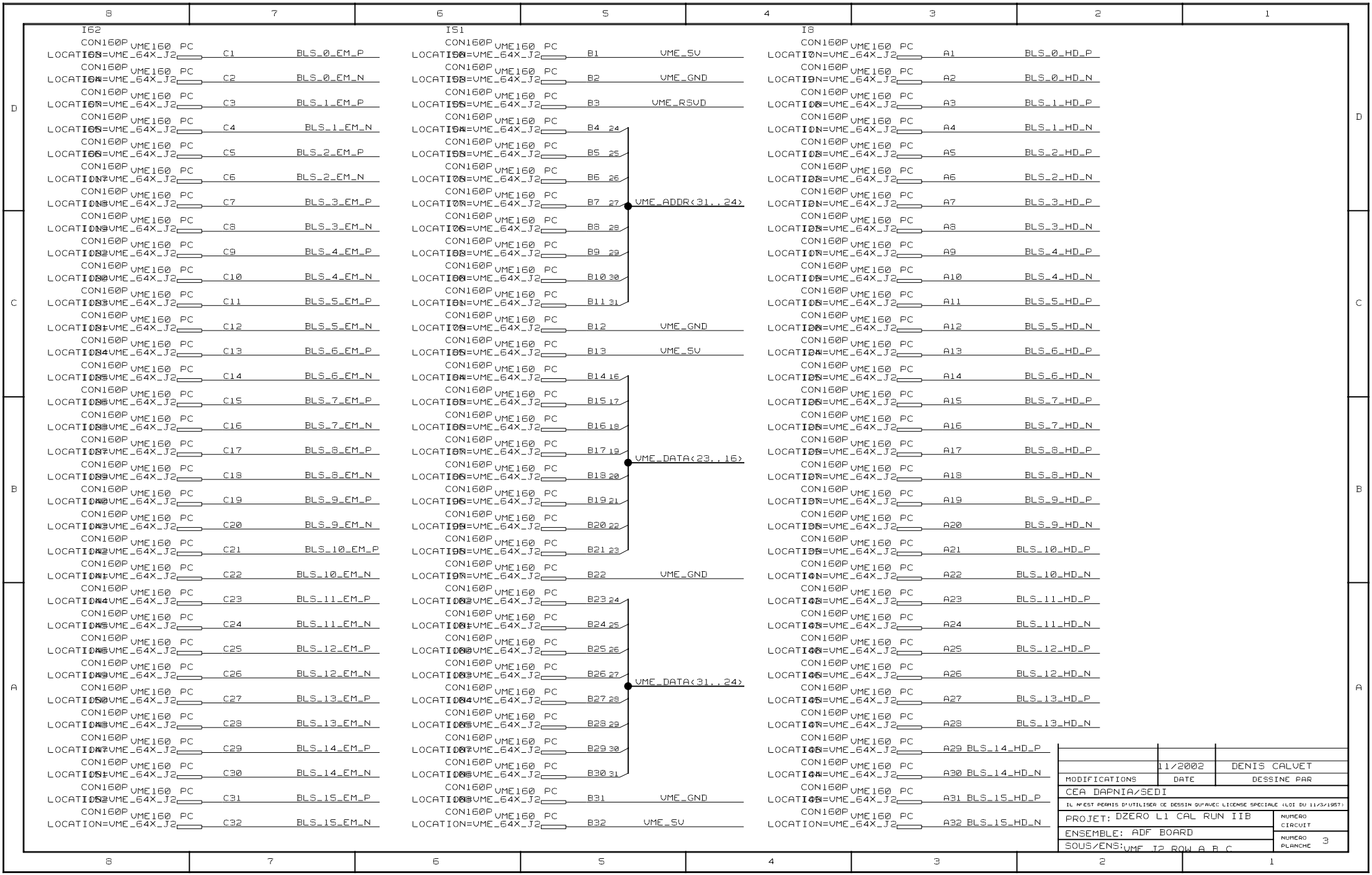
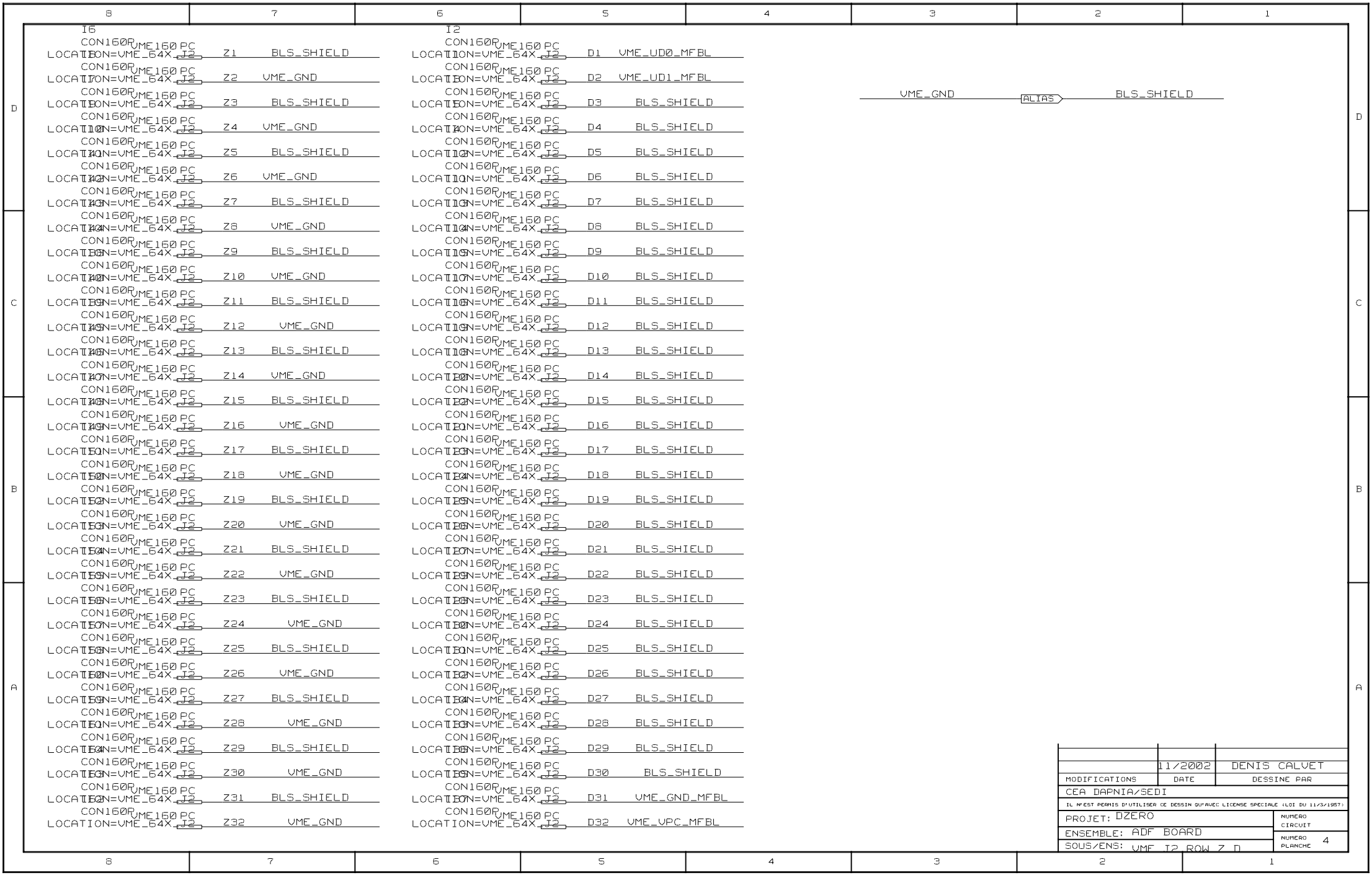
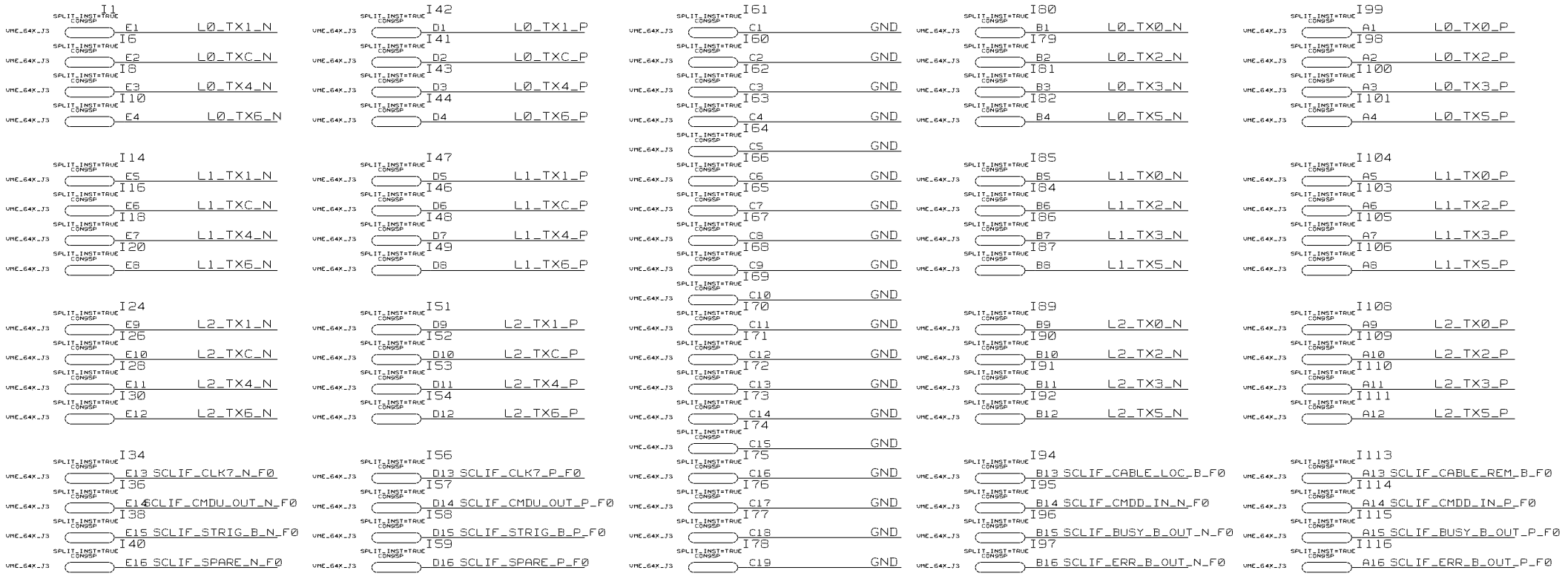

I42
I33
I2
CON160P VME160PC LOCATION=VME_64X_J1
C1 8
C2 9
C3 10
C4 11
C5 12
C6 13
C7 14
C8 15
VME_DATA<15..8>
C9 VME_GND
C10 VME_SYSFAIL_B
C11 VME_BERR_B
C12 VME_SYSRESET_B
C13 VME_LWORD_B
C14 VME_AM<5>
C15 23
C16 22
C17 21
C18 20
C19 19
C20 18
C21 17
C22 16
VME_ADDR<23..8>
C23 15
C24 14
C25 13
C26 12
C27 11
C28 10
C29 9
C30 8
C31 VME_P12V
C32 VME_5V
B1 VME_BBSY_B
B2 VME_BCLR_B
B3 VME_ACFAIL_B
B4 VME_BG0IN_B
B5 VME_BG0OUT_B
B6 VME_BG1IN_B
B7 VME_BG1OUT_B
B8 VME_BG2IN_B
B9 VME_BG2OUT_B
B10 VME_BG3IN_B
B11 VME_BG3OUT_B
B12 0
B13 1
VME_BR_B<3..0>
B14 2
B15 3
B16 0
B17 1
VME_AM<3..0>
B18 2
B19 3
B20 VME_GND
B21 VME_SERCLK
B22 VME_SERDAT_B
B23 VME_GND
B24 7
B25 6
B26 5
B27 4
VME_IRQ_B<7..1>
B28 3
B29 2
B30 1
B31 VME_5V_STDBY
B32 VME_5V
A1 0
A2 1
A3 2
A4 3
A5 4
A6 5
A7 6
A8 7
VME_DATA<7..0>
A9 VME_GND
A10 VME_SYSCLK
A11 VME_GND
A12 1
A13 0
VME_DS_B<1..0>
A14 VME_WRITE_B
A15 VME_GND
A16 VME_DTACK_B
A17 VME_GND
A18 VME_AS_B
A19 VME_GND
A20 VME_IACK_B
A21 VME_IACKIN_B
A22 VME_IACKOUT_B
A23 VME_AM<4>
A24 7
A25 6
A26 5
A27 4
VME_ADDR<7..1>
A28 3
A29 2
A30 1
A31 VME_N12V
A32 VME_5V
VME_BG0IN_B ALIAS VME_BG0OUT_B
VME_BG1IN_B ALIAS VME_BG1OUT_B
VME_BG2IN_B ALIAS VME_BG2OUT_B
VME_BG3IN_B ALIAS VME_BG3OUT_B
11/2002
DENIS CALVET
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: DZERO L1 CAL RUN IIB
NUMERO CIRCUIT
ENSEMBLE: ADF BOARD
SOUS/ENS: VME L1 ROW A B C
NUMERO PLANCHE
1


I1
I33
CON160P VME160PC LOCATION=VME_64X_J1
Z1 VME_MPR
Z2 VME_GND
Z3 VME_MCLK
Z4 VME_GND
Z5 VME_MSD
Z6 VME_GND
Z7 VME_MMD
Z8 VME_GND
Z9 VME_MCTL
Z10 VME_GND
Z11 VME_RESP_B
Z12 VME_GND
Z13 VME_RSVBUS<0>
Z14 VME_GND
Z15 VME_RSVBUS<1>
Z16 VME_GND
Z17 VME_RSVBUS<2>
Z18 VME_GND
Z19 VME_RSVBUS<3>
Z20 VME_GND
Z21 VME_RSVBUS<4>
Z22 VME_GND
Z23 VME_RSVBUS<5>
Z24 VME_GND
Z25 VME_RSVBUS<6>
Z26 VME_GND
Z27 VME_RSVBUS<7>
Z28 VME_GND
Z29 VME_RSVBUS<8>
Z30 VME_GND
Z31 VME_RSVBUS<9>
Z32 VME_GND
D1 VME_VPC_MFBL
D2 VME_GND_MFBL
D3 VME_PV1
D4 VME_PV2
D5 VME_RSVU<0>
D6 VME_NV1
D7 VME_NV2
D8 VME_RSVU<1>
D9 VME_GEOP_B
D10 VME_GEO_B<0>
D11 VME_GEO_B<1>
D12 VME_3V3
D13 VME_GEO_B<2>
D14 VME_3V3
D15 VME_GEO_B<3>
D16 VME_3V3
D17 VME_GEO_B<4>
D18 VME_3V3
D19 VME_RSVBUS<10>
D20 VME_3V3
D21 VME_RSVBUS<11>
D22 VME_3V3
D23 VME_RSVBUS<12>
D24 VME_3V3
D25 VME_RSVBUS<13>
D26 VME_3V3
D27 VME_LI_I_B
D28 VME_3V3
D29 VME_LI_O_B
D30 VME_3V3
D31 VME_GND_MFBL
D32 VME_VPC_MFBL
11/2002
DENIS CALVET
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: DZERO
NUMERO CIRCUIT
ENSEMBLE: ADF BOARD
SOUS/ENS: VME I1 ROW Z D
NUMERO PLANCHE 2


I62
I51
I8
CON160P VME160_PC LOCATION=VME_64X_J2
C1 BLS_0_EM_P
C2 BLS_0_EM_N
C3 BLS_1_EM_P
C4 BLS_1_EM_N
C5 BLS_2_EM_P
C6 BLS_2_EM_N
C7 BLS_3_EM_P
C8 BLS_3_EM_N
C9 BLS_4_EM_P
C10 BLS_4_EM_N
C11 BLS_5_EM_P
C12 BLS_5_EM_N
C13 BLS_6_EM_P
C14 BLS_6_EM_N
C15 BLS_7_EM_P
C16 BLS_7_EM_N
C17 BLS_8_EM_P
C18 BLS_8_EM_N
C19 BLS_9_EM_P
C20 BLS_9_EM_N
C21 BLS_10_EM_P
C22 BLS_10_EM_N
C23 BLS_11_EM_P
C24 BLS_11_EM_N
C25 BLS_12_EM_P
C26 BLS_12_EM_N
C27 BLS_13_EM_P
C28 BLS_13_EM_N
C29 BLS_14_EM_P
C30 BLS_14_EM_N
C31 BLS_15_EM_P
C32 BLS_15_EM_N
B1 VME_5V
B2 VME_GND
B3 VME_RSVD
B4 24
B5 25
B6 26
B7 27
B8 28
B9 29
B10 30
B11 31
VME_ADDR<31..24>
B12 VME_GND
B13 VME_5V
B14 16
B15 17
B16 18
B17 19
B18 20
B19 21
B20 22
B21 23
VME_DATA<23..16>
B22 VME_GND
B23 24
B24 25
B25 26
B26 27
B27 28
B28 29
B29 30
B30 31
VME_DATA<31..24>
B31 VME_GND
B32 VME_5V
A1 BLS_0_HD_P
A2 BLS_0_HD_N
A3 BLS_1_HD_P
A4 BLS_1_HD_N
A5 BLS_2_HD_P
A6 BLS_2_HD_N
A7 BLS_3_HD_P
A8 BLS_3_HD_N
A9 BLS_4_HD_P
A10 BLS_4_HD_N
A11 BLS_5_HD_P
A12 BLS_5_HD_N
A13 BLS_6_HD_P
A14 BLS_6_HD_N
A15 BLS_7_HD_P
A16 BLS_7_HD_N
A17 BLS_8_HD_P
A18 BLS_8_HD_N
A19 BLS_9_HD_P
A20 BLS_9_HD_N
A21 BLS_10_HD_P
A22 BLS_10_HD_N
A23 BLS_11_HD_P
A24 BLS_11_HD_N
A25 BLS_12_HD_P
A26 BLS_12_HD_N
A27 BLS_13_HD_P
A28 BLS_13_HD_N
A29 BLS_14_HD_P
A30 BLS_14_HD_N
A31 BLS_15_HD_P
A32 BLS_15_HD_N
11/2002
DENIS CALVET
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: DZERO L1 CAL RUN IIB
NUMERO CIRCUIT
ENSEMBLE: ADF BOARD
SOUS/ENS: VME I2 ROW A B C
NUMERO PLANCHE
3


I6
CON160R VME160PC LOCATION=VME_64X J2 Z1 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 Z2 VME_GND
CON160R VME160PC LOCATION=VME_64X J2 Z3 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 Z4 VME_GND
CON160R VME160PC LOCATION=VME_64X J2 Z5 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 Z6 VME_GND
CON160R VME160PC LOCATION=VME_64X J2 Z7 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 Z8 VME_GND
CON160R VME160PC LOCATION=VME_64X J2 Z9 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 Z10 VME_GND
CON160R VME160PC LOCATION=VME_64X J2 Z11 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 Z12 VME_GND
CON160R VME160PC LOCATION=VME_64X J2 Z13 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 Z14 VME_GND
CON160R VME160PC LOCATION=VME_64X J2 Z15 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 Z16 VME_GND
CON160R VME160PC LOCATION=VME_64X J2 Z17 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 Z18 VME_GND
CON160R VME160PC LOCATION=VME_64X J2 Z19 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 Z20 VME_GND
CON160R VME160PC LOCATION=VME_64X J2 Z21 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 Z22 VME_GND
CON160R VME160PC LOCATION=VME_64X J2 Z23 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 Z24 VME_GND
CON160R VME160PC LOCATION=VME_64X J2 Z25 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 Z26 VME_GND
CON160R VME160PC LOCATION=VME_64X J2 Z27 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 Z28 VME_GND
CON160R VME160PC LOCATION=VME_64X J2 Z29 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 Z30 VME_GND
CON160R VME160PC LOCATION=VME_64X J2 Z31 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 Z32 VME_GND
I2
CON160R VME160PC LOCATION=VME_64X J2 D1 VME_UD0_MFBL
CON160R VME160PC LOCATION=VME_64X J2 D2 VME_UD1_MFBL
CON160R VME160PC LOCATION=VME_64X J2 D3 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D4 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D5 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D6 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D7 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D8 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D9 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D10 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D11 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D12 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D13 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D14 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D15 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D16 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D17 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D18 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D19 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D20 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D21 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D22 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D23 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D24 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D25 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D26 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D27 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D28 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D29 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D30 BLS_SHIELD
CON160R VME160PC LOCATION=VME_64X J2 D31 VME_GND_MFBL
CON160R VME160PC LOCATION=VME_64X J2 D32 VME_VPC_MFBL
VME_GND ALIAS BLS_SHIELD
11/2002 DENIS CALVET
MODIFICATIONS DATE DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: DZERO
NUMERO CIRCUIT
ENSEMBLE: ADF BOARD
SOUS/ENS: VME I2 ROW Z D
NUMERO PLANCHE 4



GND ALIAS VME_GND

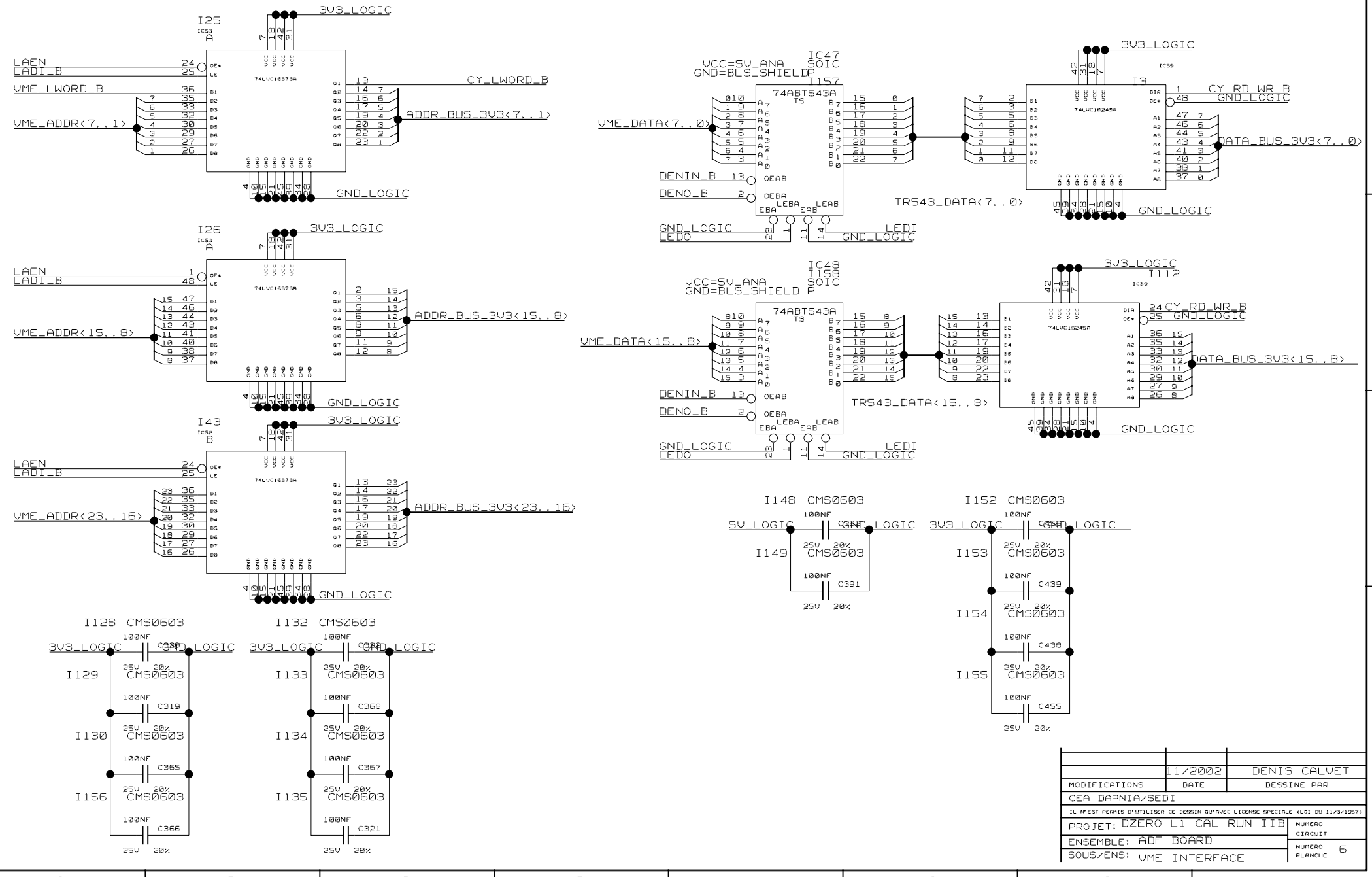
	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR

CEA DAPNIA/SEDI

PROJET: DZERO L1 CAL RUN IIB — NUMERO CIRCUIT

ENSEMBLE: ADF BOARD

SOUS/ENS: VME I0 ROW ABCDF — NUMERO PLANCHE 5



	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR

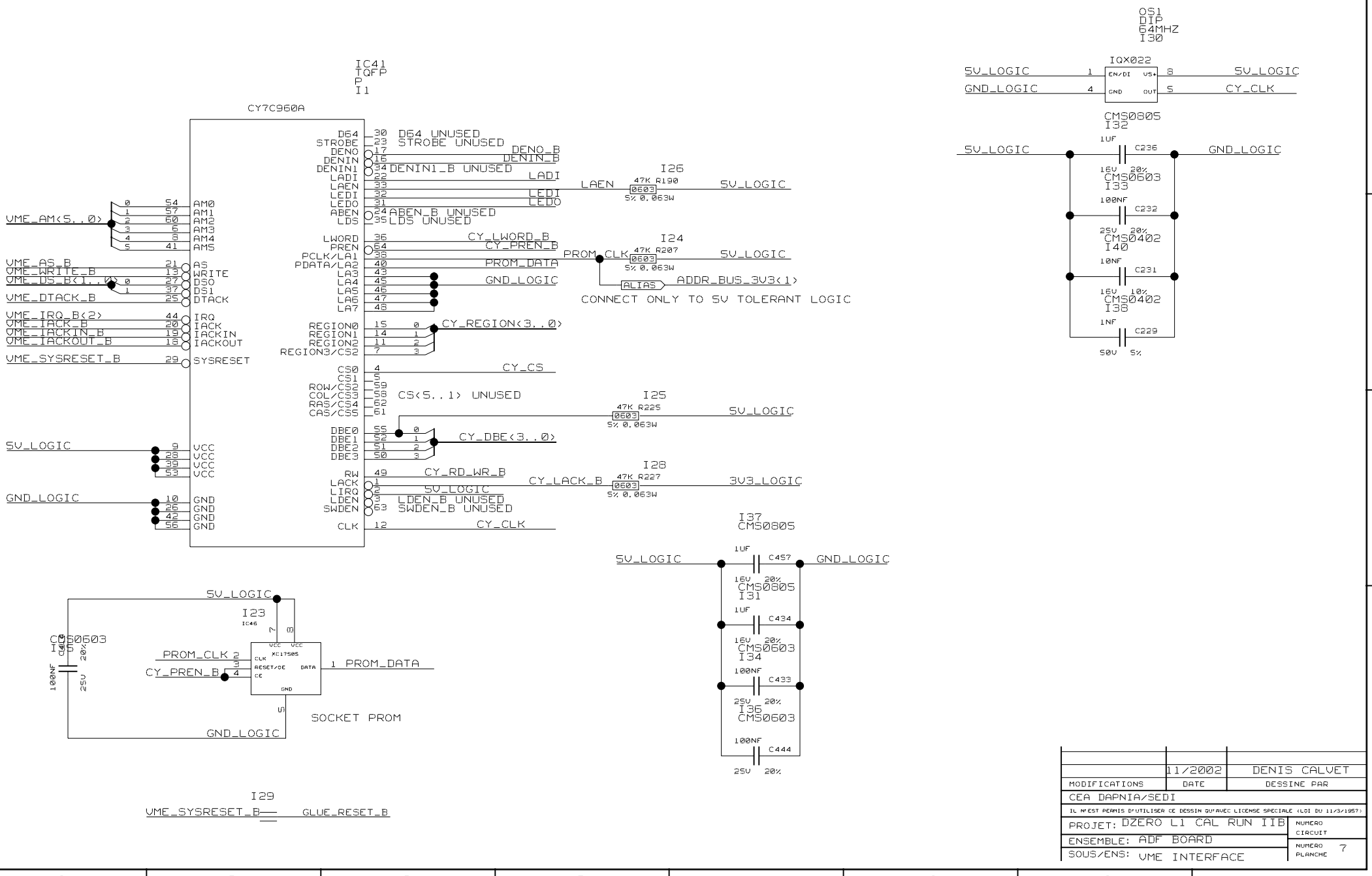
CEA DAPNIA/SEDI

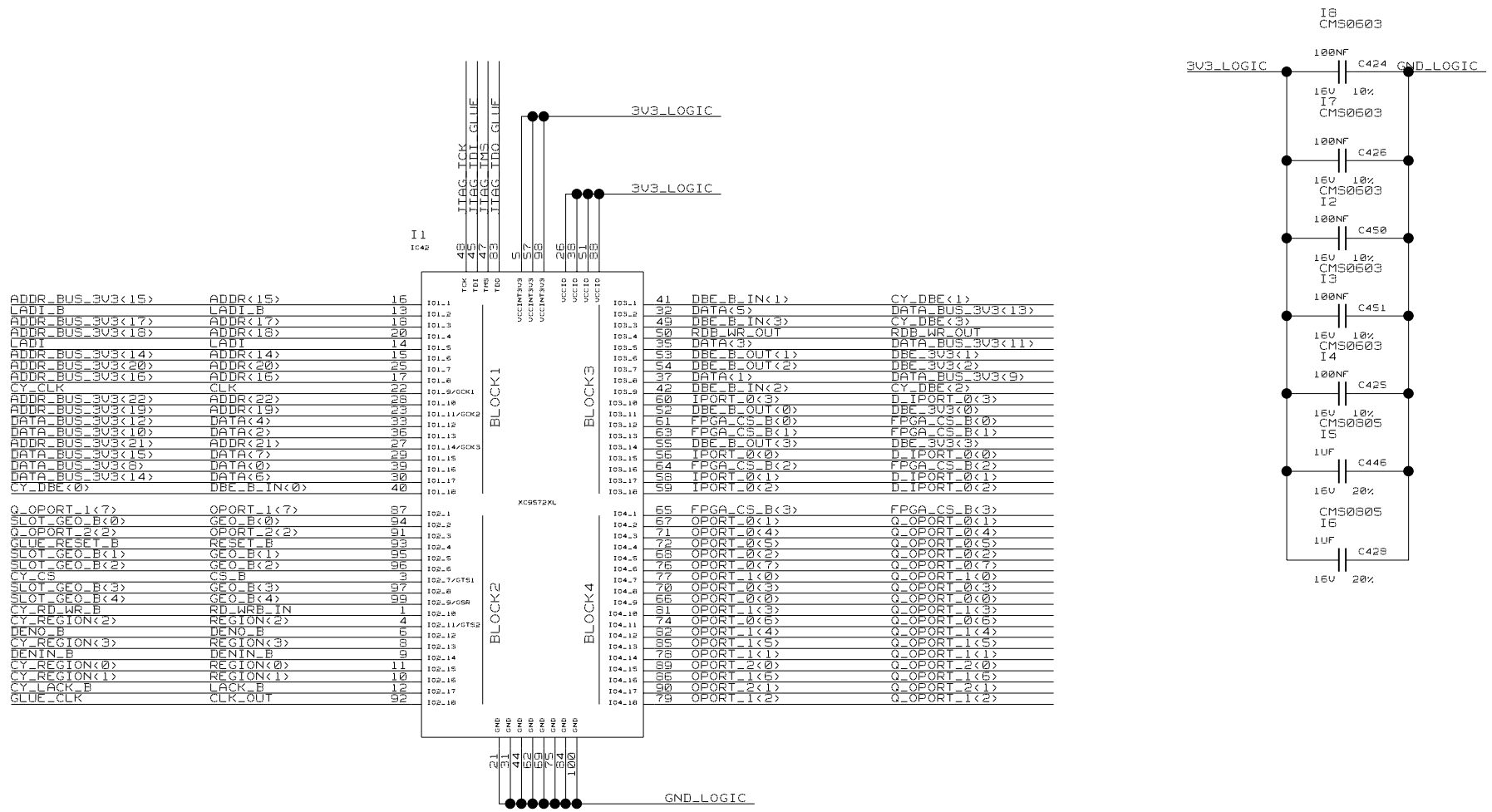
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)

PROJET: DZERO L1 CAL RUN IIB — NUMERO CIRCUIT

ENSEMBLE: ADF BOARD

SOUS/ENS: VME INTERFACE — NUMERO PLANCHE 6


IC41
TQFP
P
I1
CY7C960A
D64 30 D64 UNUSED
STROBE 23 STROBE UNUSED
DENO 17 DENO_B
DENIN 16 DENIN_B
DENIN1 34 DENIN1_B UNUSED
LADI 22 LADI
LAEN 33 LAEN
LEDI 32 LEDI
LEDO 31 LEDO
ABEN 24 ABEN_B UNUSED
LDS 35 LDS UNUSED
LWORD 36 CY_LWORD_B
PREN 64 CY_PREN_B
PCLK/LA1 38 PROM
PDATA/LA2 40 PROM_DATA
LA3 43
LA4 45 GND_LOGIC
LA5 46
LA6 47
LA7 48
REGION0 15 CY_REGION<3..0>
REGION1 14
REGION2 11
REGION3/CS2 7
CS0 4 CY_CS
CS1 5
ROW/CS3 59
COL/CS5 58 CS<5..1> UNUSED
RAS/CS4 62
CAS/CS5 61
DBE0 55 CY_DBE<3..0>
DBE1 52
DBE2 51
DBE3 50
RW 49 CY_RD_WR_B
LACK 1 CY_LACK_B
LIRQ 2 5V_LOGIC
LDEN 3 LDEN_B UNUSED
SWDEN 63 SWDEN_B UNUSED
CLK 12 CY_CLK
VME_AM<5..0>
AM0 54
AM1 57
AM2 60
AM3 61
AM4 40
AM5 41
VME_AS_B 21 AS
VME_WRITE_B 13 WRITE
VME_DS_B<1..0> DS0 27
DS1 37
VME_DTACK_B 25 DTACK
VME_IRQ_B<2> 44 IRQ
VME_IACK_B 20 IACK
VME_IACKIN_B 19 IACKIN
VME_IACKOUT_B 18 IACKOUT
VME_SYSRESET_B 29 SYSRESET
5V_LOGIC
VCC 9
VCC 28
VCC 39
VCC 53
GND_LOGIC
GND 10
GND 26
GND 42
GND 56
I26
47K R190 0603 5% 0.063W
LAEN 5V_LOGIC
I24
47K R207 0603 5% 0.063W
PROM CLK 5V_LOGIC
ALIAS ADDR_BUS_3V3<1>
CONNECT ONLY TO 5V TOLERANT LOGIC
I25
47K R225 0603 5% 0.063W
5V_LOGIC
I28
47K R227 0603 5% 0.063W
CY_LACK_B 3V3_LOGIC
I23
IC46
XC17S05
VCC VCC
CLK
RESET/OE DATA
CE
GND
PROM_CLK
CY_PREN_B
1 PROM_DATA
SOCKET PROM
5V_LOGIC
GND_LOGIC
I29
VME_SYSRESET_B GLUE_RESET_B
O51
DIP
64MHZ
I30
IQX022
EN/DI VS+
GND OUT
5V_LOGIC 1
GND_LOGIC 4
8 5V_LOGIC
5 CY_CLK
CMS0805
I32
5V_LOGIC
1UF C236 GND_LOGIC
16V 20%
CMS0603
I33
100NF C232
25V 20%
CMS0402
I40
10NF C231
16V 10%
CMS0402
I38
1NF C229
50V 5%
I37
CMS0805
5V_LOGIC
1UF C457 GND_LOGIC
16V 20%
CMS0805
I31
1UF C434
16V 20%
CMS0603
I34
100NF C433
25V 20%
I36
CMS0603
100NF C444
25V 20%
11/2002
DENIS CALVET
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: DZERO L1 CAL RUN IIB
NUMERO CIRCUIT
ENSEMBLE: ADF BOARD
SOUS/ENS: VME INTERFACE
NUMERO PLANCHE 7



Q_OPORT_2<2> ALIAS FPGA_RESET

FPGA_CS_B_F0 ALIAS FPGA_CS_B<0>

FPGA_CS_B_F1 ALIAS FPGA_CS_B<1>

FPGA_CS_B_F2 ALIAS FPGA_CS_B<2>

FPGA_CS_B_F3 ALIAS FPGA_CS_B<3>

VME_GEO_B<0> ALIAS SLOT_GEO_B<0>

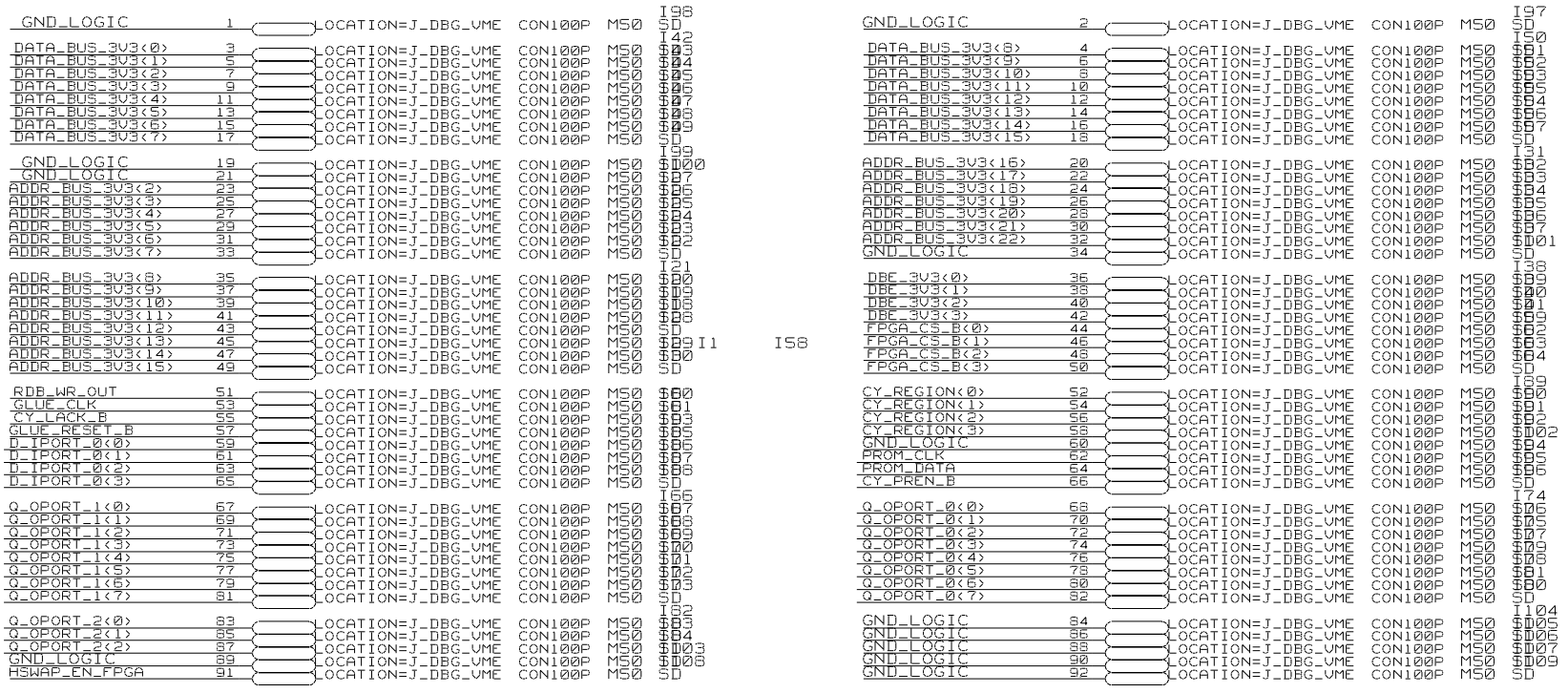
VME_GEO_B<1> ALIAS SLOT_GEO_B<1>

VME_GEO_B<2> ALIAS SLOT_GEO_B<2>

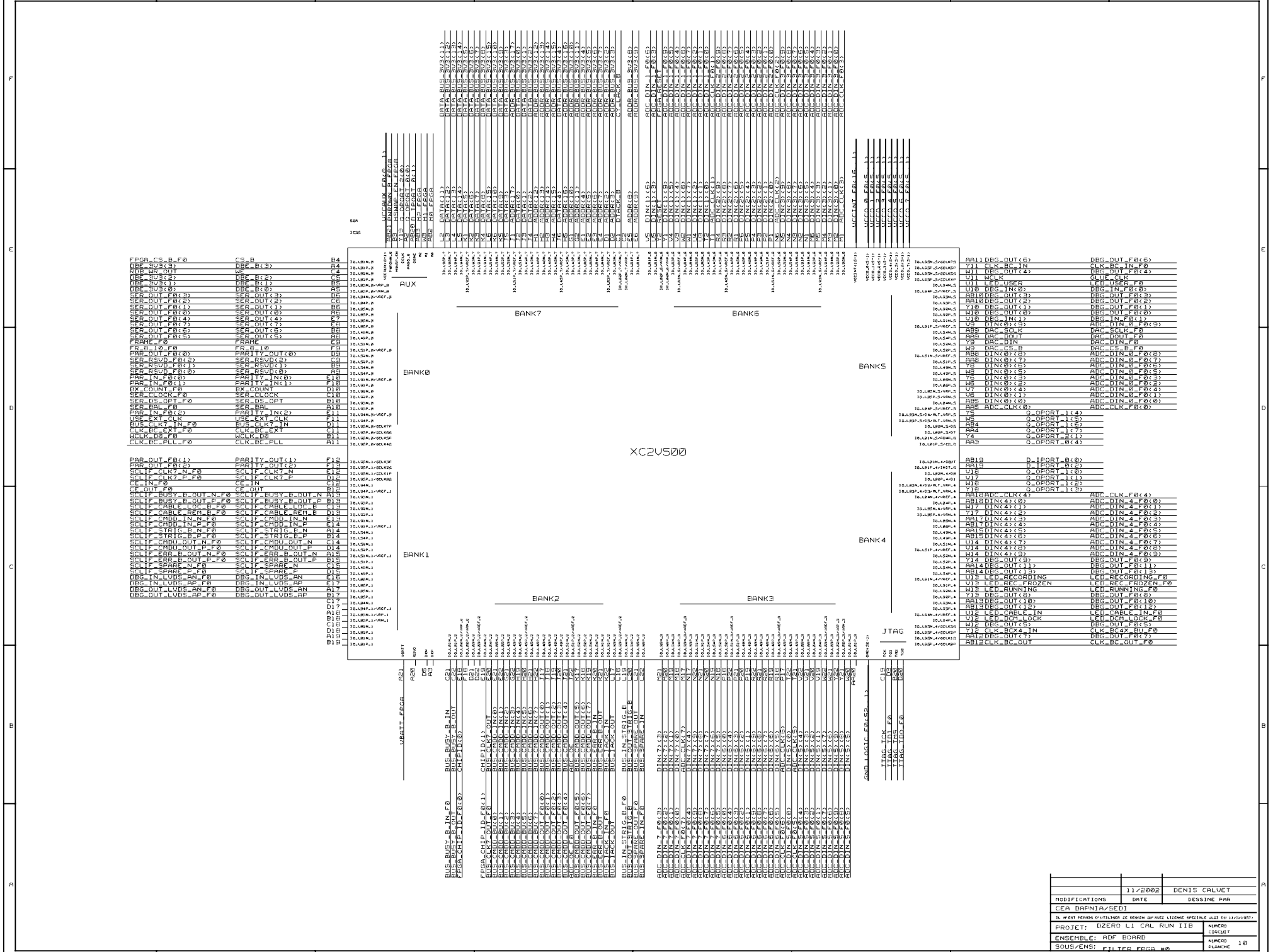
VME_GEO_B<3> ALIAS SLOT_GEO_B<3>

VME_GEO_B<4> ALIAS SLOT_GEO_B<4>

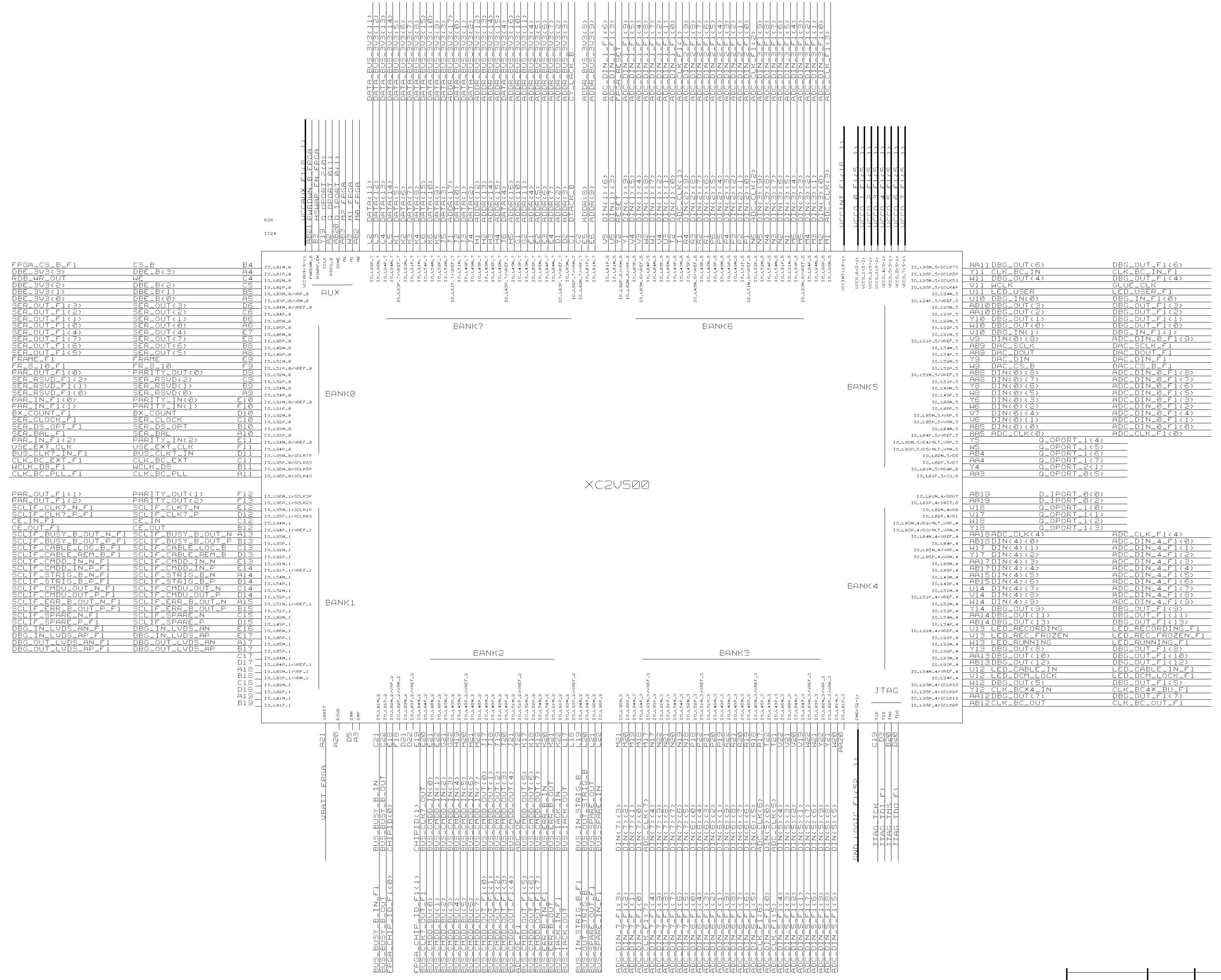
	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: VME INTERFACE		NUMERO PLANCHE 8



	01/2003	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: DEBUG VME INTERFACE		NUMERO PLANCHE 9



		11/2002	DENIS CALVET
MODIFICATIONS		DATE	DESSINE PAR
CEA DAPNIA/SEDI			
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC L'ACCORD SPECIALE ECRIT DU 11/3/1957			
PROJET: DZERO L1 CAL RUN IIB			NUMERO CIRCUIT
ENSEMBLE: ADF BOARD			NUMERO PLANCHE 10
SOUS/ENS: FILTER FEGA #0			



	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR

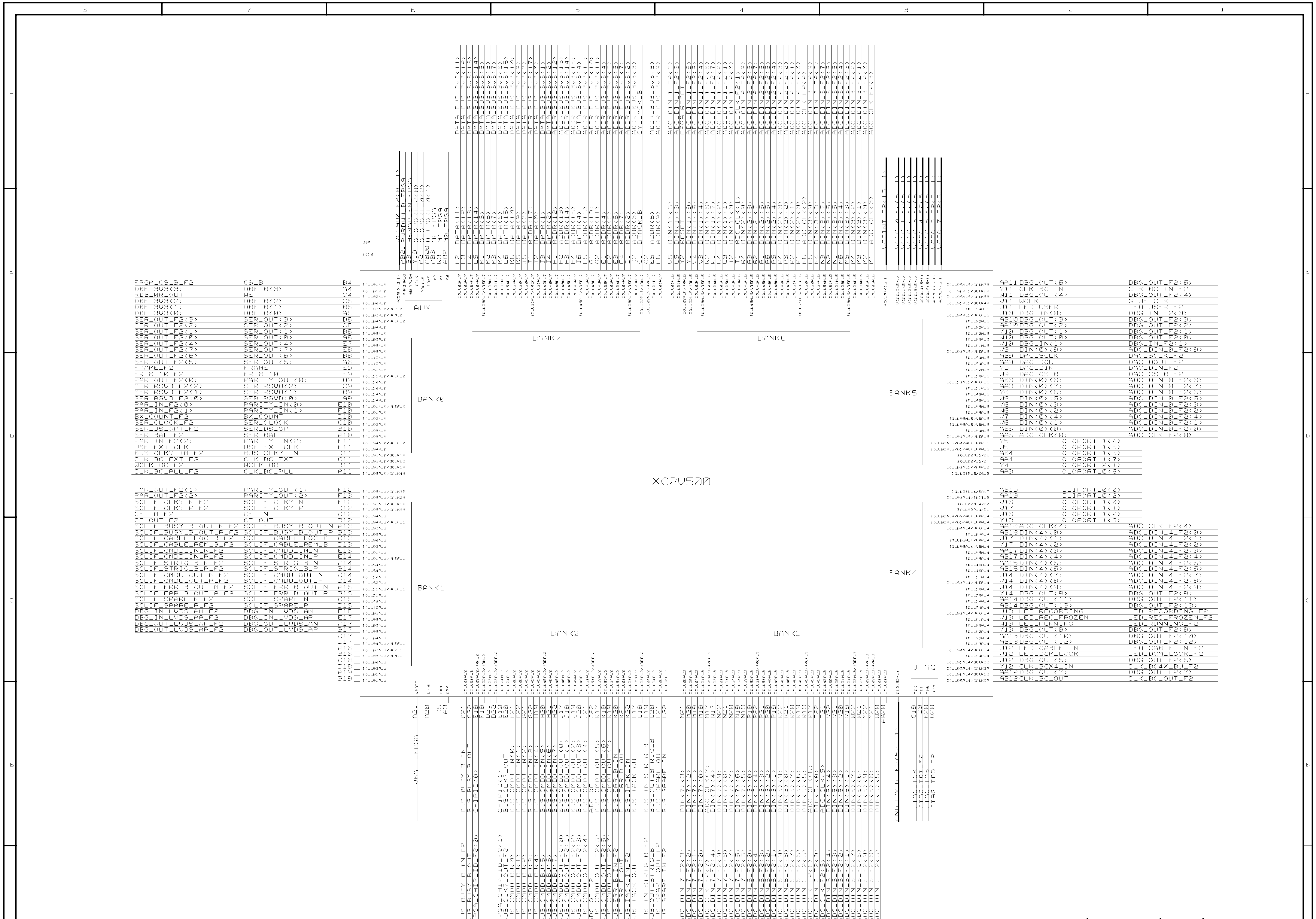
CEA DAPNIA/SEDI

IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)

PROJET: DZERO L1 CAL RUN IIB — NUMERO CIRCUIT

ENSEMBLE: ADF BOARD — NUMERO PLANCHE 11

SOUS/ENS: FILTER FPGA #1



MODIFICATIONS	DATE	DESSINE PAR
	11/2002	DENIS CALVET

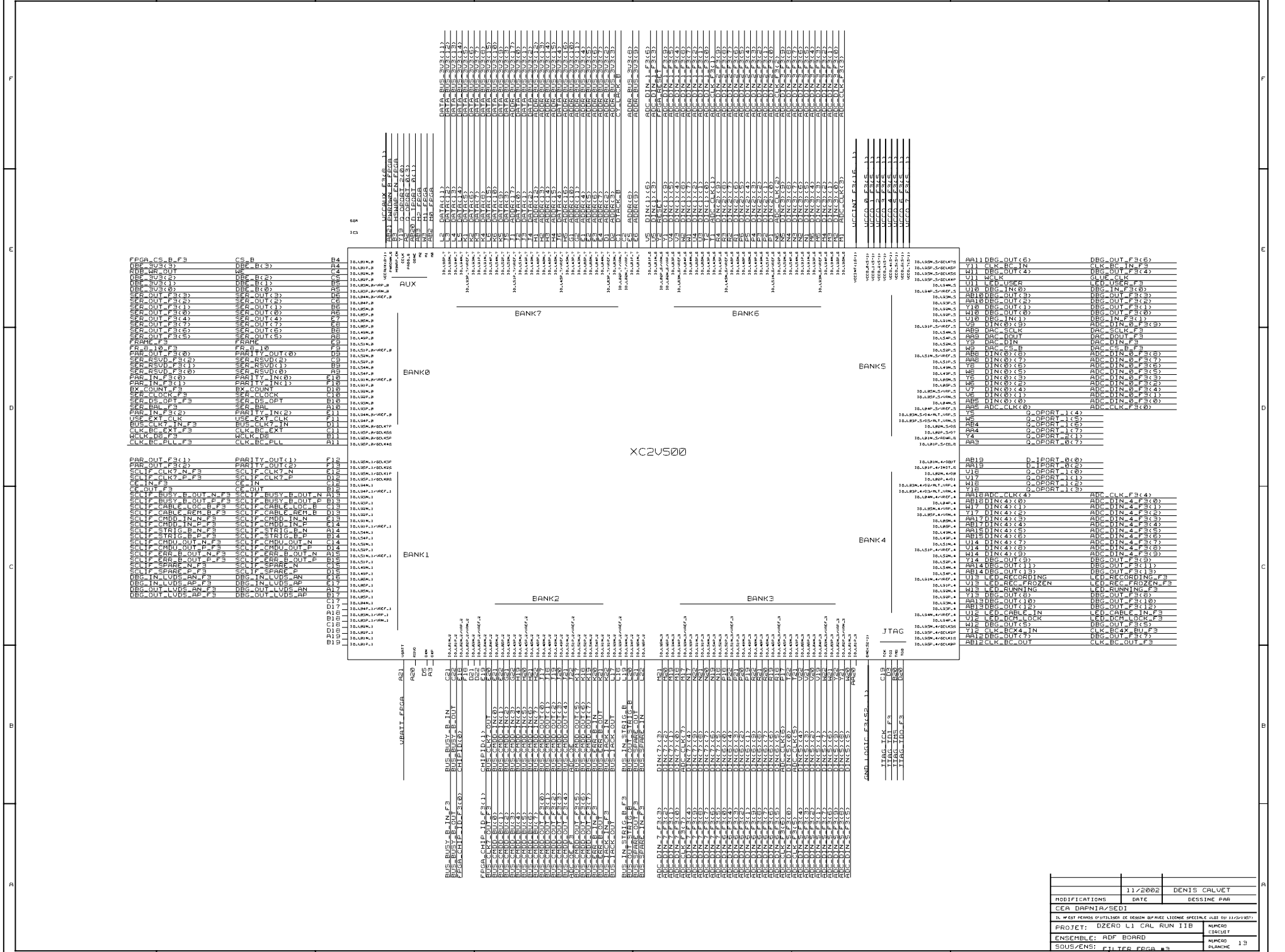
CEA DAPNIA/SEDI

IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)

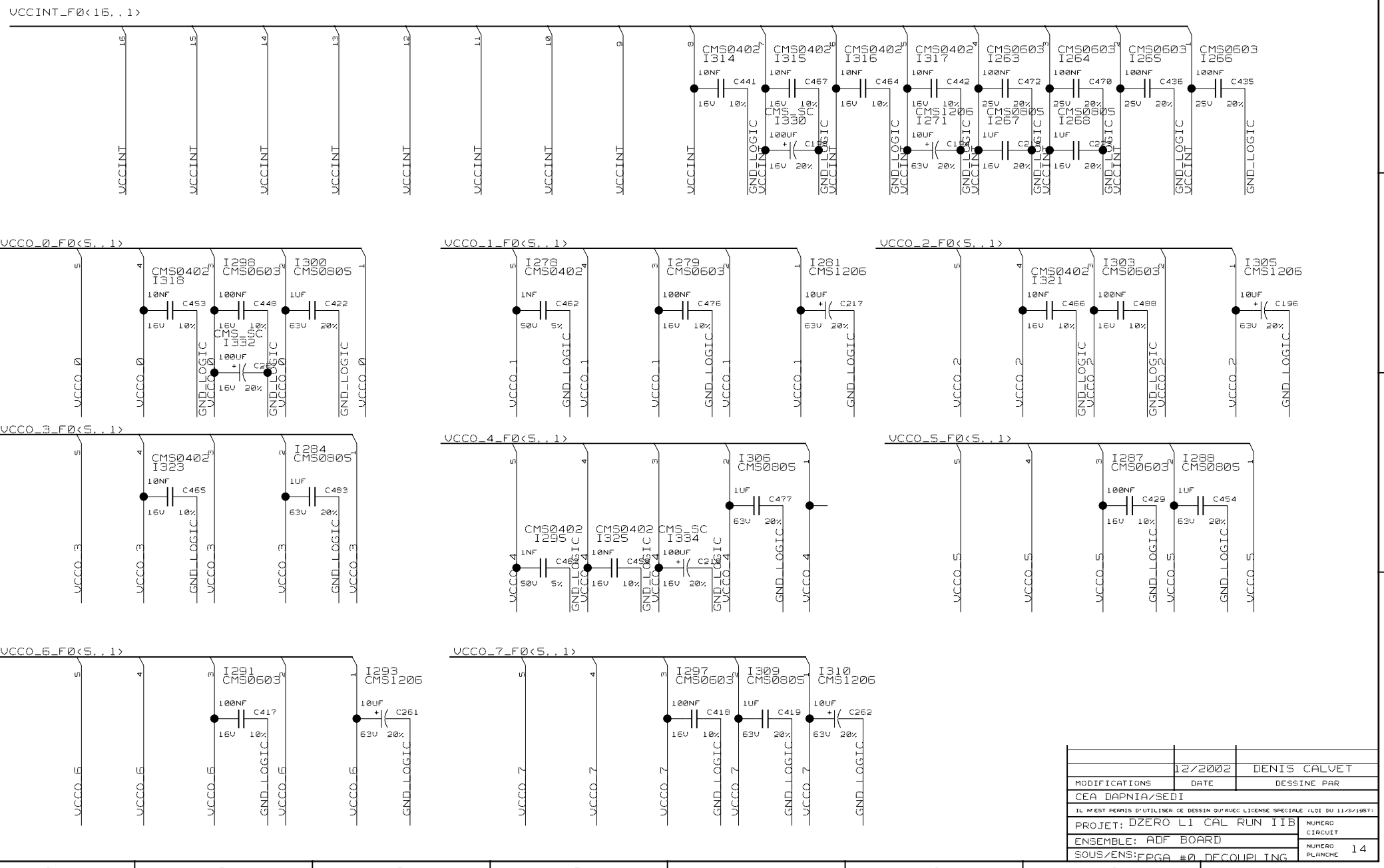
PROJET: DZERO L1 CAL RUN IIB — NUMERO CIRCUIT

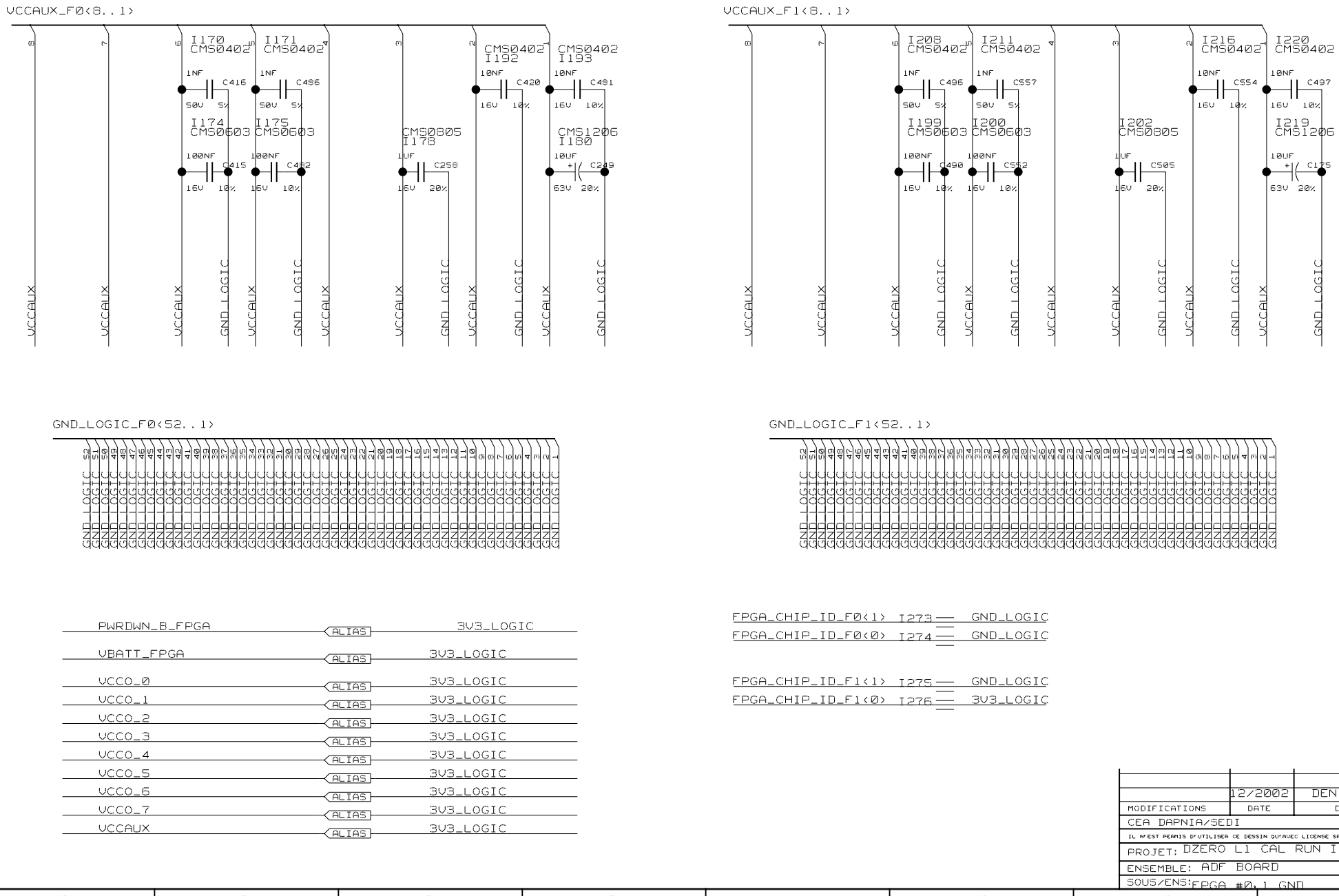
ENSEMBLE: ADF BOARD

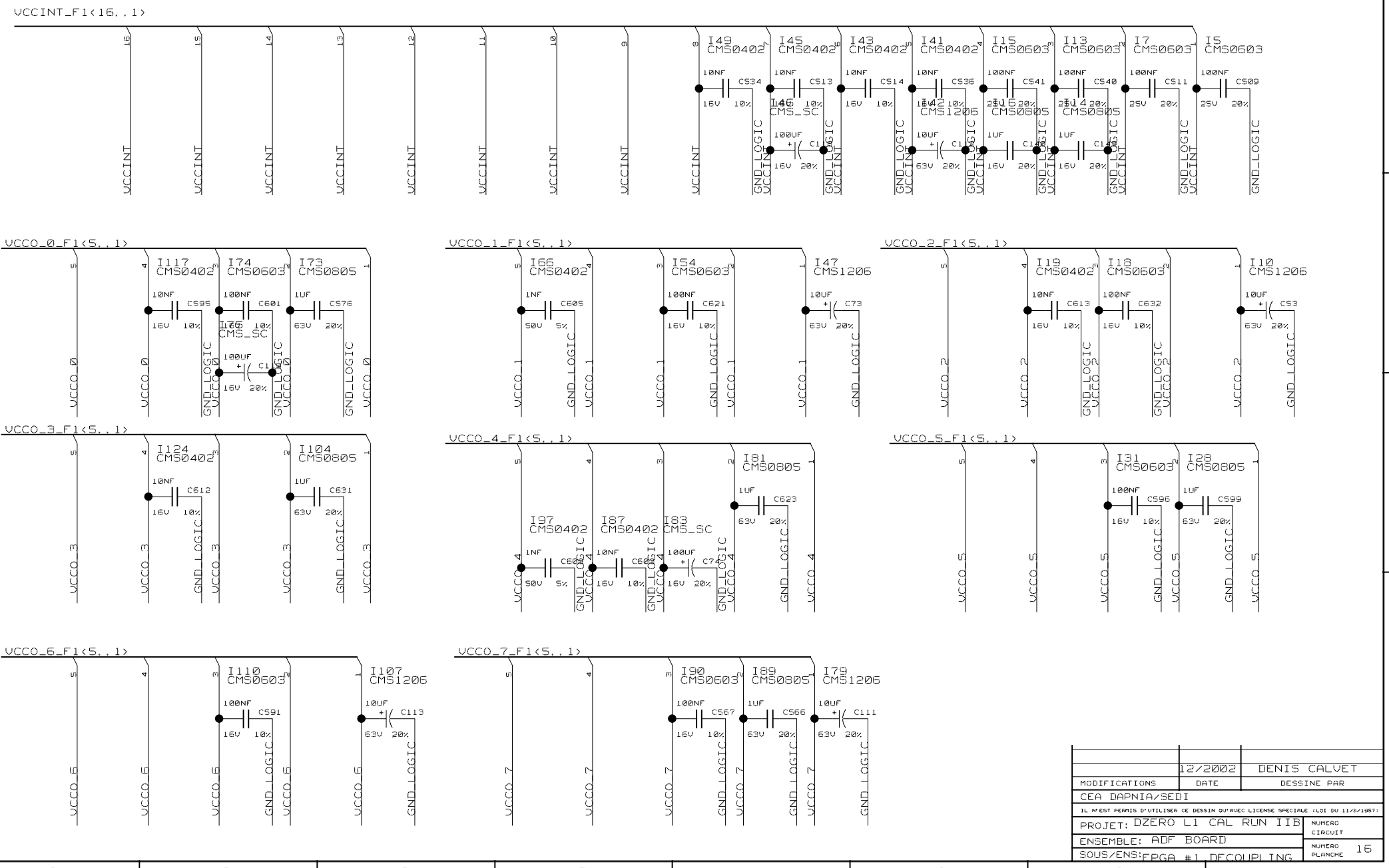
SOUS/ENS: FILTER FPGA #2 — NUMERO PLANCHE 12



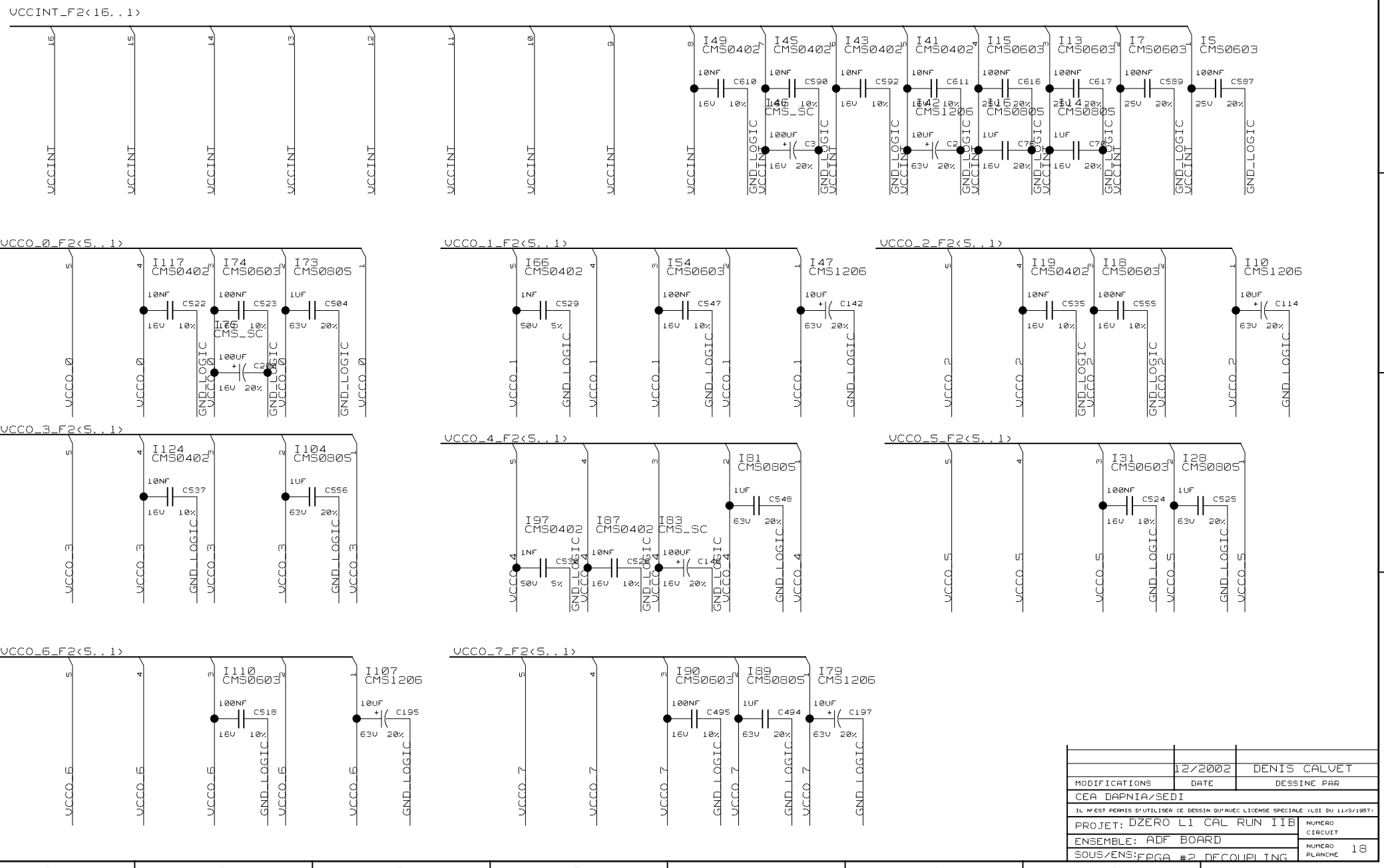
	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC L'ACCORD SPECIALE ECRIT DU 11/3/1997		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		NUMERO PLANCHE 13
SOUS/ENS: FILTER FEGA #3		


VCCINT_F0<16..1>
VCCINT
CMS0402 I314
CMS0402 I315
CMS0402 I316
CMS0402 I317
CMS0603 I263
CMS0603 I264
CMS0603 I265
CMS0603 I266
10NF C441
10NF C467
10NF C454
10NF C442
100NF C472
100NF C470
100NF C436
100NF C435
CMS1206 I330
CMS1206 I271
CMS0805 I267
CMS0805 I268
100UF C1
10UF C1
1UF C2
GND_LOGIC
VCCO_0_F0<5..1>
CMS0402 I318
I298 CMS0603
I300 CMS0805
10NF C453
100NF C448
1UF C422
CMS1206 I331
100UF C2
VCCO_0
VCCO_1_F0<5..1>
I278 CMS0402
I279 CMS0603
I281 CMS1206
1NF C452
100NF C476
10UF C217
VCCO_1
VCCO_2_F0<5..1>
CMS0402 I321
I303 CMS0603
I305 CMS1206
10NF C466
100NF C488
10UF C196
VCCO_2
VCCO_3_F0<5..1>
CMS0402 I323
I284 CMS0805
10NF C465
1UF C453
VCCO_3
VCCO_4_F0<5..1>
I306 CMS0805
CMS0402 I295
CMS0402 I325
CMS1206 I334
1UF C477
1NF C450
10NF C451
100UF C215
VCCO_4
VCCO_5_F0<5..1>
I287 CMS0603
I288 CMS0805
100NF C429
1UF C454
VCCO_5
VCCO_6_F0<5..1>
I291 CMS0603
I293 CMS1206
100NF C417
10UF C261
VCCO_6
VCCO_7_F0<5..1>
I297 CMS0603
I309 CMS0805
I310 CMS1206
100NF C418
1UF C419
10UF C262
VCCO_7
16V 10%
50V 5%
63V 20%
25V 20%
12/2002
DENIS CALVET
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: DZERO L1 CAL RUN IIB
NUMERO CIRCUIT
ENSEMBLE: ADF BOARD
SOUS/ENS: FPGA #0 DECOUPLING
NUMERO PLANCHE
14


VCCAUX_F0<8..1>
I170 CMS0402
I171 CMS0402
CMS0402 I192
CMS0402 I193
1NF C416 50V 5%
1NF C486 50V 5%
10NF C420 16V 10%
10NF C481 16V 10%
I174 CMS0603
I175 CMS0603
CMS0805 I178
CMS1206 I180
100NF C415 16V 10%
100NF C482 16V 10%
1UF C258 16V 20%
10UF C249 63V 20%
VCCAUX
GND_LOGIC
VCCAUX_F1<8..1>
I208 CMS0402
I211 CMS0402
I216 CMS0402
I220 CMS0402
1NF C496 50V 5%
1NF C557 50V 5%
10NF C554 16V 10%
10NF C497 16V 10%
I199 CMS0603
I200 CMS0603
I202 CMS0805
I219 CMS1206
100NF C490 16V 10%
100NF C552 16V 10%
1UF C505 16V 20%
10UF C175 63V 20%
GND_LOGIC_F0<52..1>
GND_LOGIC_F1<52..1>
PWRDWN_B_FPGA ALIAS 3V3_LOGIC
VBATT_FPGA ALIAS 3V3_LOGIC
VCCO_0 ALIAS 3V3_LOGIC
VCCO_1 ALIAS 3V3_LOGIC
VCCO_2 ALIAS 3V3_LOGIC
VCCO_3 ALIAS 3V3_LOGIC
VCCO_4 ALIAS 3V3_LOGIC
VCCO_5 ALIAS 3V3_LOGIC
VCCO_6 ALIAS 3V3_LOGIC
VCCO_7 ALIAS 3V3_LOGIC
VCCAUX ALIAS 3V3_LOGIC
FPGA_CHIP_ID_F0<1> I273 GND_LOGIC
FPGA_CHIP_ID_F0<0> I274 GND_LOGIC
FPGA_CHIP_ID_F1<1> I275 GND_LOGIC
FPGA_CHIP_ID_F1<0> I276 3V3_LOGIC
12/2002
DENIS CALVET
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: DZERO L1 CAL RUN IIB
NUMERO CIRCUIT
ENSEMBLE: ADF BOARD
SOUS/ENS: FPGA #0,1 GND
NUMERO PLANCHE 15

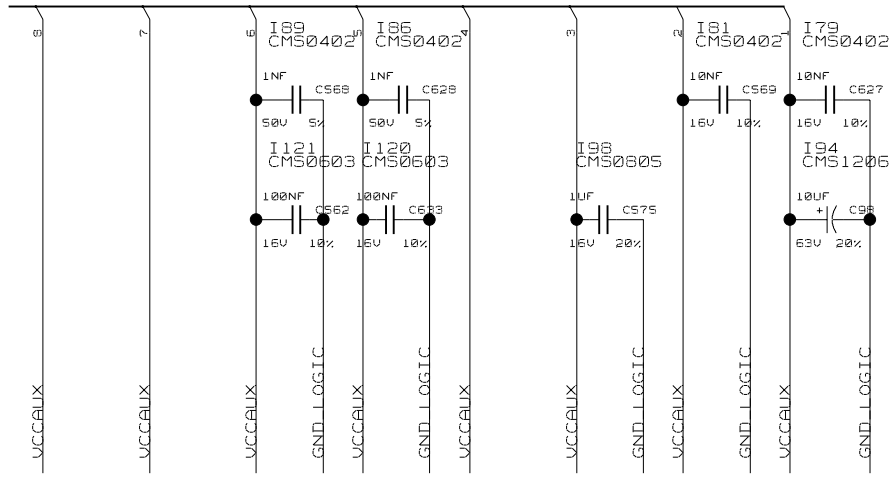


	12/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: FPGA #1 DECOUPLING		NUMERO PLANCHE 16

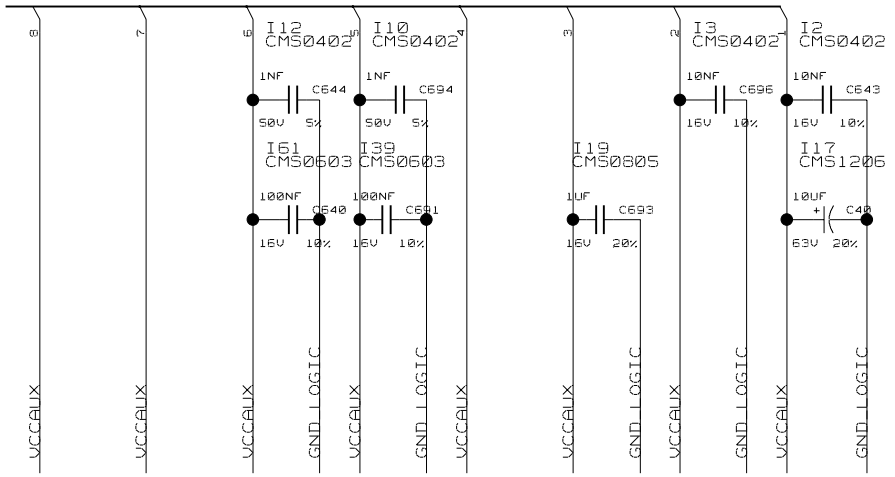


	12/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: FPGA #2 DECOUPLING		NUMERO PLANCHE 18

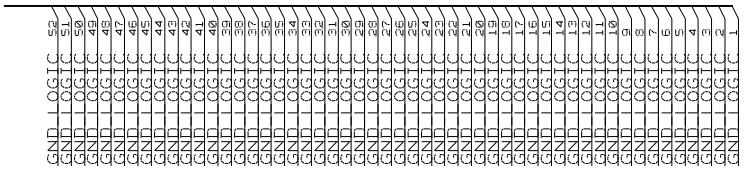
VCCAUX_F2<8..1>



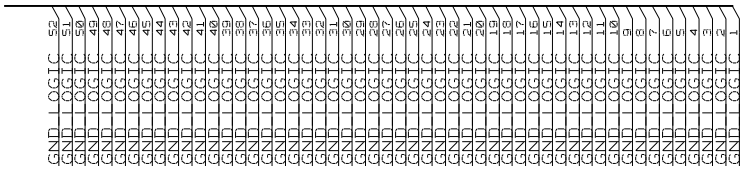
VCCAUX_F3<8..1>



GND_LOGIC_F2<52..1>



GND_LOGIC_F3<52..1>



I155

FPGA_CHIP_ID_F2<1> — 3V3_LOGIC

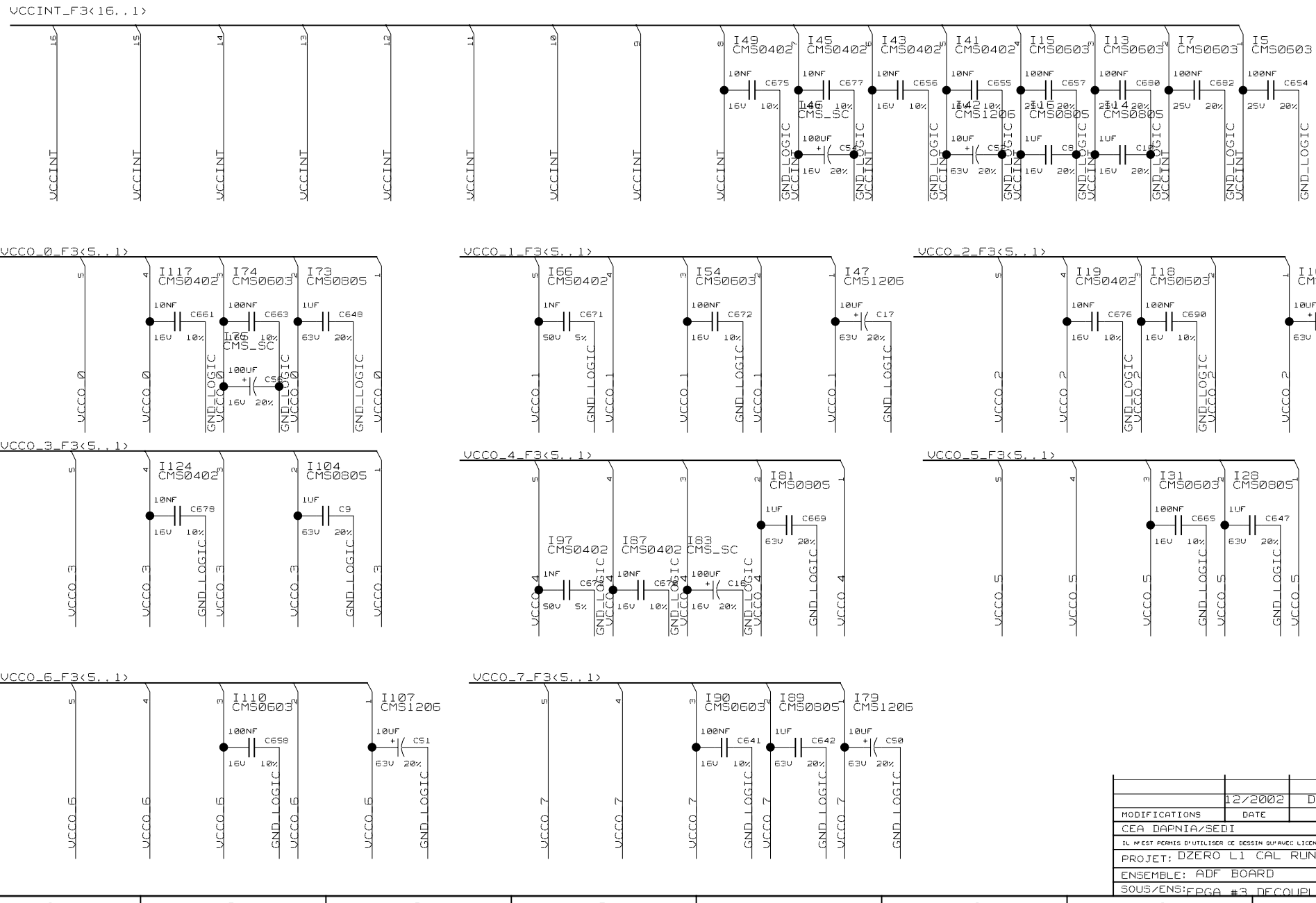
FPGA_CHIP_ID_F2<0> — GND_LOGIC

I157

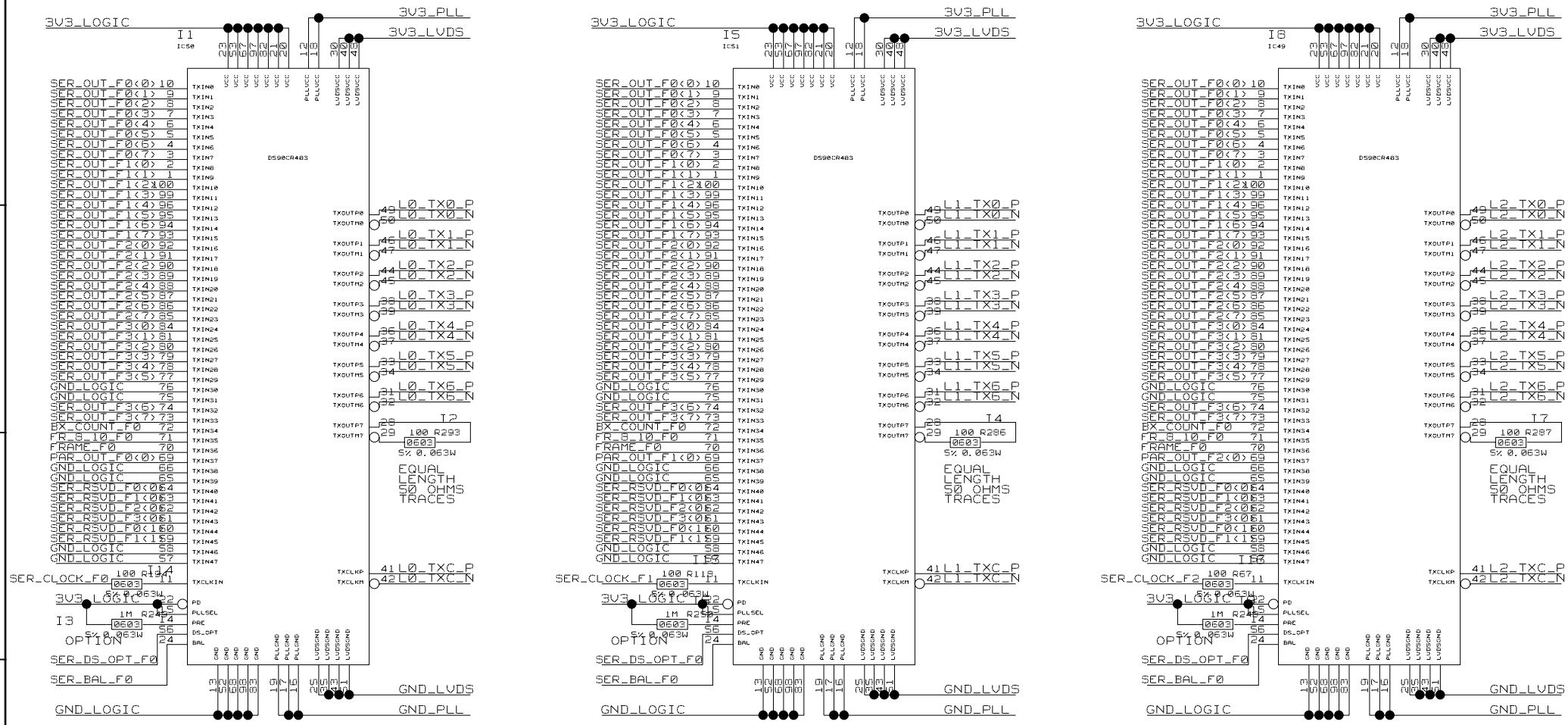
FPGA_CHIP_ID_F3<1> — 3V3_LOGIC

FPGA_CHIP_ID_F3<0> — 3V3_LOGIC

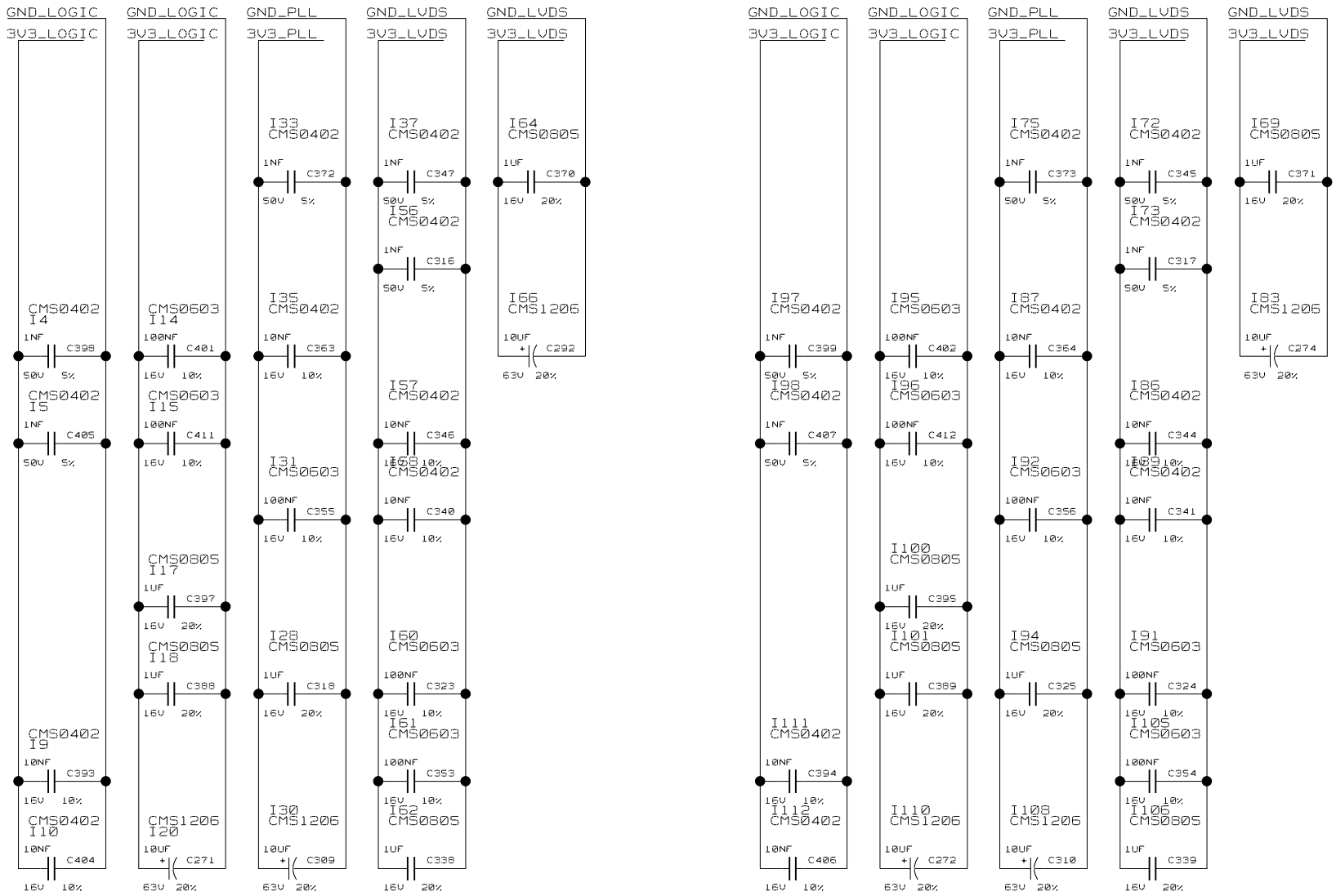
	12/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: FPGA #2,3 GND		NUMERO PLANCHE 19



	12/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: FPGA #3 DECOUPLING		NUMERO PLANCHE 20



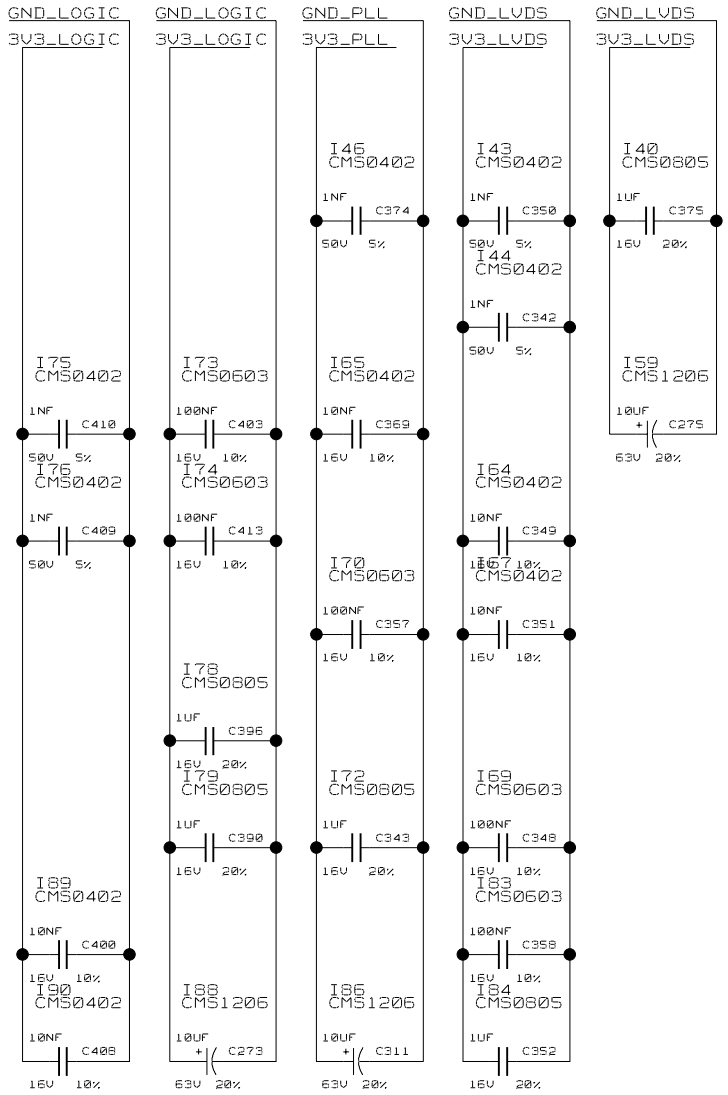
	12/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: OUTPUT LINK 0, 1, 2		NUMERO PLANCHE 22



DECOUPLING CHANNEL LINK #0

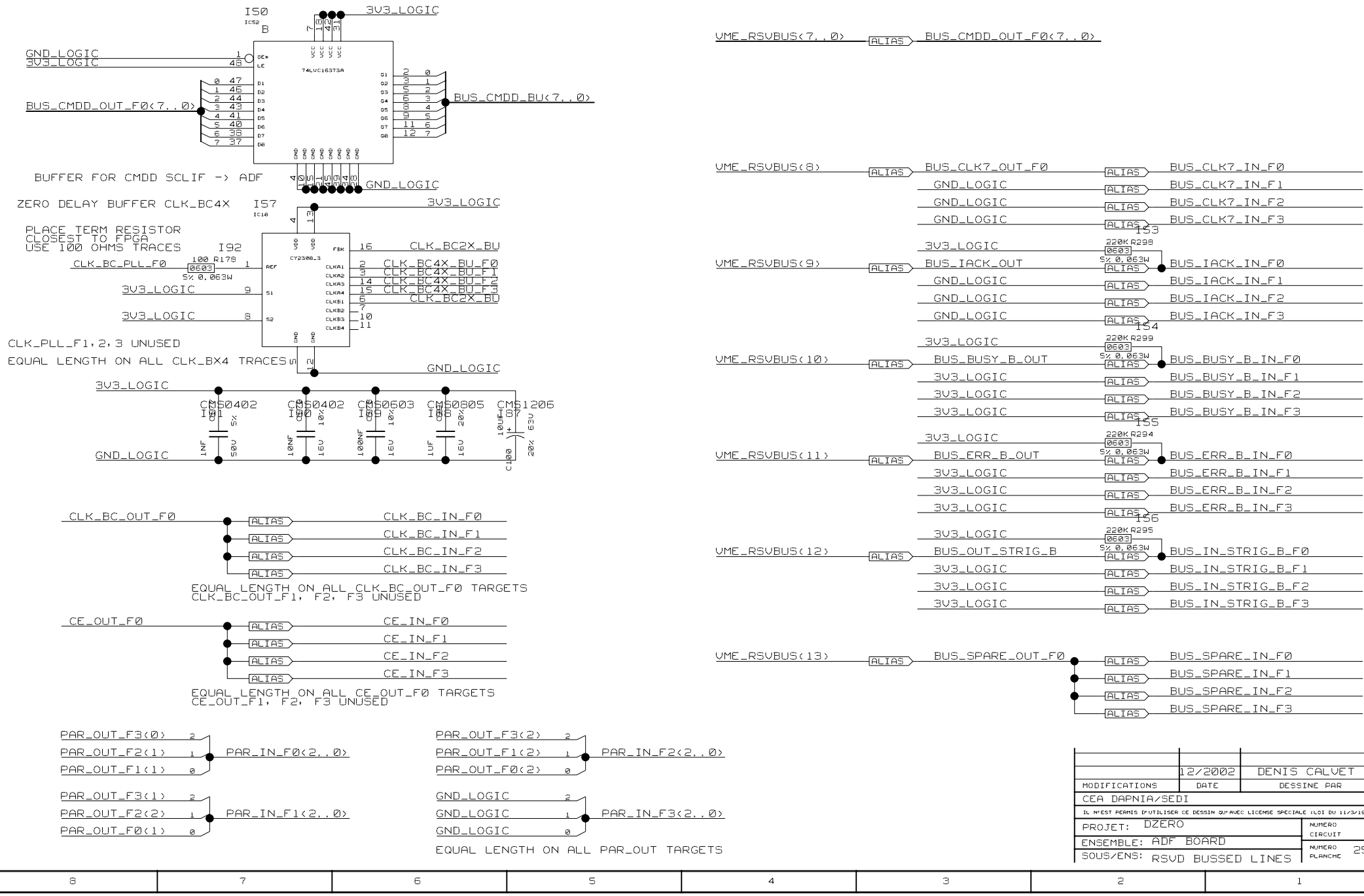
DECOUPLING CHANNEL LINK #1

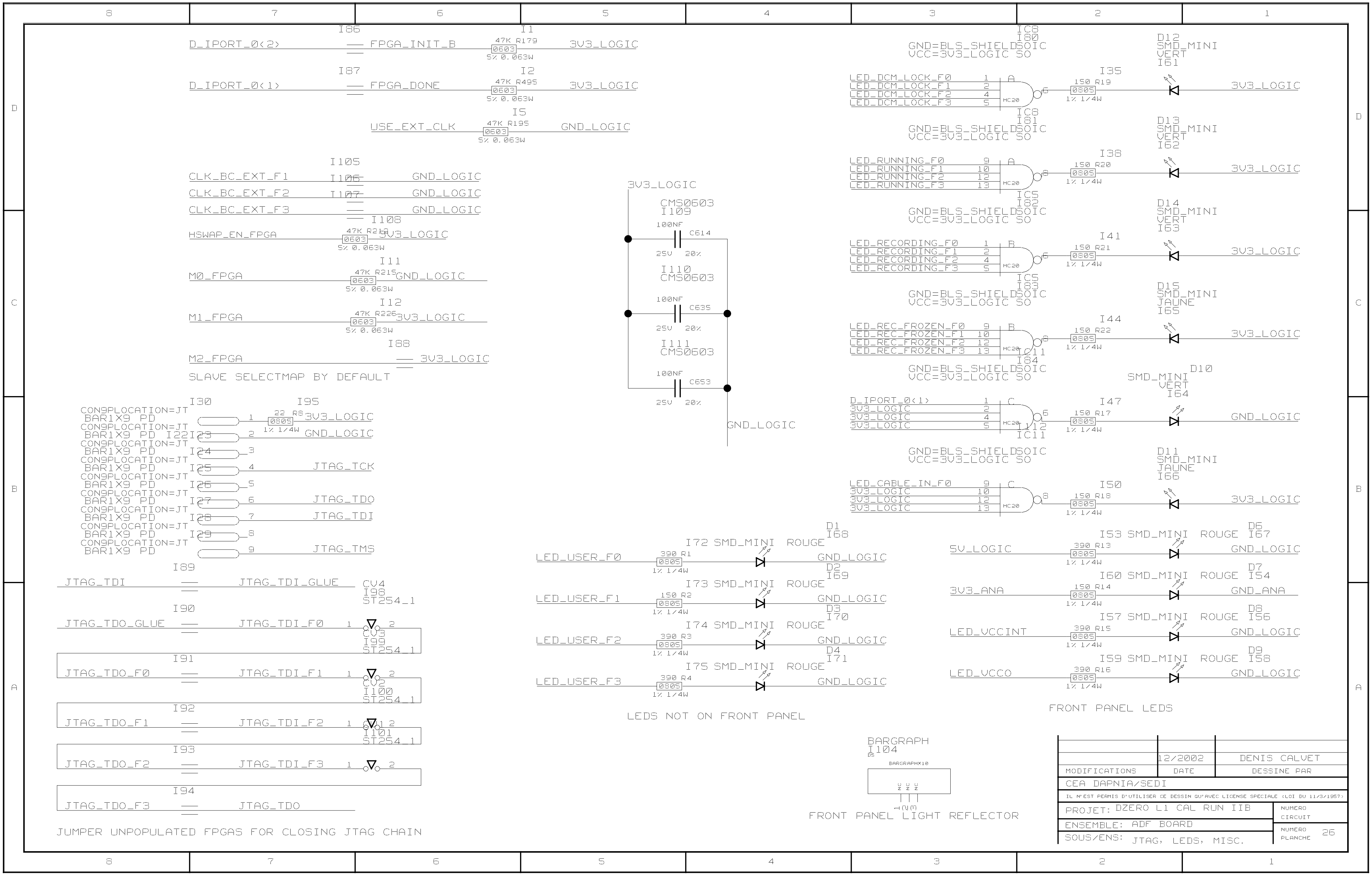
	12/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: CHAN LNK DECOUPLING		NUMERO PLANCHE 23

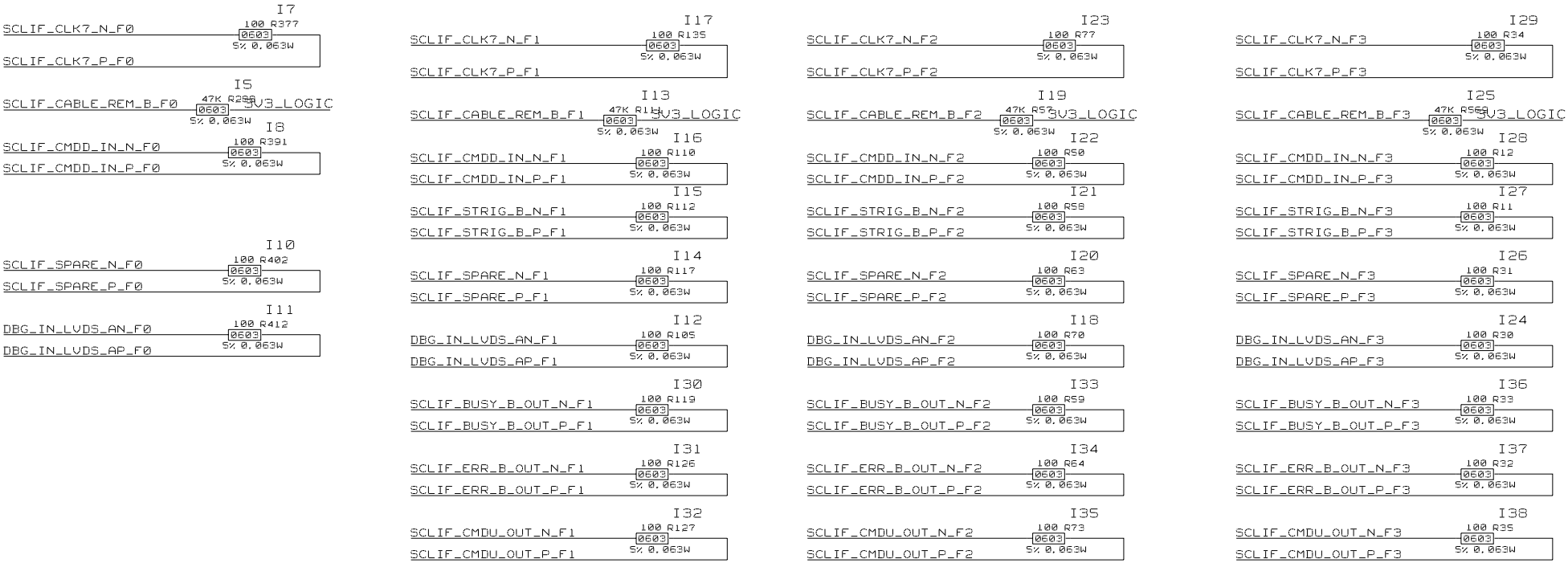


DECOUPLING CHANNEL LINK #2

	12/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: CHAN LNK DECOUPLING		NUMERO PLANCHE 24


I50
IC52
B
3V3_LOGIC
GND_LOGIC
3V3_LOGIC
74LVC16373A
BUS_CMDD_OUT_F0<7..0>
BUS_CMDD_BU<7..0>
BUFFER FOR CMDD SCLIF -> ADF
GND_LOGIC
ZERO DELAY BUFFER CLK_BC4X I57
IC16
3V3_LOGIC
PLACE TERM RESISTOR
CLOSEST TO FPGA
USE 100 OHMS TRACES I92
CLK_BC_PLL_F0
100 R178
0603
5% 0.063W
3V3_LOGIC
3V3_LOGIC
CY2308.3
CLK_BC2X_BU
CLK_BC4X_BU_F0
CLK_BC4X_BU_F1
CLK_BC4X_BU_F2
CLK_BC4X_BU_F3
CLK_BC2X_BU
CLK_PLL_F1,2,3 UNUSED
EQUAL LENGTH ON ALL CLK_BX4 TRACES
GND_LOGIC
3V3_LOGIC
C1 CM50402 1NF 5% 50V
C2 CM50402 10NF 10% 16V
C3 CM50603 100NF 10% 16V
C4 CM50805 1UF 20% 16V
C100 CM61206 10UF-H 20% 63V
GND_LOGIC
CLK_BC_OUT_F0
ALIAS
CLK_BC_IN_F0
CLK_BC_IN_F1
CLK_BC_IN_F2
CLK_BC_IN_F3
EQUAL LENGTH ON ALL CLK_BC_OUT_F0 TARGETS
CLK_BC_OUT_F1, F2, F3 UNUSED
CE_OUT_F0
CE_IN_F0
CE_IN_F1
CE_IN_F2
CE_IN_F3
EQUAL LENGTH ON ALL CE_OUT_F0 TARGETS
CE_OUT_F1, F2, F3 UNUSED
PAR_OUT_F3<0>
PAR_OUT_F2<1>
PAR_OUT_F1<1>
PAR_IN_F0<2..0>
PAR_OUT_F3<1>
PAR_OUT_F2<2>
PAR_OUT_F0<1>
PAR_IN_F1<2..0>
PAR_OUT_F3<2>
PAR_OUT_F1<2>
PAR_OUT_F0<2>
PAR_IN_F2<2..0>
GND_LOGIC
GND_LOGIC
GND_LOGIC
PAR_IN_F3<2..0>
EQUAL LENGTH ON ALL PAR_OUT TARGETS
VME_RSVBUS<7..0>
ALIAS
BUS_CMDD_OUT_F0<7..0>
VME_RSVBUS<8>
BUS_CLK7_OUT_F0
BUS_CLK7_IN_F0
GND_LOGIC
BUS_CLK7_IN_F1
GND_LOGIC
BUS_CLK7_IN_F2
GND_LOGIC
BUS_CLK7_IN_F3
I53
VME_RSVBUS<9>
3V3_LOGIC
220K R298
0603
5% 0.063W
BUS_IACK_OUT
BUS_IACK_IN_F0
GND_LOGIC
BUS_IACK_IN_F1
GND_LOGIC
BUS_IACK_IN_F2
GND_LOGIC
BUS_IACK_IN_F3
I54
VME_RSVBUS<10>
3V3_LOGIC
220K R299
0603
5% 0.063W
BUS_BUSY_B_OUT
BUS_BUSY_B_IN_F0
3V3_LOGIC
BUS_BUSY_B_IN_F1
3V3_LOGIC
BUS_BUSY_B_IN_F2
3V3_LOGIC
BUS_BUSY_B_IN_F3
I55
VME_RSVBUS<11>
3V3_LOGIC
220K R294
0603
5% 0.063W
BUS_ERR_B_OUT
BUS_ERR_B_IN_F0
3V3_LOGIC
BUS_ERR_B_IN_F1
3V3_LOGIC
BUS_ERR_B_IN_F2
3V3_LOGIC
BUS_ERR_B_IN_F3
I56
VME_RSVBUS<12>
3V3_LOGIC
220K R295
0603
5% 0.063W
BUS_OUT_STRIG_B
BUS_IN_STRIG_B_F0
3V3_LOGIC
BUS_IN_STRIG_B_F1
3V3_LOGIC
BUS_IN_STRIG_B_F2
3V3_LOGIC
BUS_IN_STRIG_B_F3
VME_RSVBUS<13>
BUS_SPARE_OUT_F0
BUS_SPARE_IN_F0
BUS_SPARE_IN_F1
BUS_SPARE_IN_F2
BUS_SPARE_IN_F3
12/2002
DENIS CALVET
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: DZERO
NUMERO CIRCUIT
ENSEMBLE: ADF BOARD
SOUS/ENS: RSVD BUSSED LINES
NUMERO PLANCHE 25

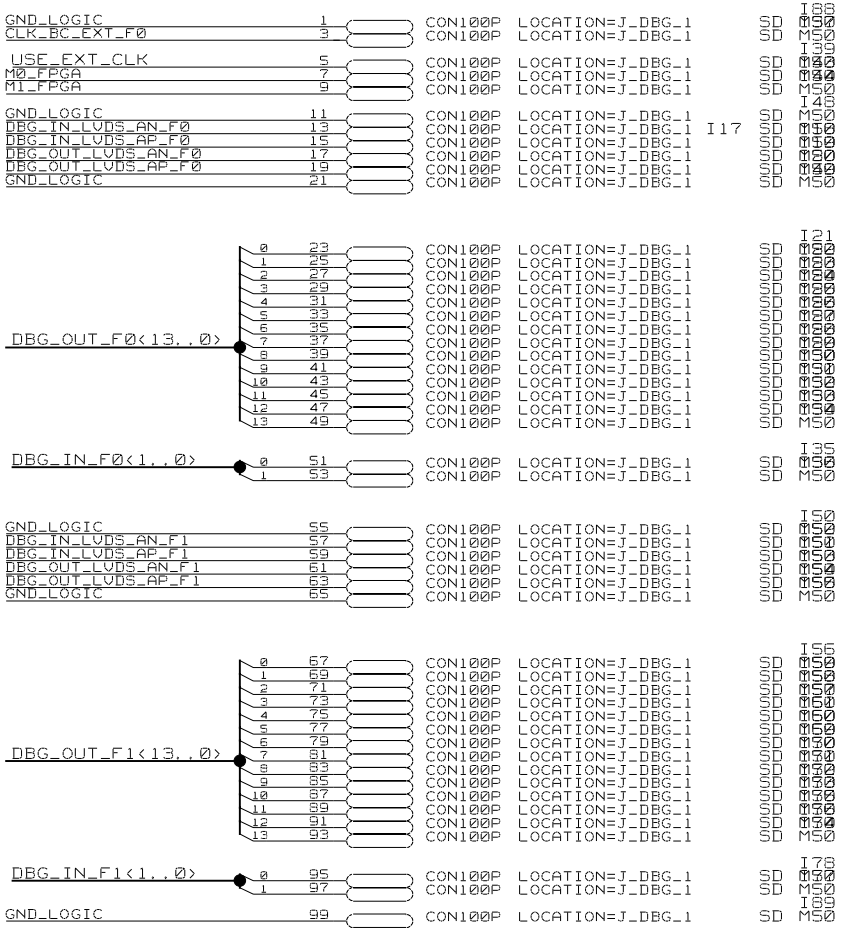

D_IPORT_0<2>
FPGA_INIT_B
3V3_LOGIC
D_IPORT_0<1>
FPGA_DONE
USE_EXT_CLK
GND_LOGIC
CLK_BC_EXT_F1
CLK_BC_EXT_F2
CLK_BC_EXT_F3
HSWAP_EN_FPGA
M0_FPGA
M1_FPGA
M2_FPGA
SLAVE SELECTMAP BY DEFAULT
JTAG_TCK
JTAG_TDO
JTAG_TDI
JTAG_TMS
JTAG_TDI_GLUE
JTAG_TDO_GLUE
JTAG_TDI_F0
JTAG_TDO_F0
JTAG_TDI_F1
JTAG_TDO_F1
JTAG_TDI_F2
JTAG_TDO_F2
JTAG_TDI_F3
JTAG_TDO_F3
JUMPER UNPOPULATED FPGAS FOR CLOSING JTAG CHAIN
GND=BLS_SHIELDSOIC
VCC=3V3_LOGIC SO
LED_DCM_LOCK_F0
LED_DCM_LOCK_F1
LED_DCM_LOCK_F2
LED_DCM_LOCK_F3
LED_RUNNING_F0
LED_RUNNING_F1
LED_RUNNING_F2
LED_RUNNING_F3
LED_RECORDING_F0
LED_RECORDING_F1
LED_RECORDING_F2
LED_RECORDING_F3
LED_REC_FROZEN_F0
LED_REC_FROZEN_F1
LED_REC_FROZEN_F2
LED_REC_FROZEN_F3
LED_CABLE_IN_F0
SMD_MINI
VERT
JAUNE
ROUGE
LED_USER_F0
LED_USER_F1
LED_USER_F2
LED_USER_F3
LEDS NOT ON FRONT PANEL
5V_LOGIC
3V3_ANA
GND_ANA
LED_VCCINT
LED_VCCO
FRONT PANEL LEDS
BARGRAPH
I104
FRONT PANEL LIGHT REFLECTOR
12/2002
DENIS CALVET
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: DZERO L1 CAL RUN IIB
ENSEMBLE: ADF BOARD
SOUS/ENS: JTAG, LEDS, MISC.
NUMERO CIRCUIT
NUMERO PLANCHE 26



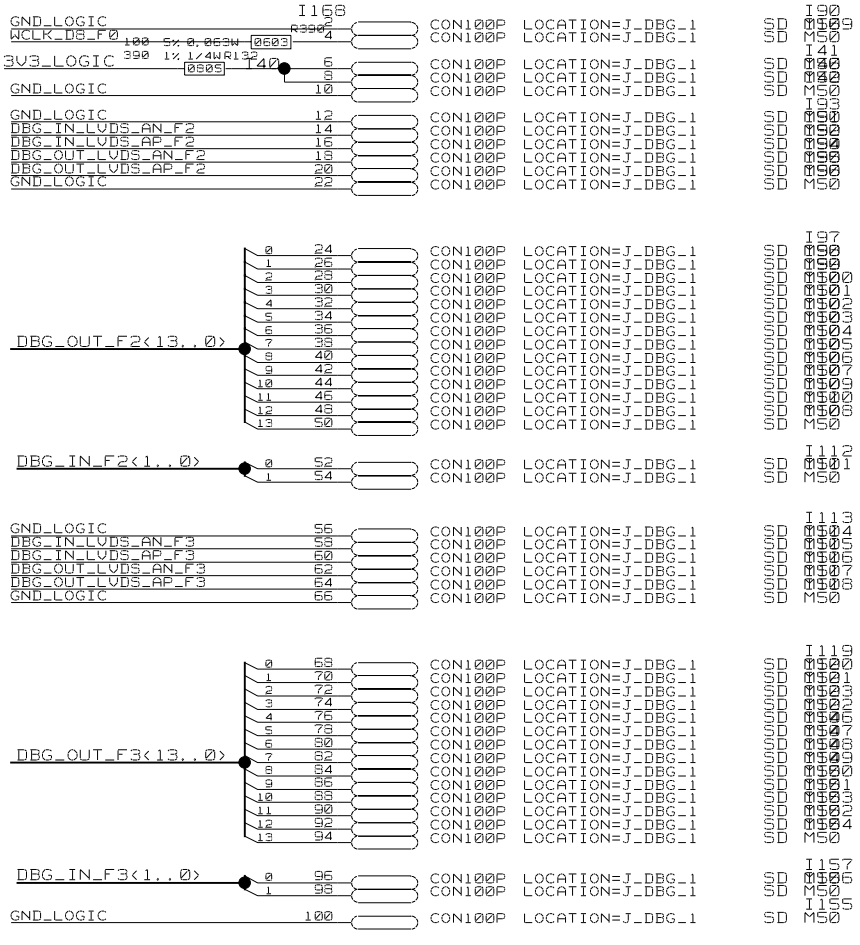
50 OHMS TRACES ON ALL SCLIF TRACES EXCEPT SCLIF_CABLE_LOC_B AND SCLIF_CABLE_REM_B
SCLIF SIGNALS _F1, _F2, _F3 UNUSED

	12/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: SCLIF CABLE		NUMERO PLANCHE 27

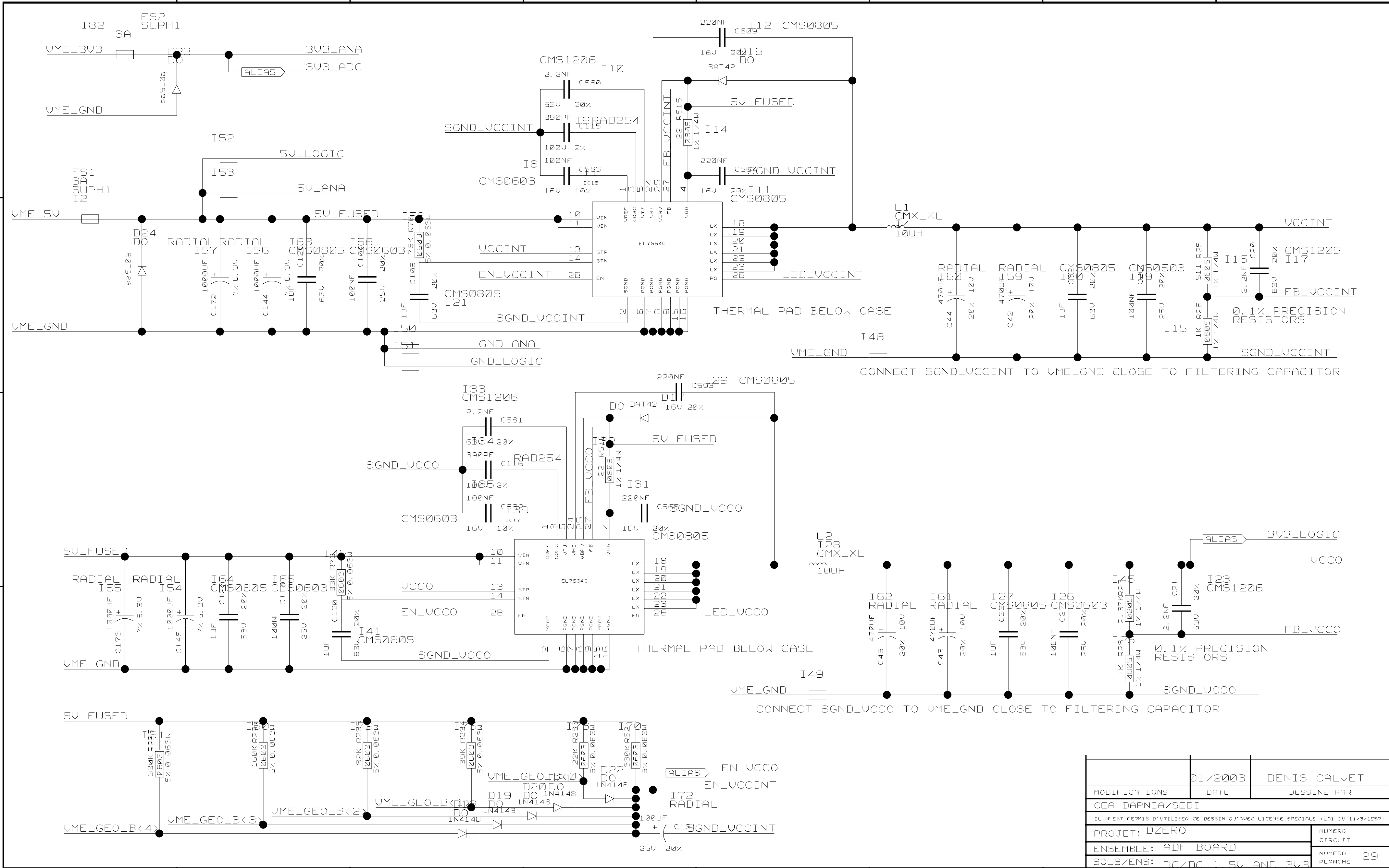
SET USE_EXT_CLK TO 3V3 TO USE EXTERNAL CLOCK
PROVIDE EXTERNAL CLOCK ON CLK_BC_EXT_F0 OR WIRE TO WCLK_D8_F0
PULL UP M0 AND DOWN M1 FOR CONFIGURATION BY JTAG



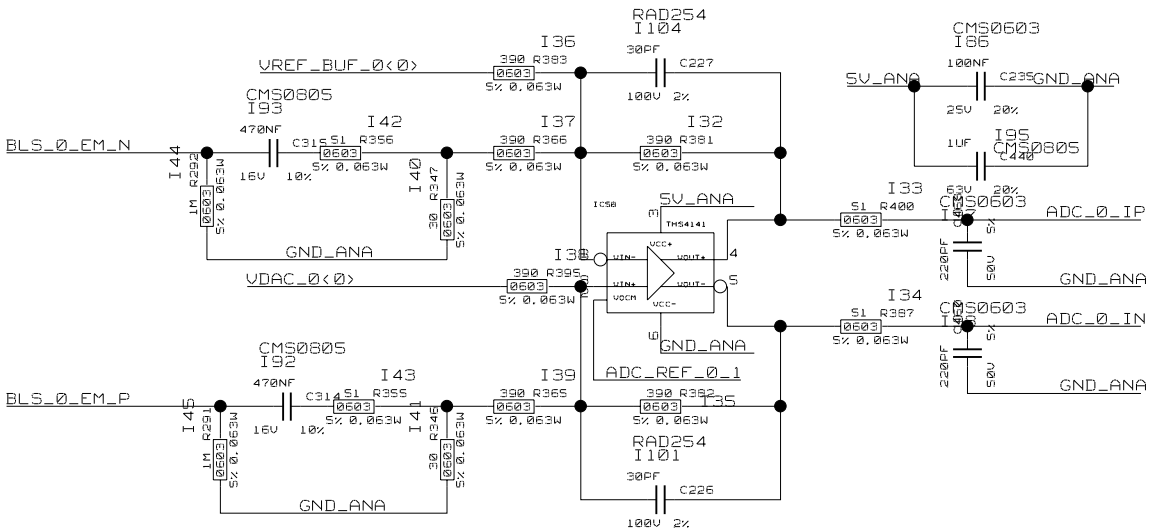
PLACE TERM RESISTOR
CLOSESTEST TO FPGA
USE 100 OHMS TRACES

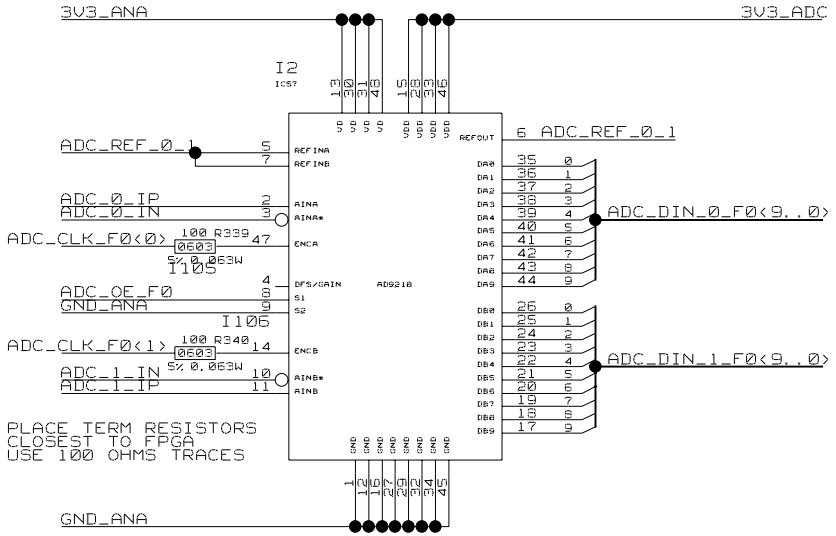


	12/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: DEBUG CONNECTOR		NUMERO PLANCHE 28

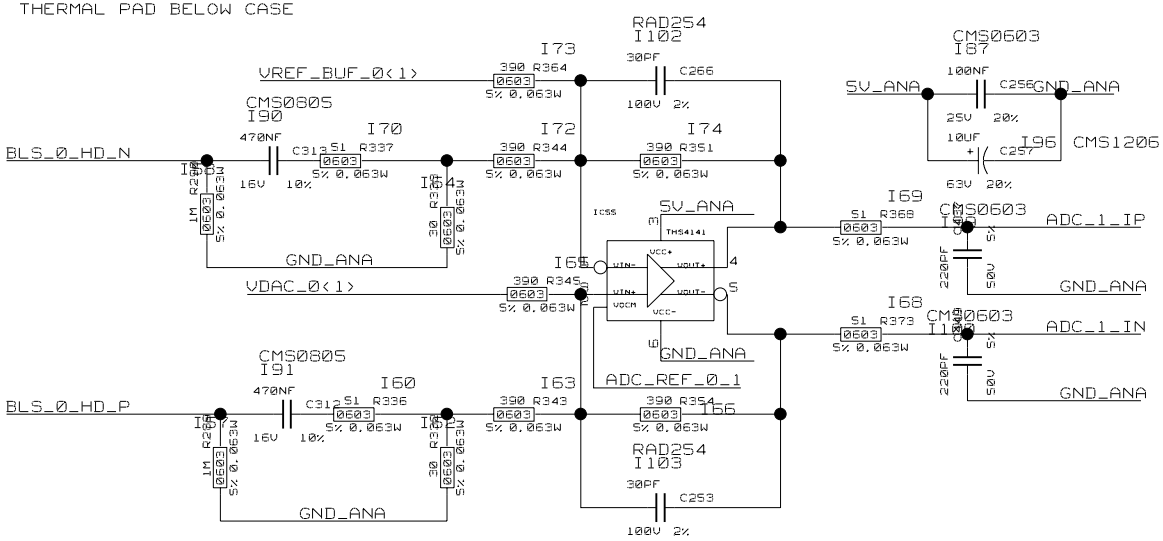


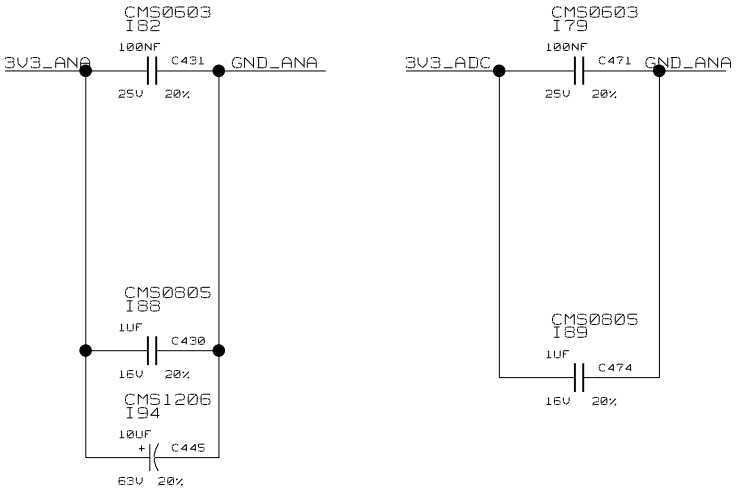
CONNECT SGND_VCCINT TO VME_GND CLOSE TO FILTERING CAPACITOR
CONNECT SGND_VCCO TO VME_GND CLOSE TO FILTERING CAPACITOR
THERMAL PAD BELOW CASE
0.1% PRECISION RESISTORS
EL7564C
MODIFICATIONS
01/2003
DATE
DENIS CALVET
DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: DZERO
ENSEMBLE: ADF BOARD
SOUS/ENS: DC/DC 1.5V AND 3V3
NUMERO CIRCUIT
NUMERO PLANCHE 29



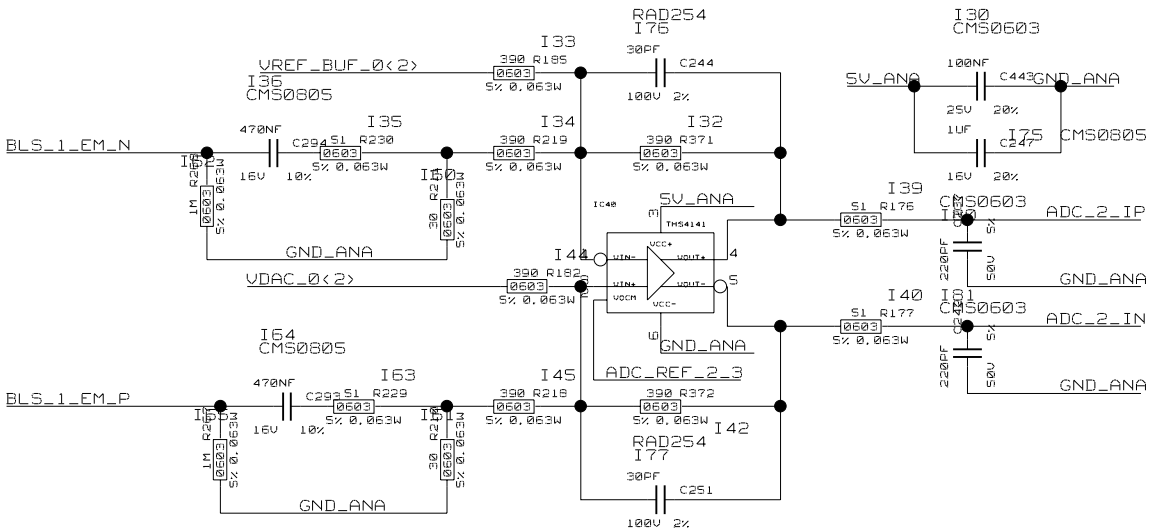


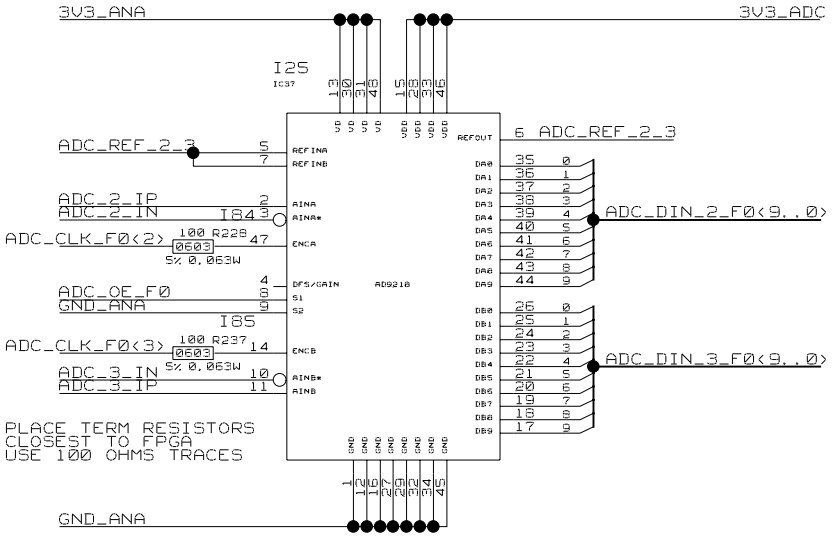
79 OHMS TRACES ON ALL BLS_ SIGNALS
MATCH LENGTH OF _P AND _N SIGNAL TRACES
THERMAL PAD BELOW CASE



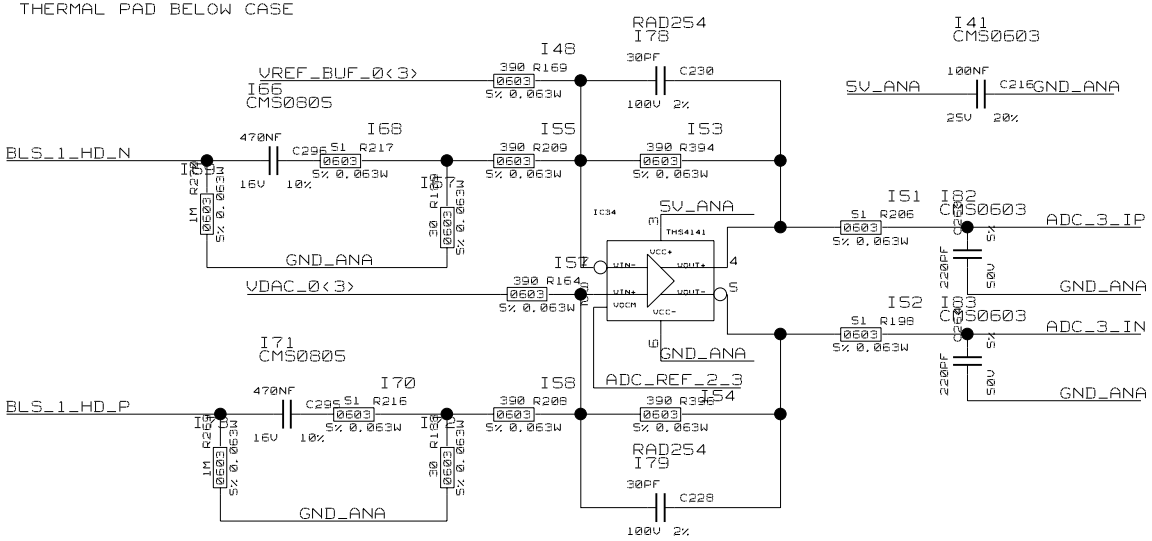


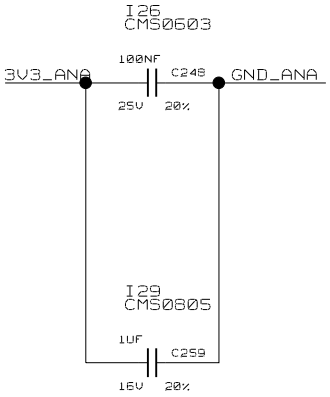
	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: ADC CHANNEL 0-1		NUMERO PLANCHE 40

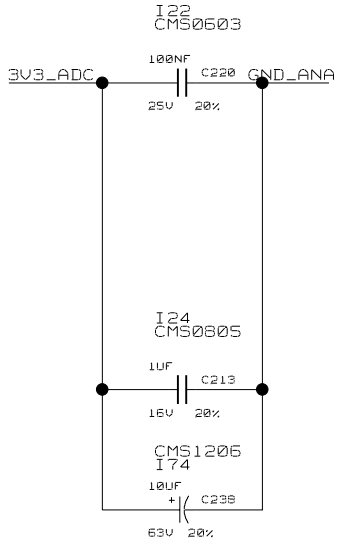




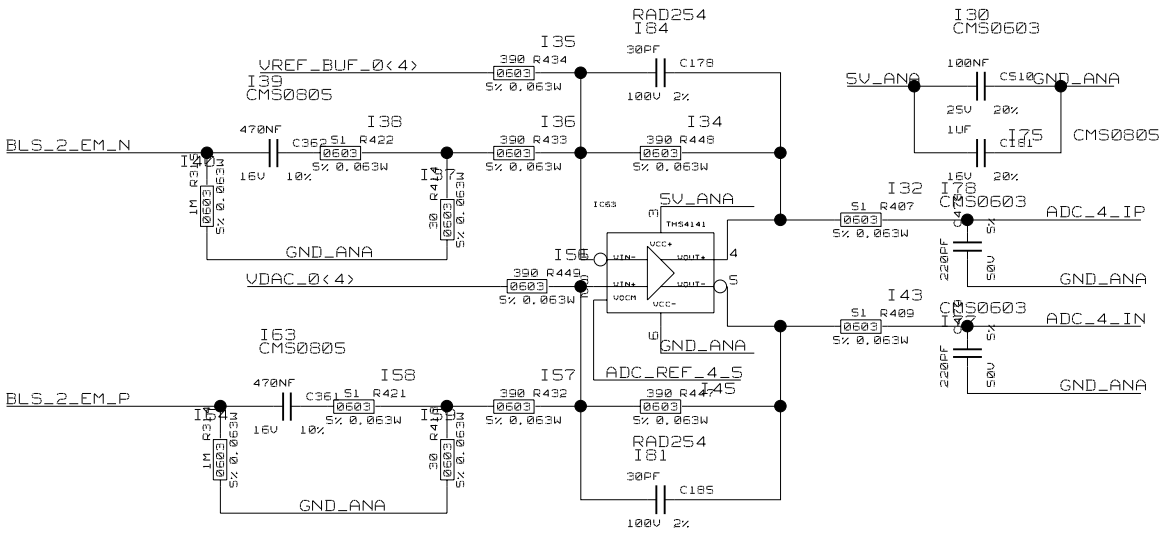
79 OHMS TRACES ON ALL BLS_ SIGNALS
MATCH LENGTH OF _P AND _N SIGNAL TRACES
THERMAL PAD BELOW CASE

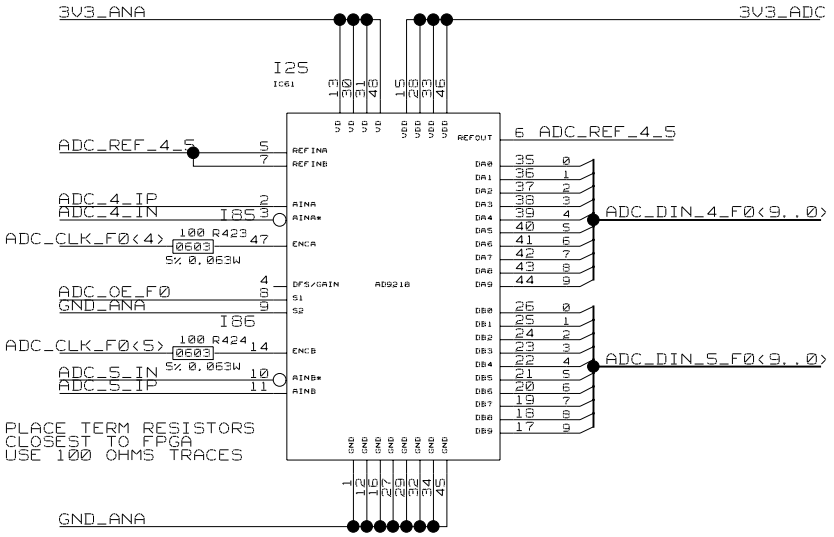




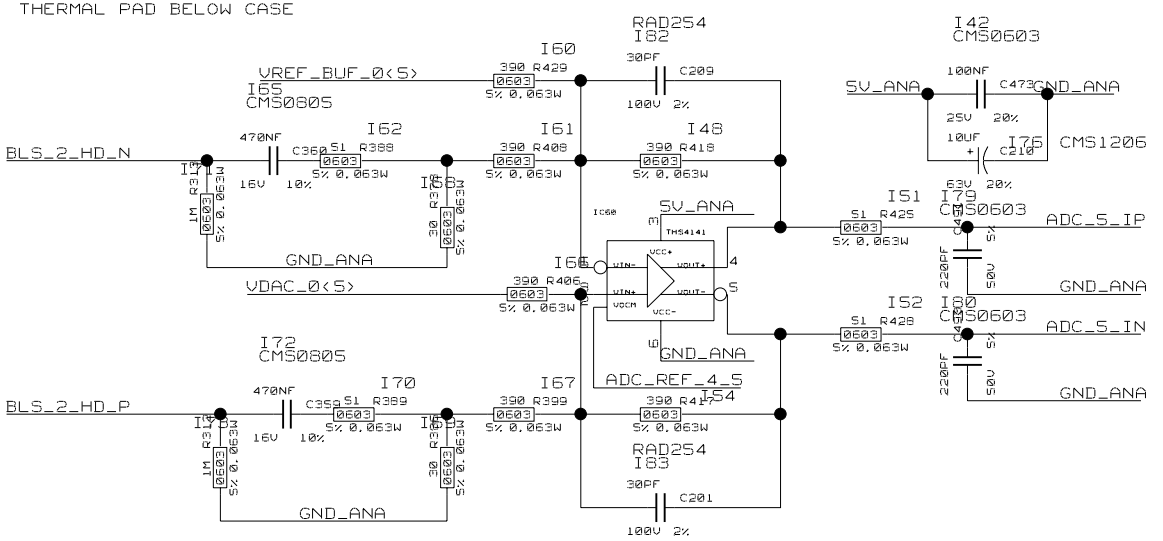


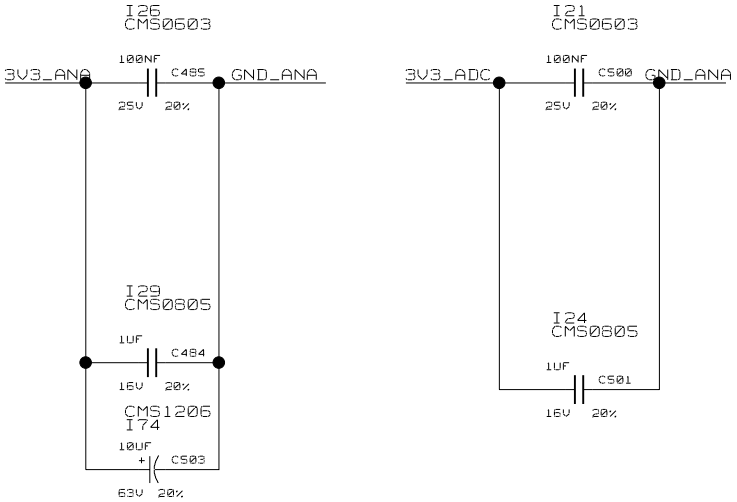
	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: ADC CHANNEL 2-3		NUMERO PLANCHE 41



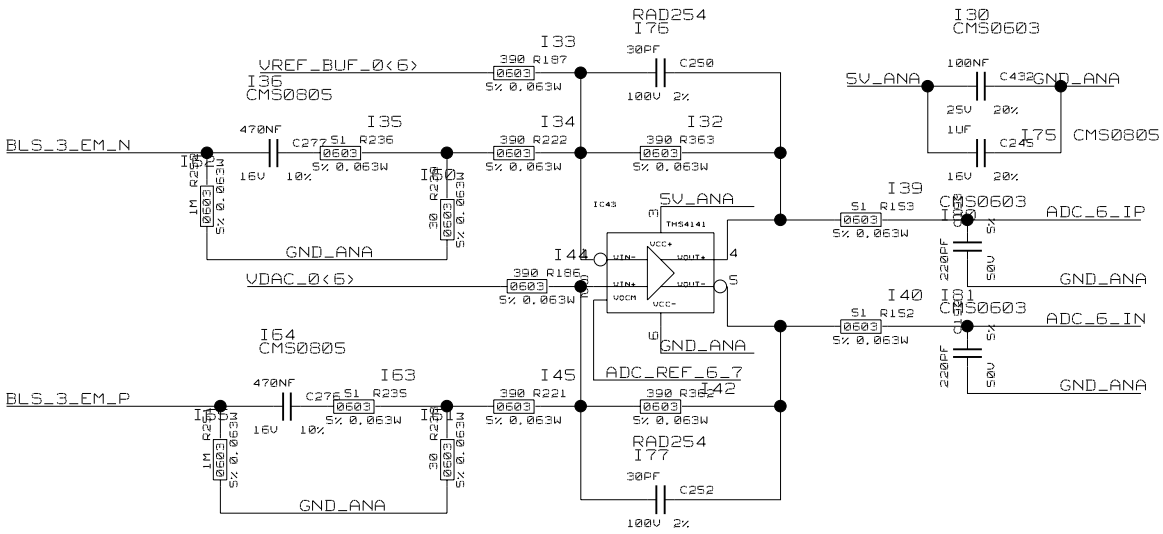


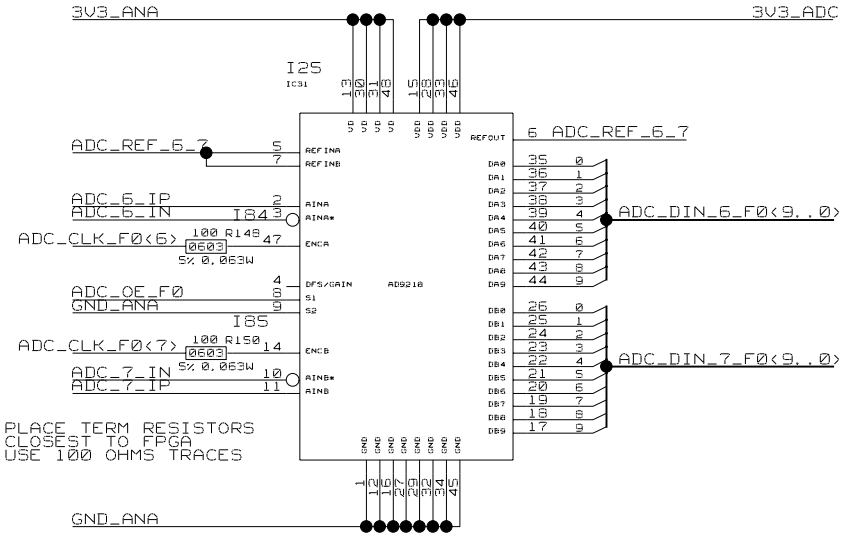
79 OHMS TRACES ON ALL BLS_ SIGNALS
MATCH LENGTH OF _P AND _N SIGNAL TRACES
THERMAL PAD BELOW CASE



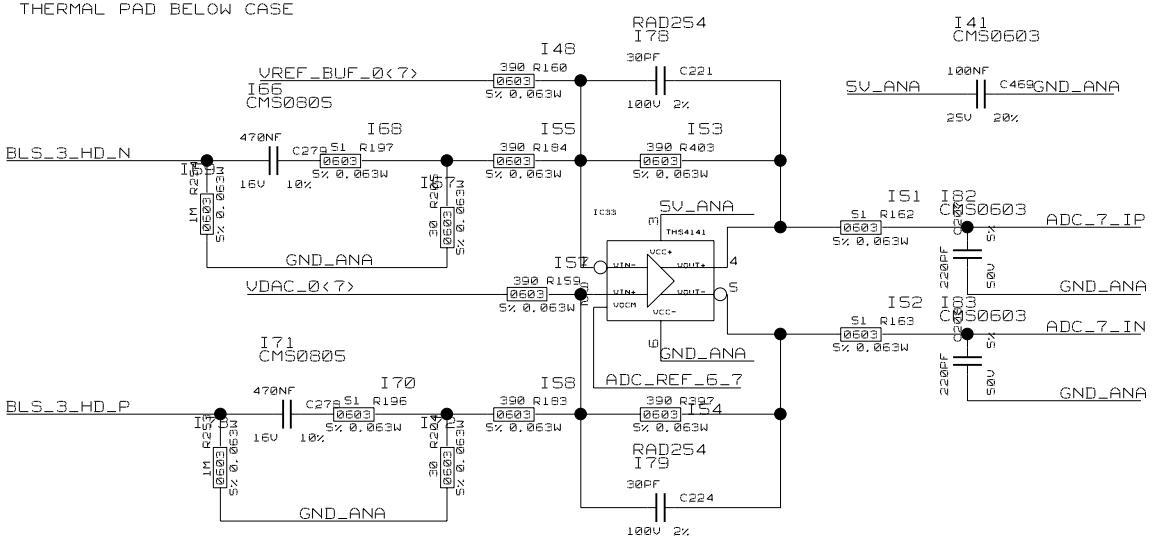


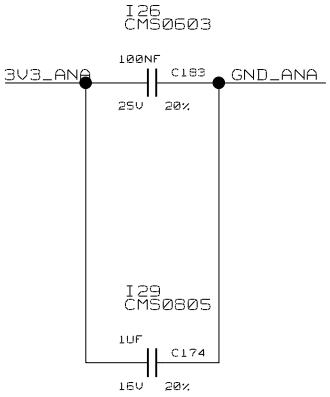
	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: ADC CHANNEL 4-5		NUMERO PLANCHE 42

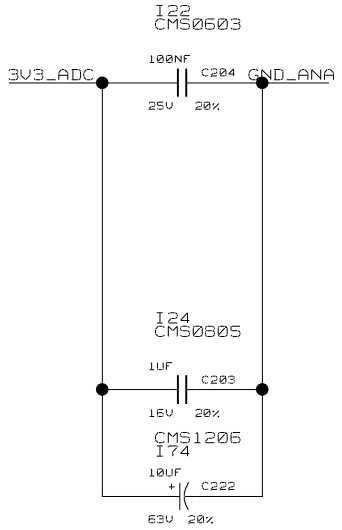




79 OHMS TRACES ON ALL BLS_ SIGNALS
MATCH LENGTH OF _P AND _N SIGNAL TRACES
THERMAL PAD BELOW CASE







	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR

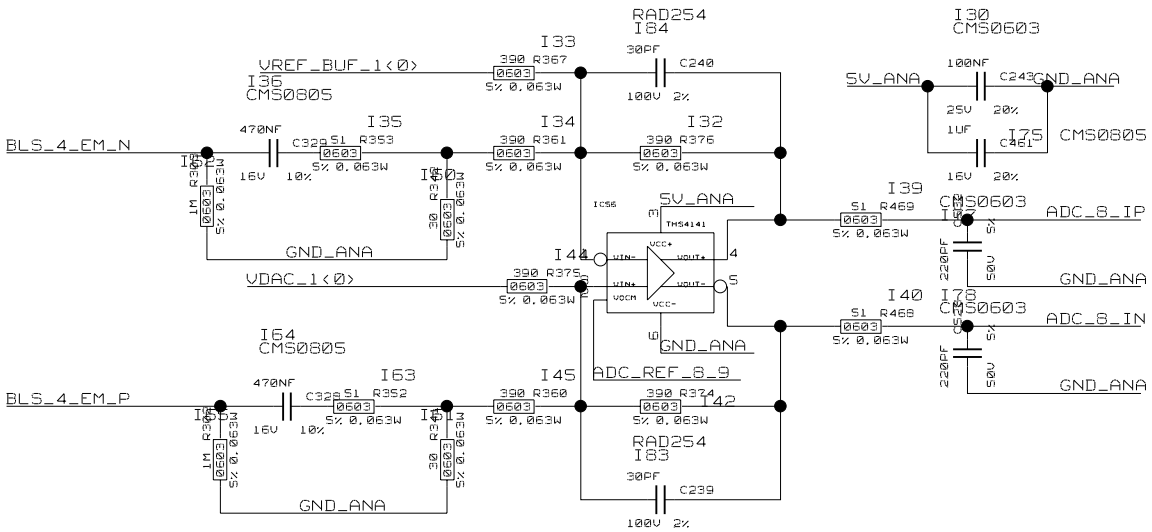
CEA DAPNIA/SEDI

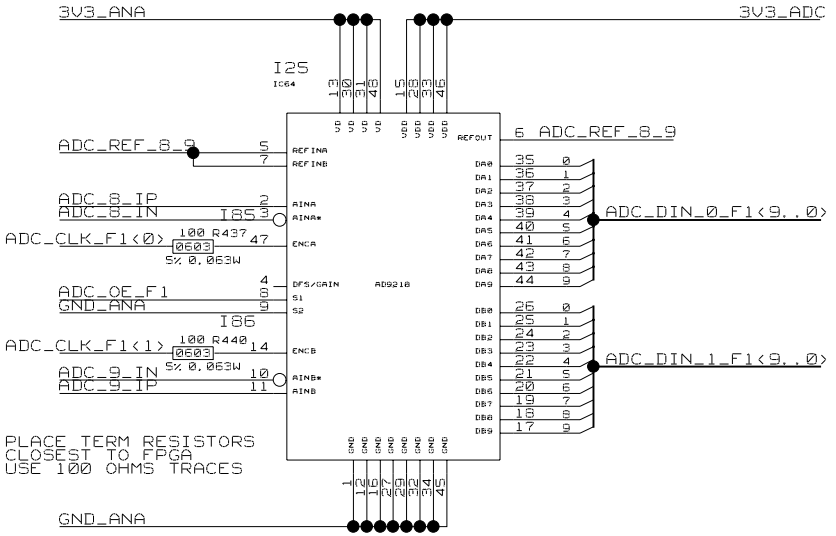
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)

PROJET: DZERO L1 CAL RUN IIB — NUMERO CIRCUIT

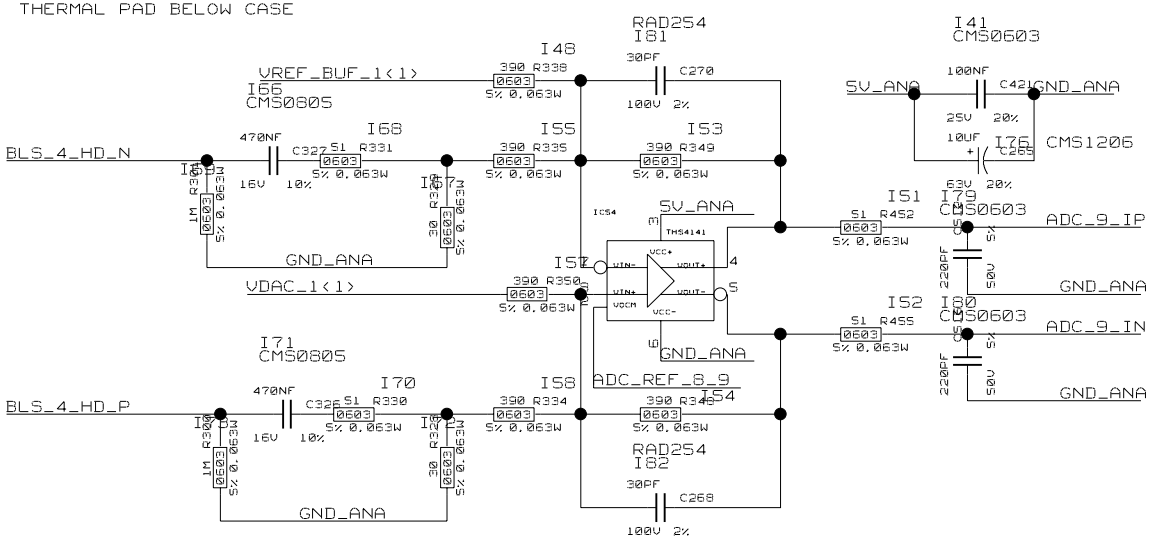
ENSEMBLE: ADF BOARD

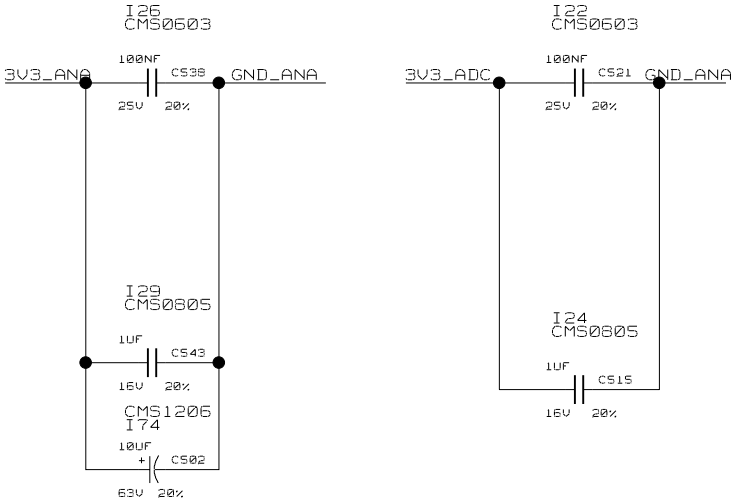
SOUS/ENS: ADC CHANNEL 6-7 — NUMERO PLANCHE 43



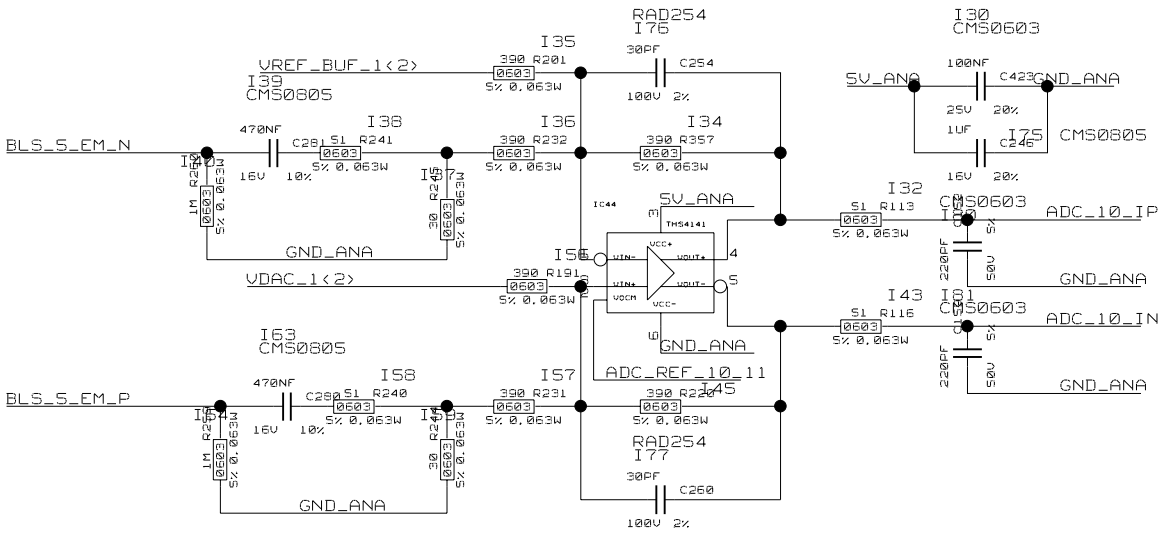


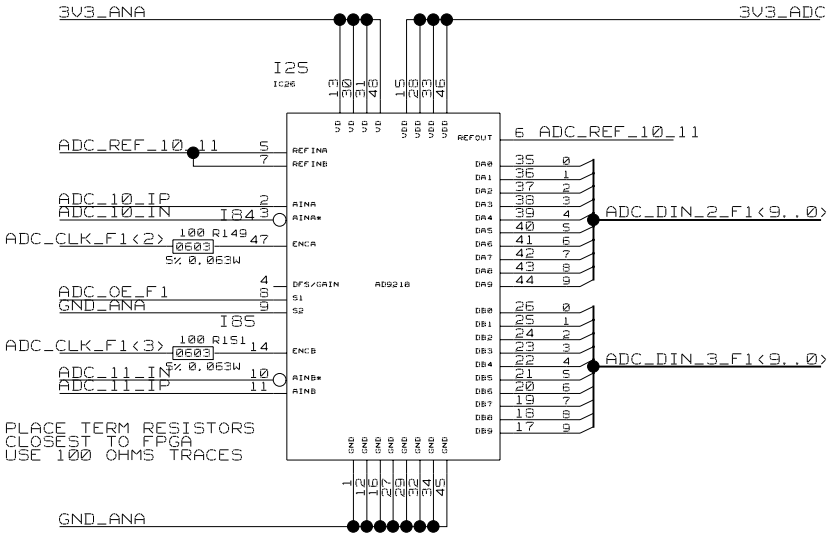
79 OHMS TRACES ON ALL BLS_ SIGNALS
MATCH LENGTH OF _P AND _N SIGNAL TRACES
THERMAL PAD BELOW CASE



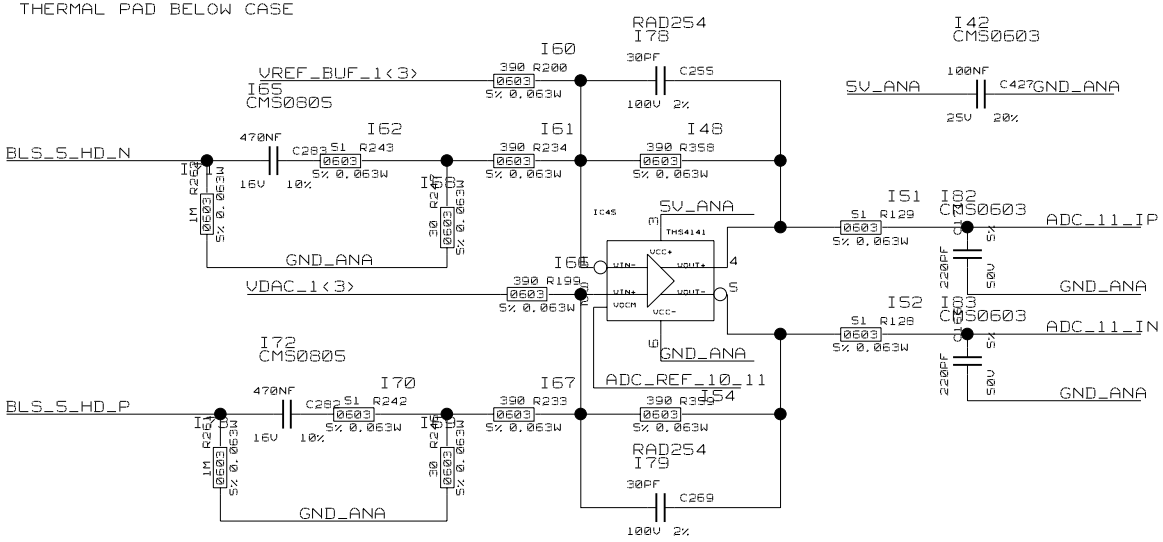


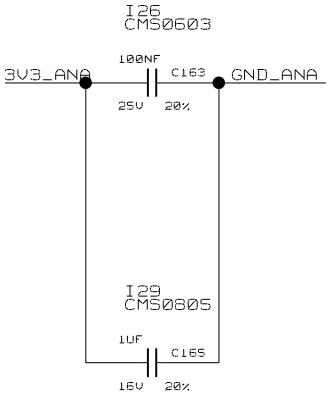
	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		NUMERO PLANCHE 44
SOUS/ENS: ADC CHANNEL 8-9		

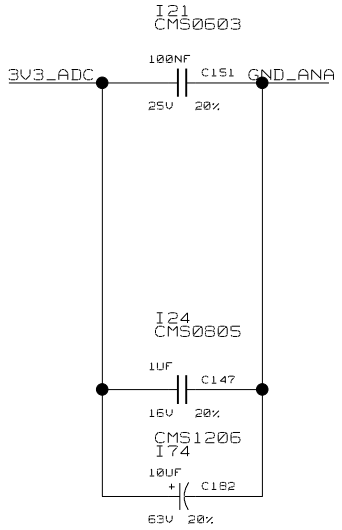




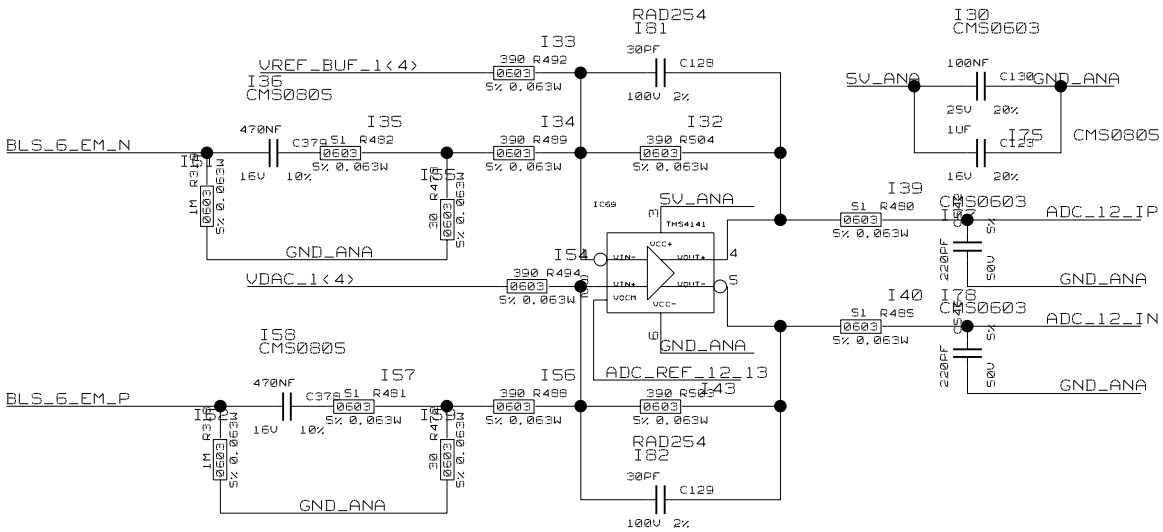
79 OHMS TRACES ON ALL BLS_ SIGNALS
MATCH LENGTH OF _P AND _N SIGNAL TRACES
THERMAL PAD BELOW CASE

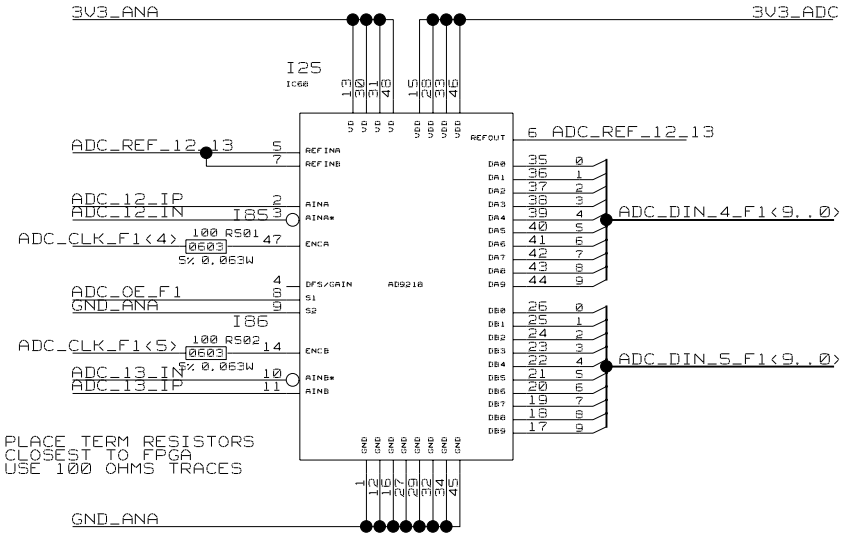




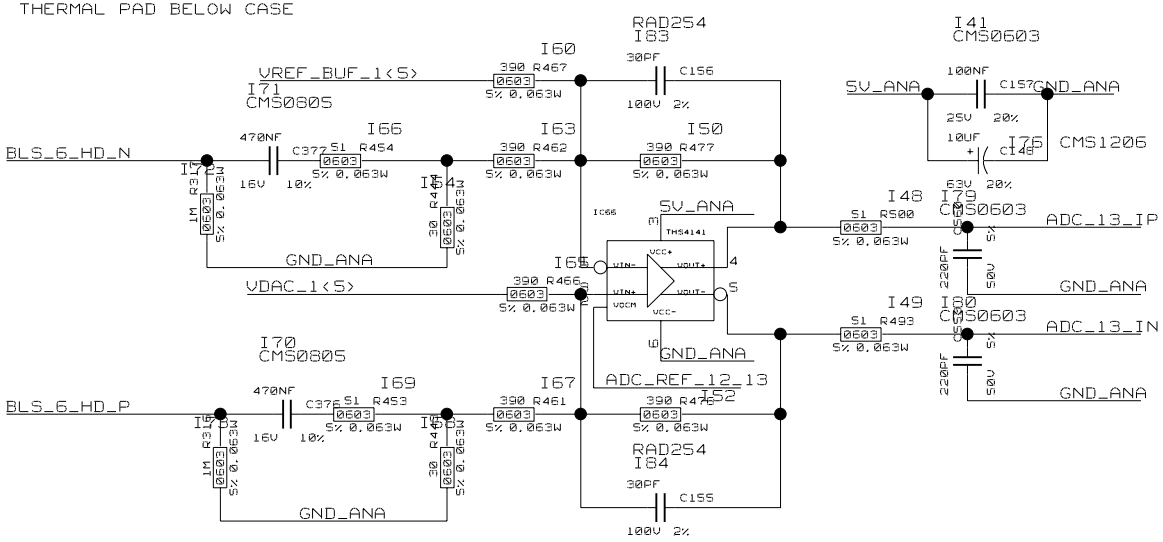


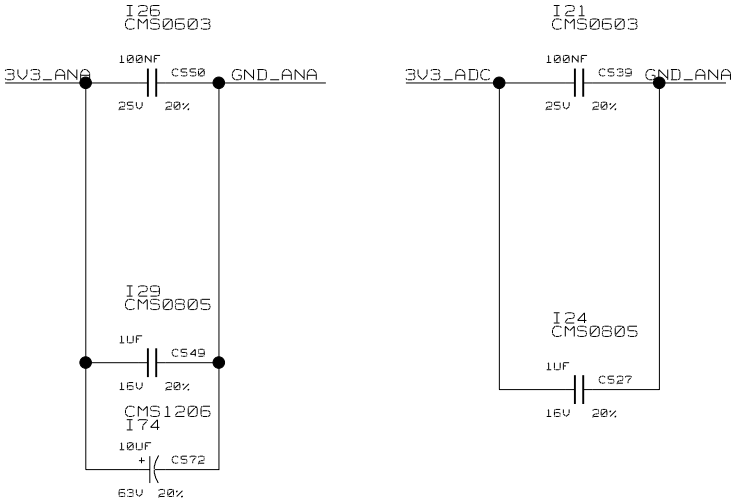
	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: ADC CHANNEL 10-11		NUMERO PLANCHE 45



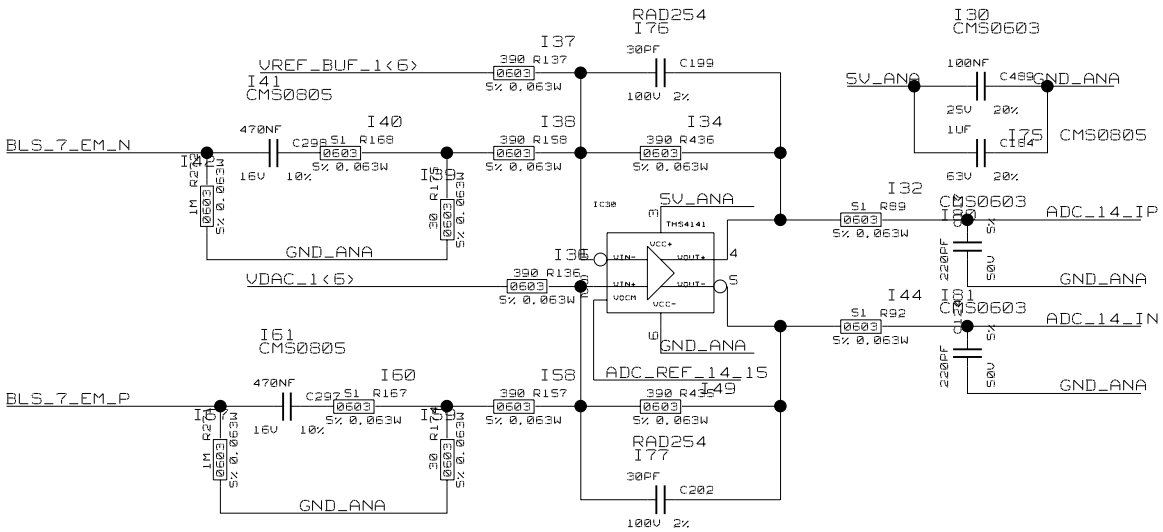


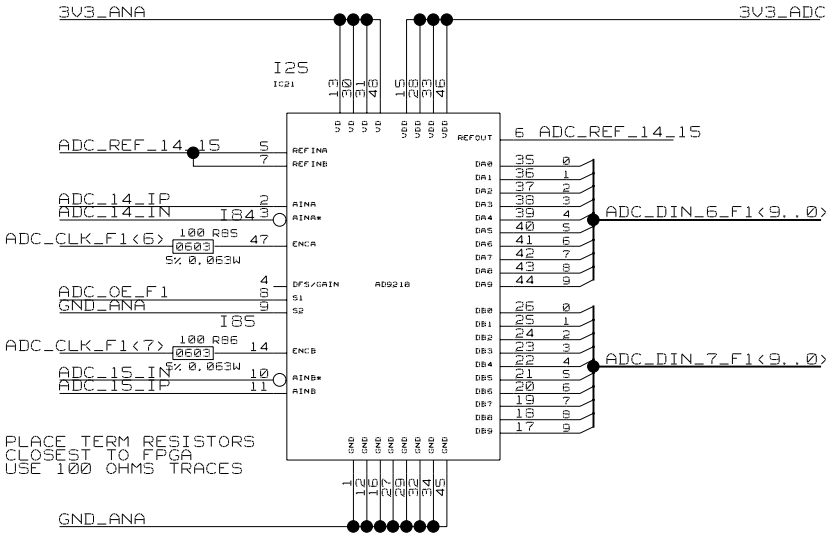
79 OHMS TRACES ON ALL BLS_ SIGNALS
MATCH LENGTH OF _P AND _N SIGNAL TRACES
THERMAL PAD BELOW CASE



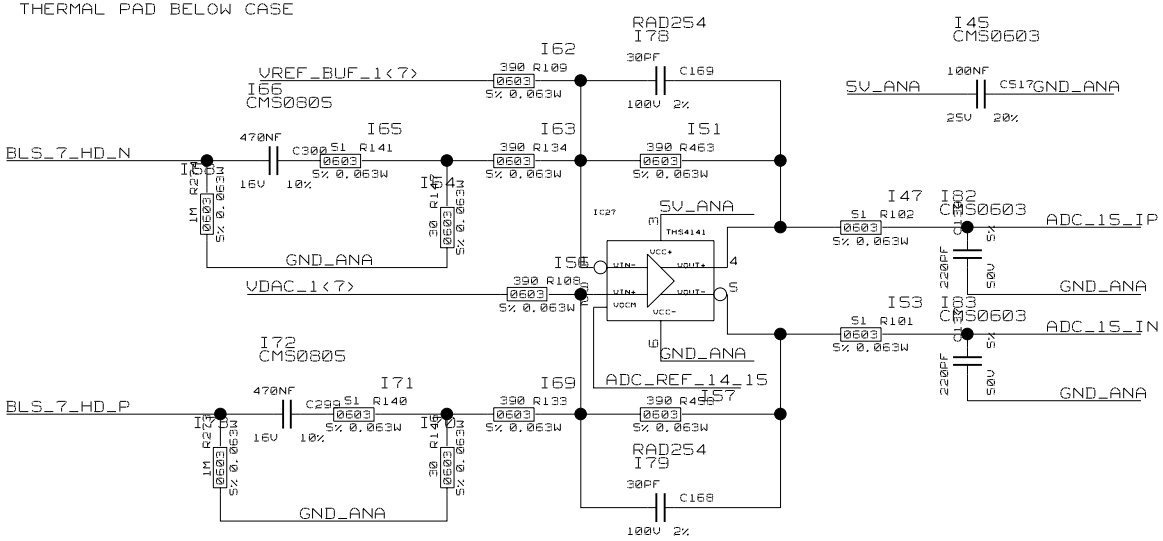


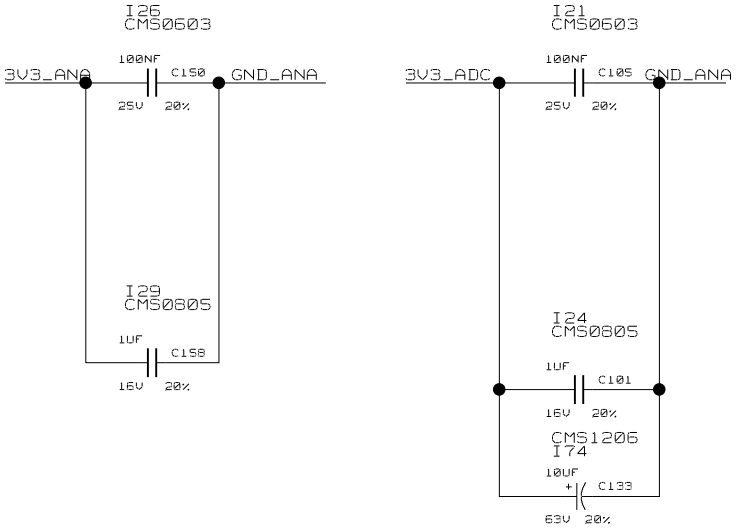
	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: ADC CHANNEL 12-13		NUMERO PLANCHE 46



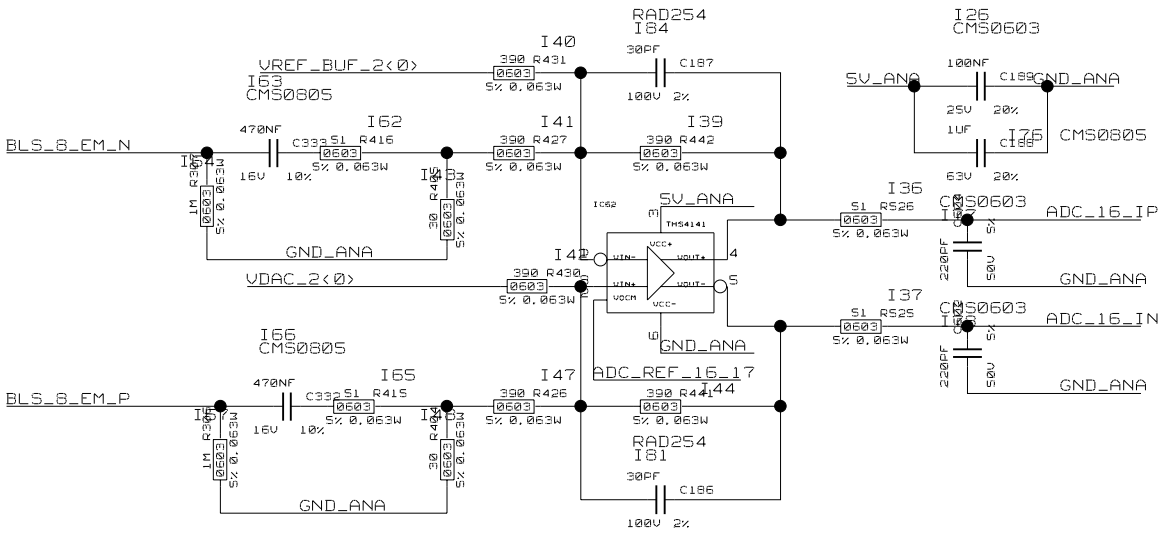


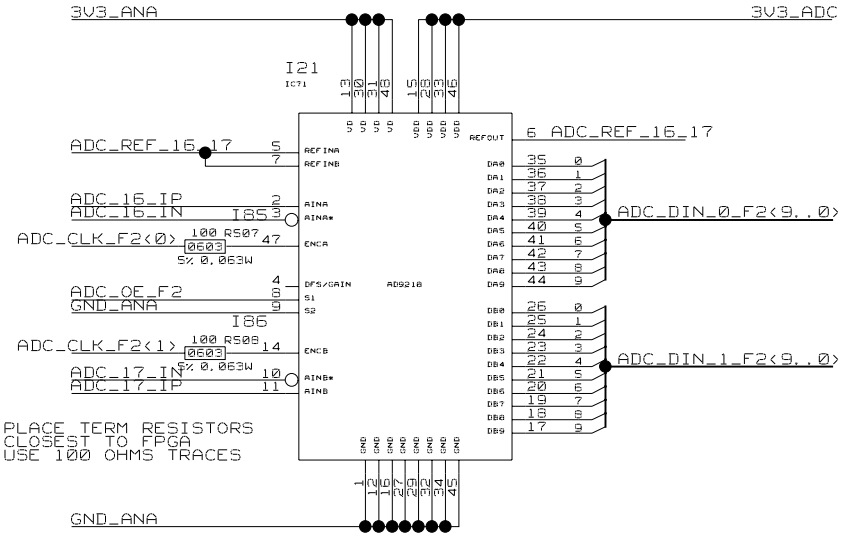
79 OHMS TRACES ON ALL BLS_ SIGNALS
MATCH LENGTH OF _P AND _N SIGNAL TRACES
THERMAL PAD BELOW CASE



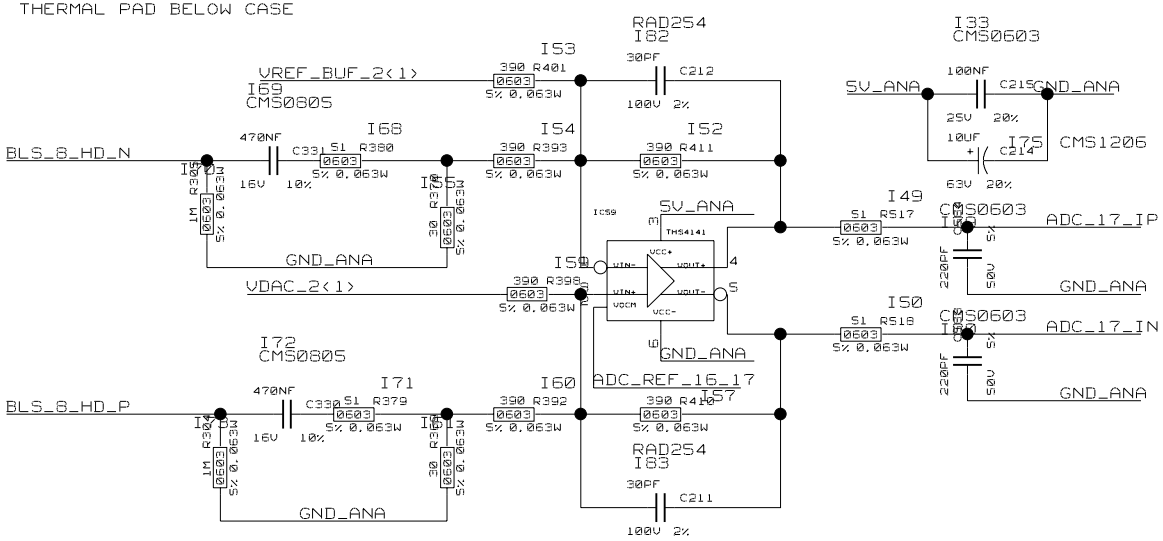


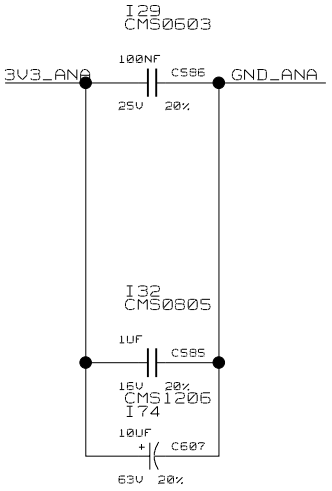
	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		NUMERO PLANCHE 47
SOUS/ENS: ADC CHANNEL 14-15		

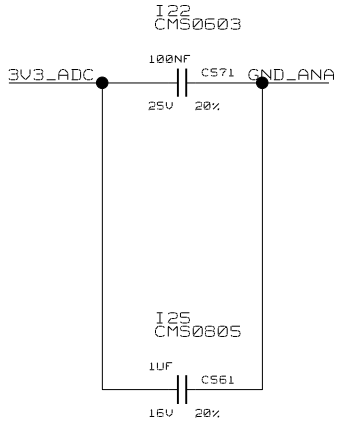




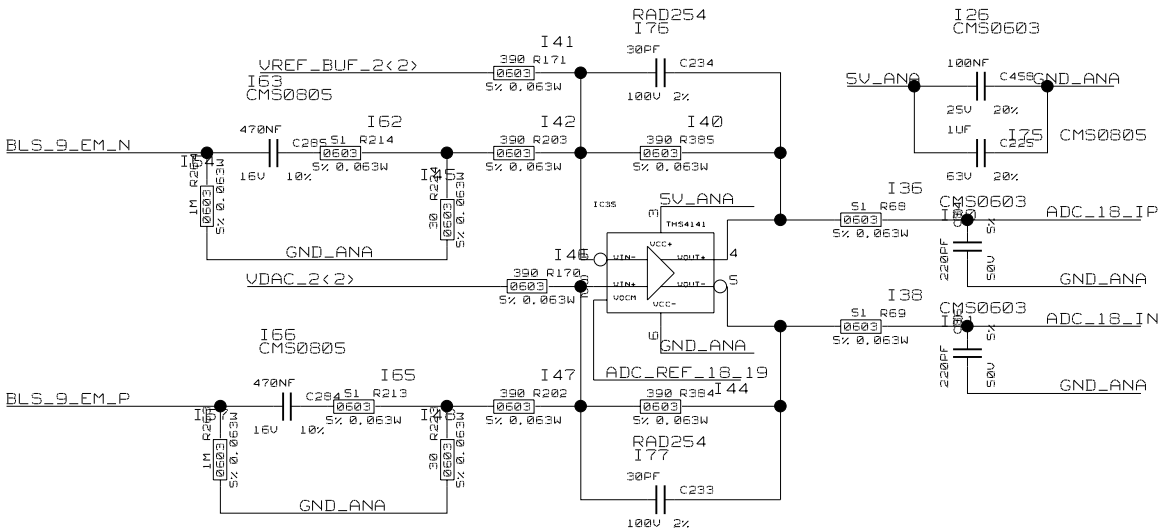
79 OHMS TRACES ON ALL BLS_ SIGNALS
MATCH LENGTH OF _P AND _N SIGNAL TRACES
THERMAL PAD BELOW CASE

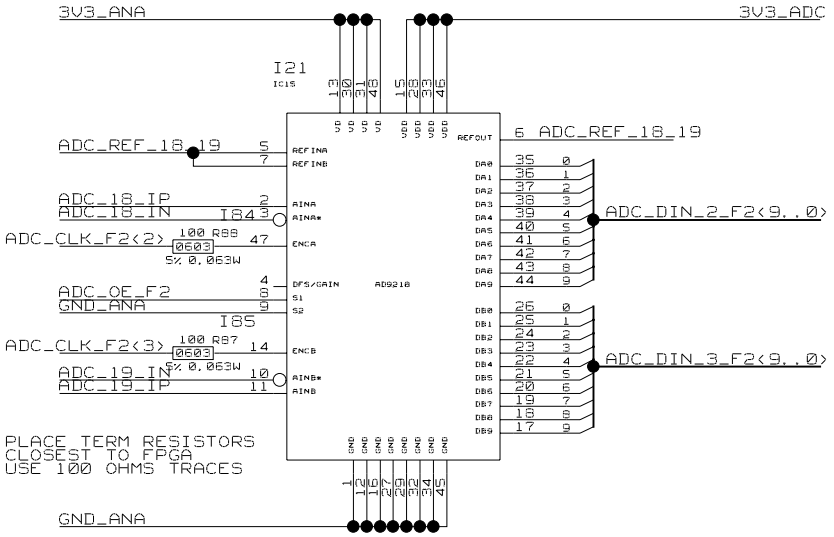




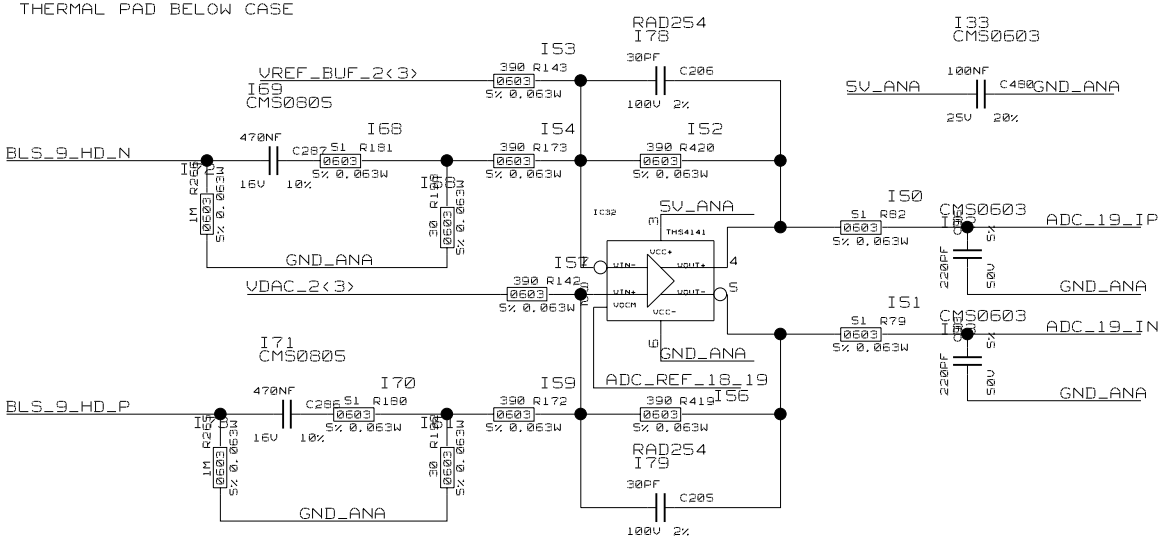


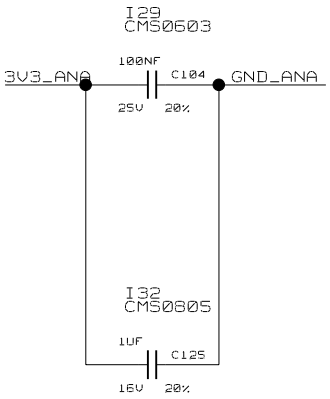
	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		NUMERO PLANCHE 48
SOUS/ENS: ADC CHANNEL 16-17		

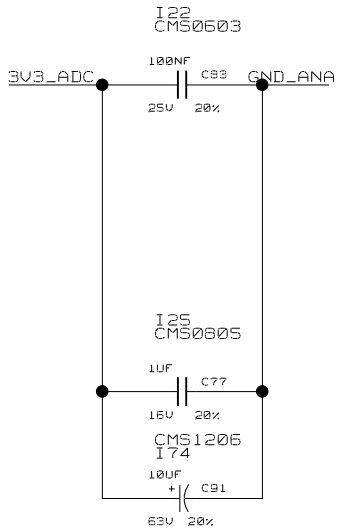




79 OHMS TRACES ON ALL BLS_ SIGNALS
MATCH LENGTH OF _P AND _N SIGNAL TRACES
THERMAL PAD BELOW CASE







	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR

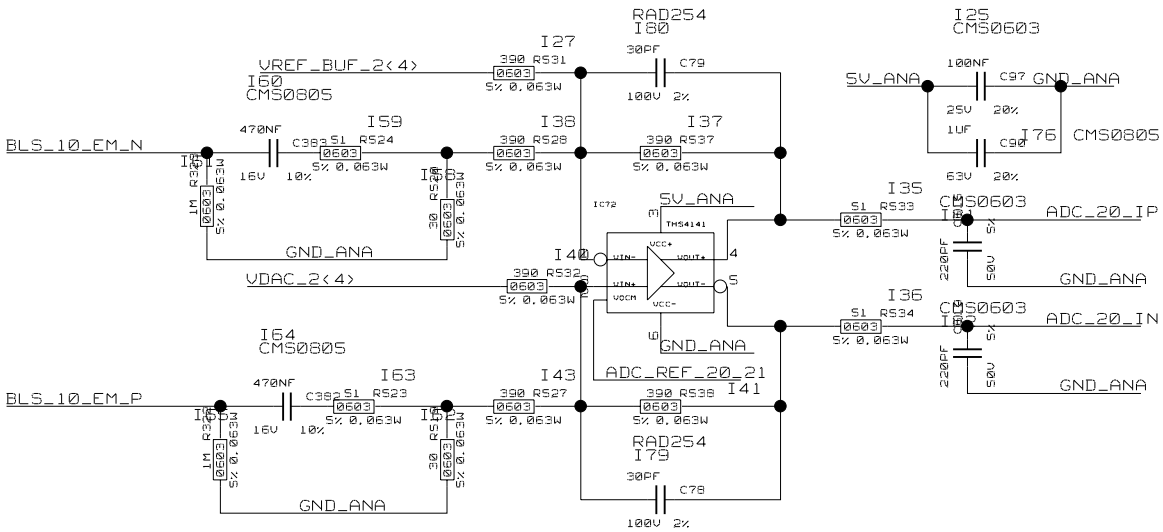
CEA DAPNIA/SEDI

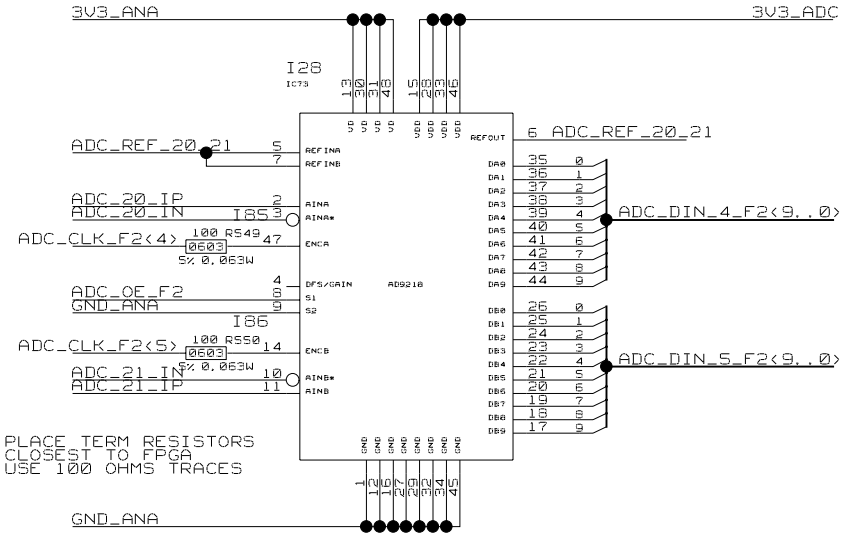
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)

PROJET: DZERO L1 CAL RUN IIB — NUMERO CIRCUIT

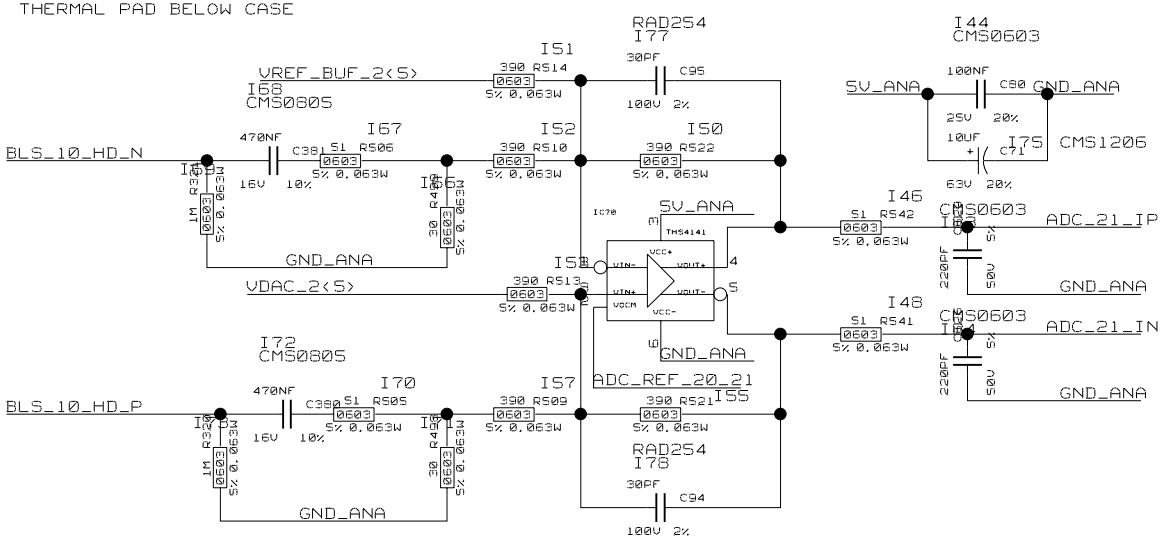
ENSEMBLE: ADF BOARD

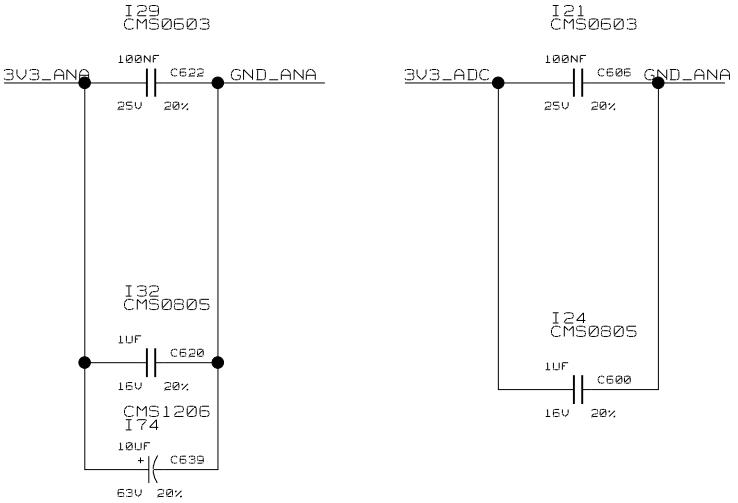
SOUS/ENS: ADC CHANNEL 18-19 — NUMERO PLANCHE 49



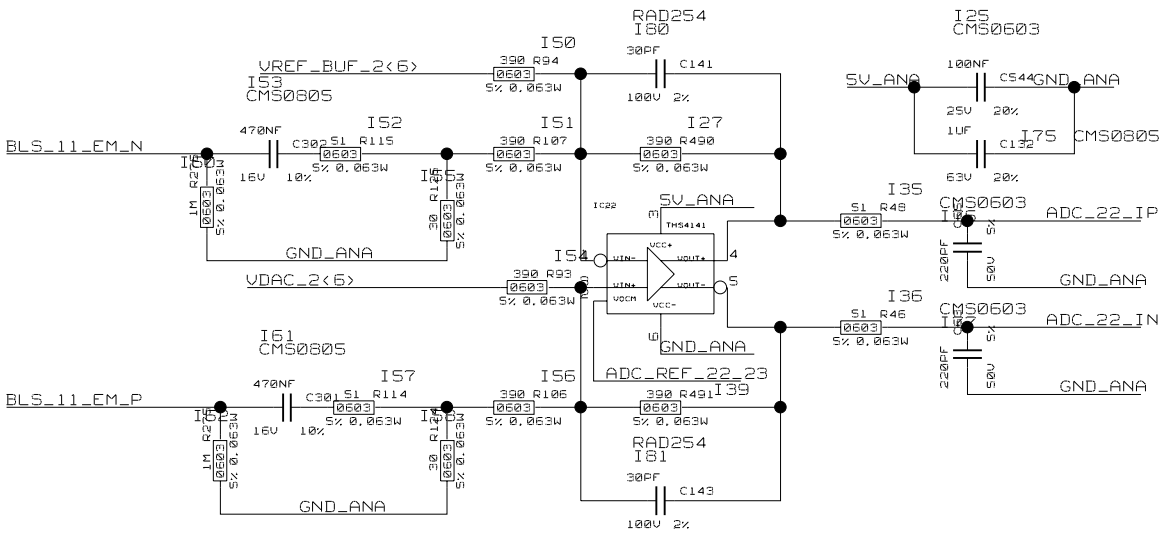


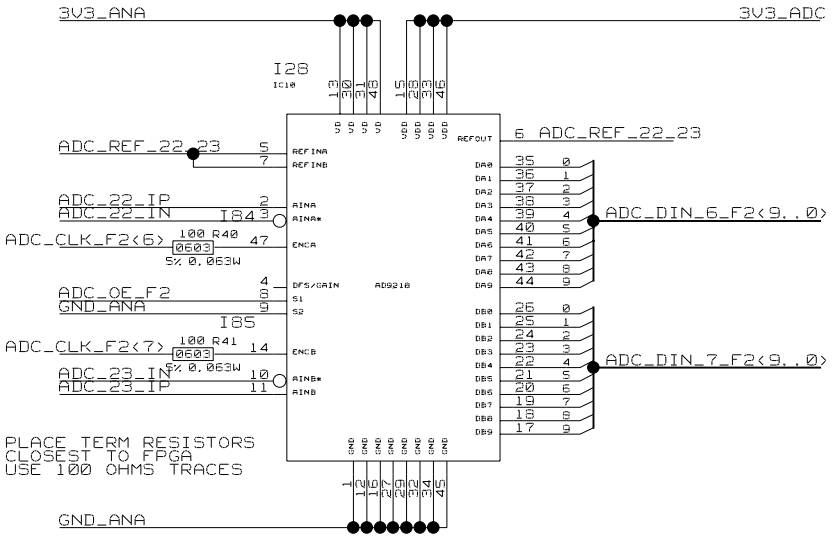
79 OHMS TRACES ON ALL BLS_ SIGNALS
MATCH LENGTH OF _P AND _N SIGNAL TRACES
THERMAL PAD BELOW CASE



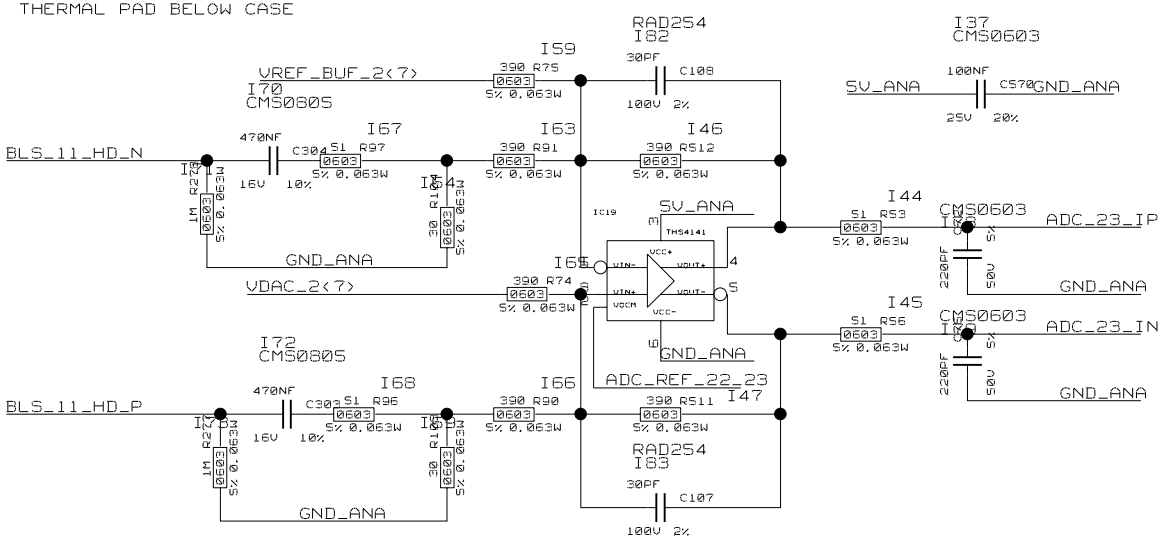


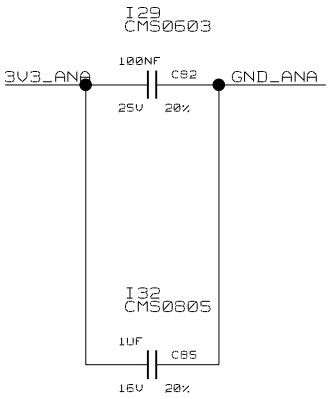
	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		NUMERO PLANCHE S0
SOUS/ENS: ADC CHANNEL 20-21		

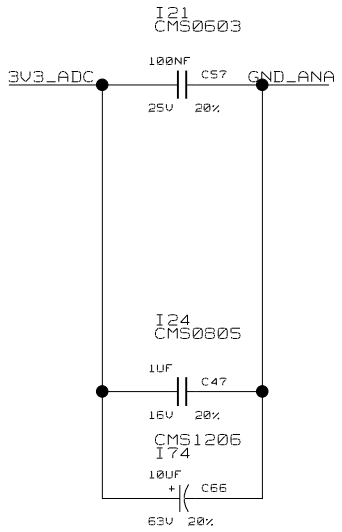




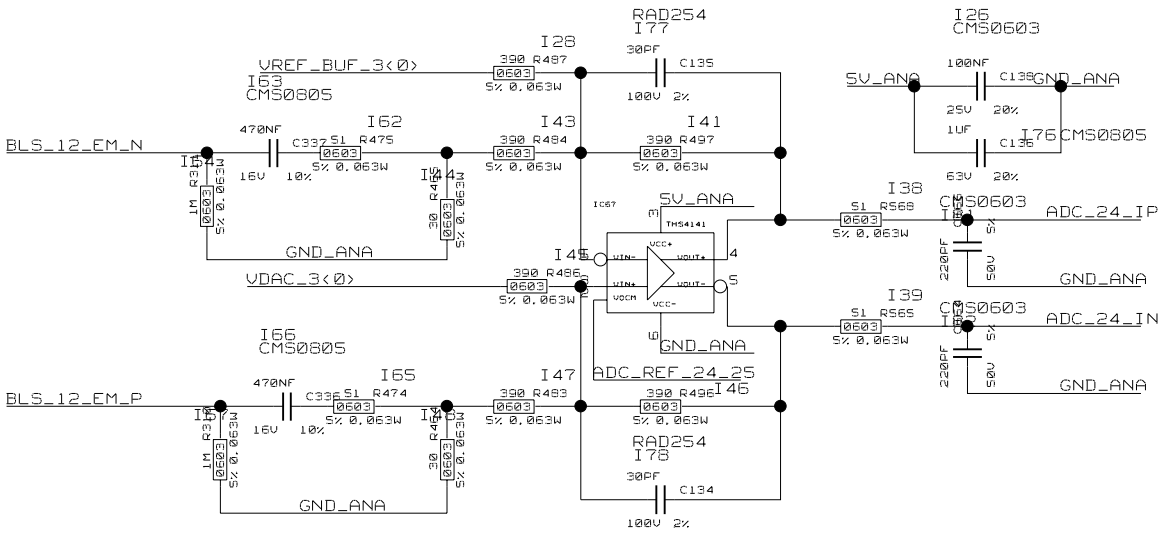
79 OHMS TRACES ON ALL BLS_ SIGNALS
MATCH LENGTH OF _P AND _N SIGNAL TRACES
THERMAL PAD BELOW CASE

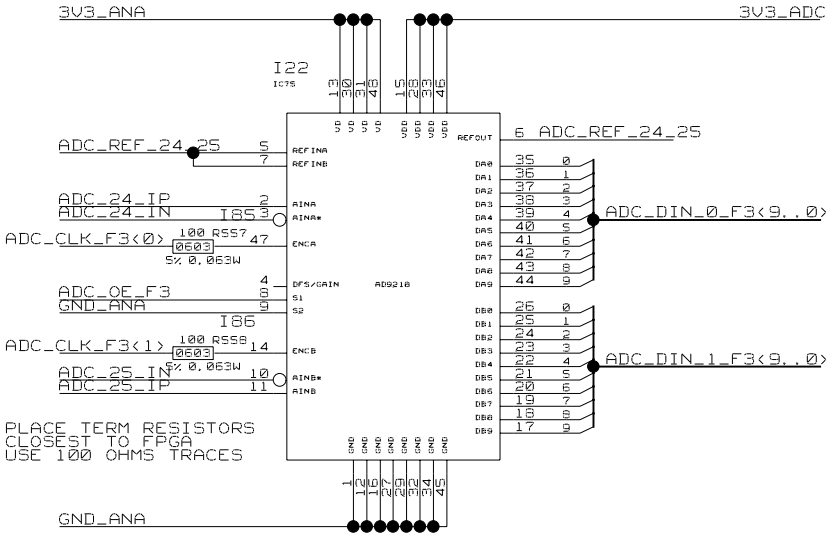




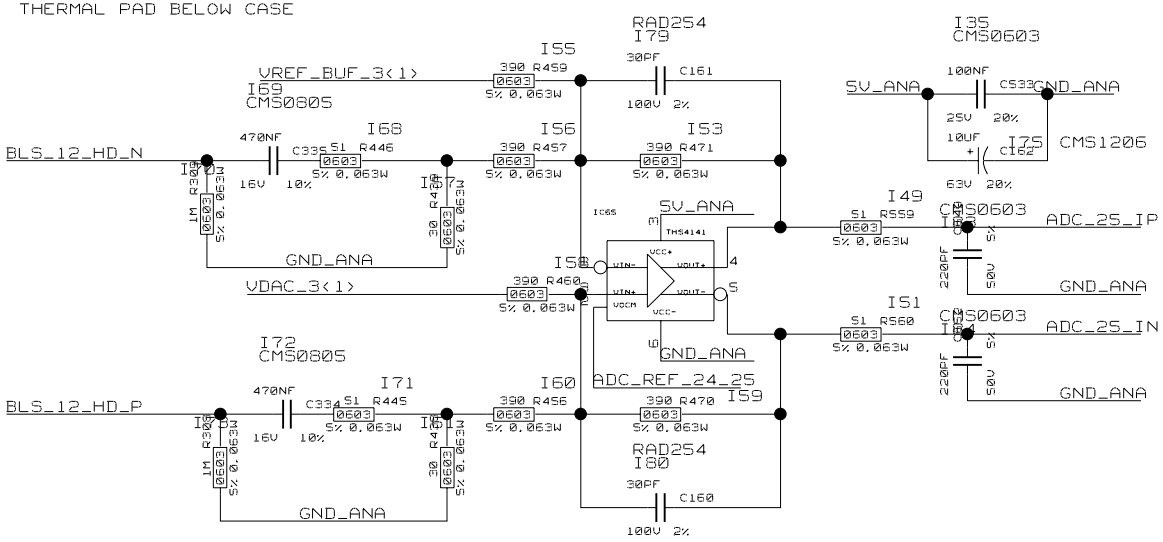


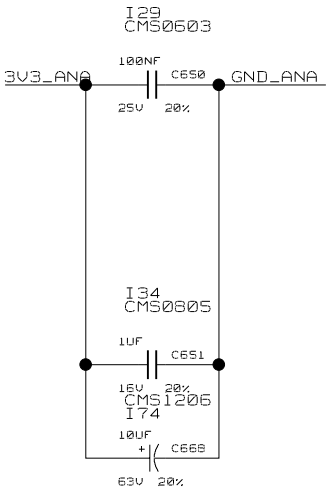
	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: ADC CHANNEL 22-23		NUMERO PLANCHE S1

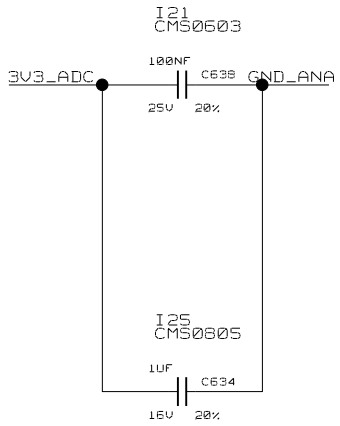




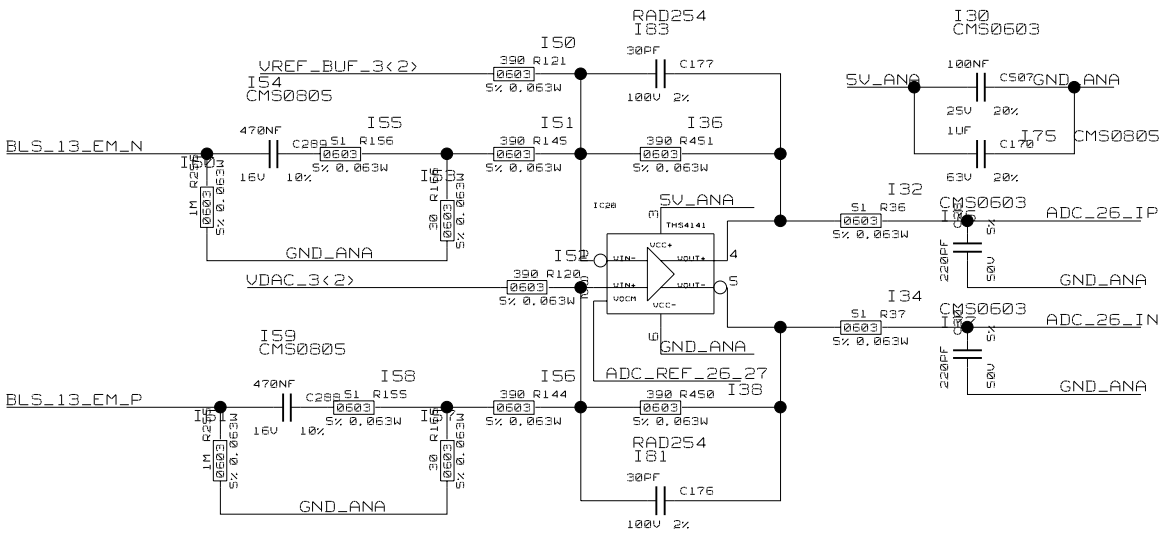
79 OHMS TRACES ON ALL BLS_ SIGNALS
MATCH LENGTH OF _P AND _N SIGNAL TRACES
THERMAL PAD BELOW CASE

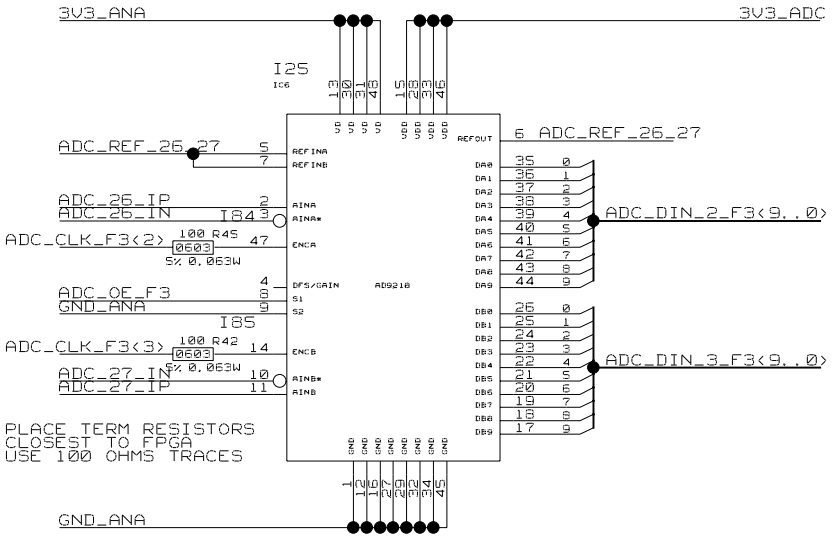




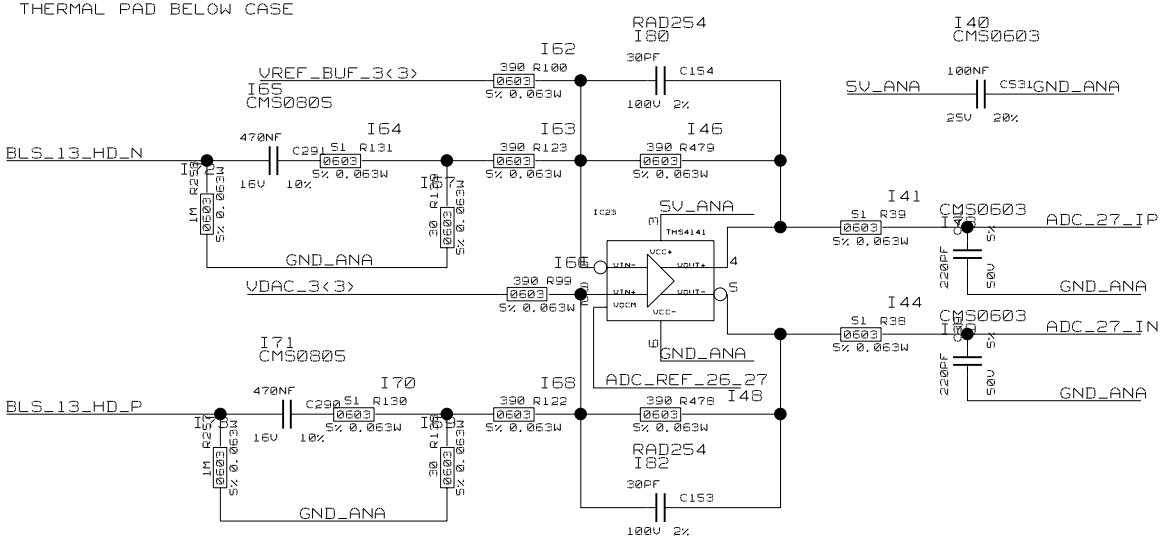


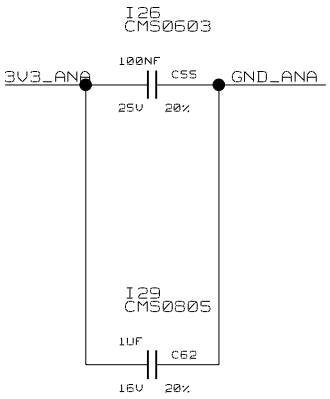
	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		NUMERO PLANCHE S2
SOUS/ENS: ADC CHANNEL 24-25		

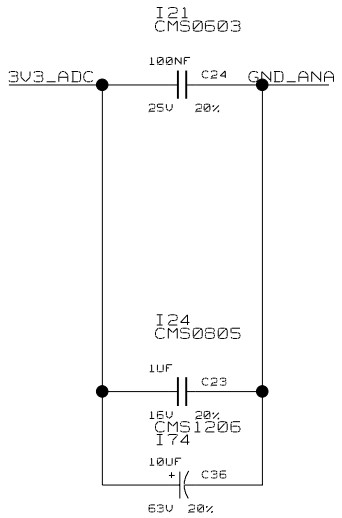




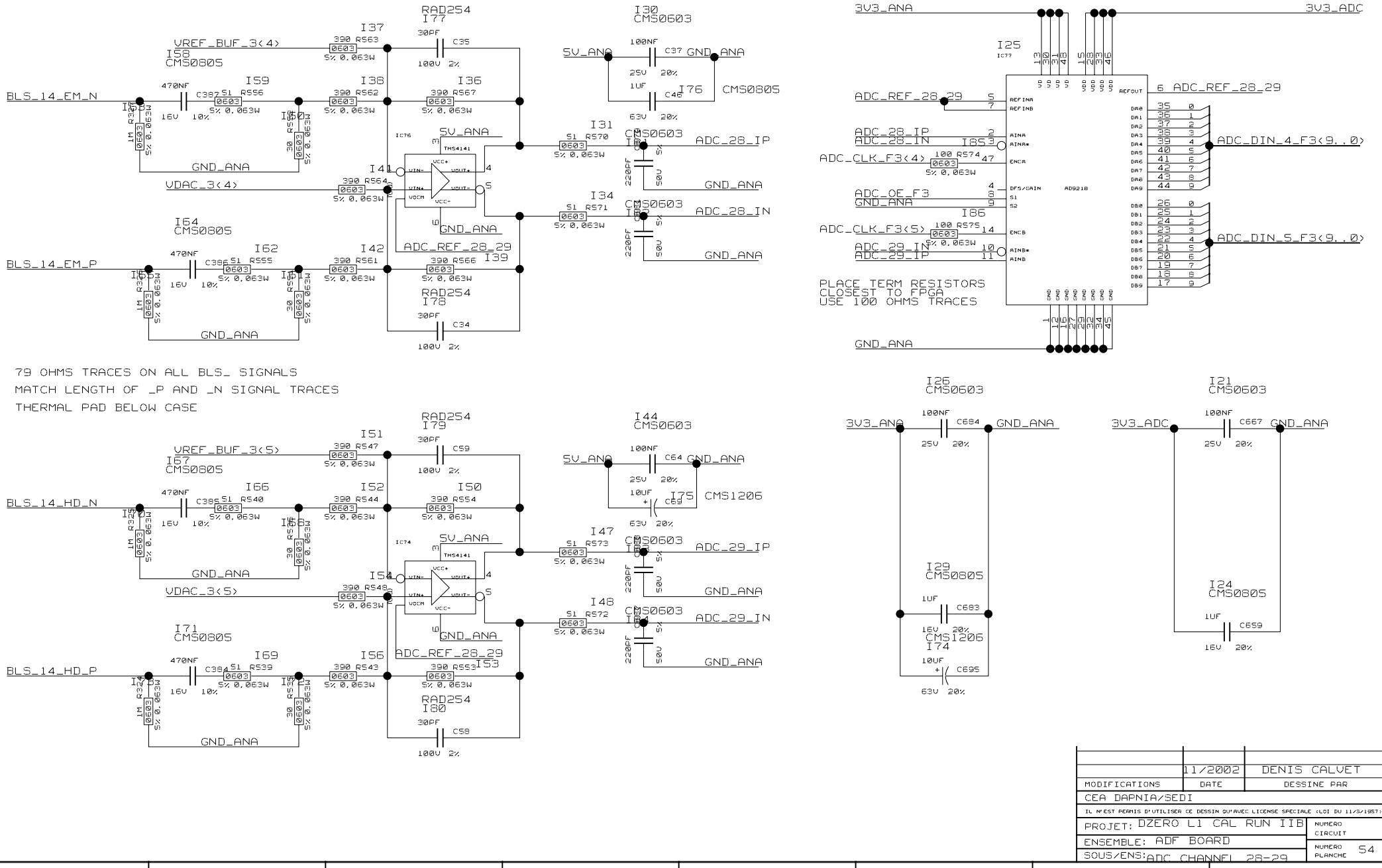
79 OHMS TRACES ON ALL BLS_ SIGNALS
MATCH LENGTH OF _P AND _N SIGNAL TRACES
THERMAL PAD BELOW CASE



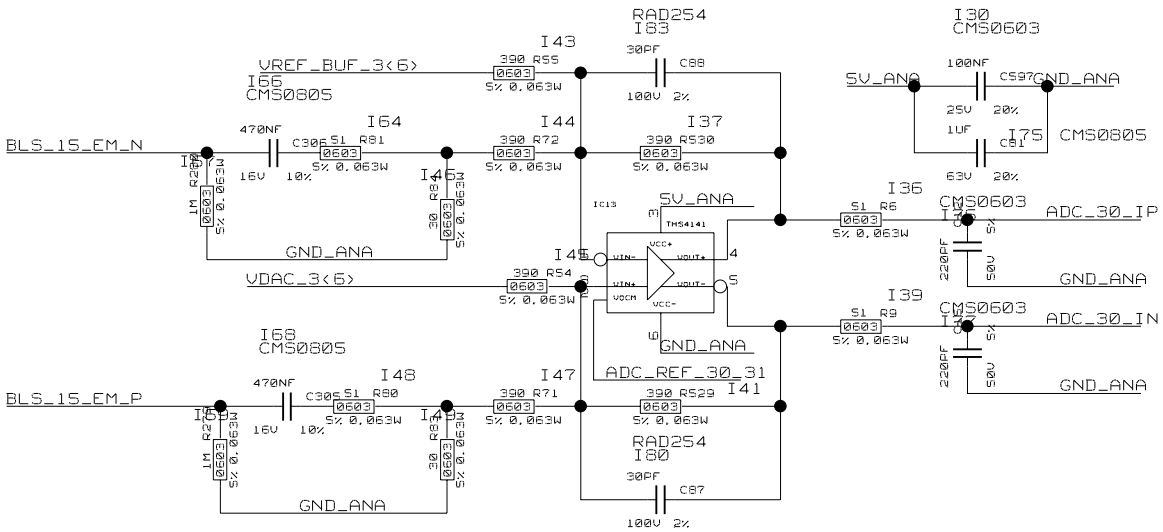


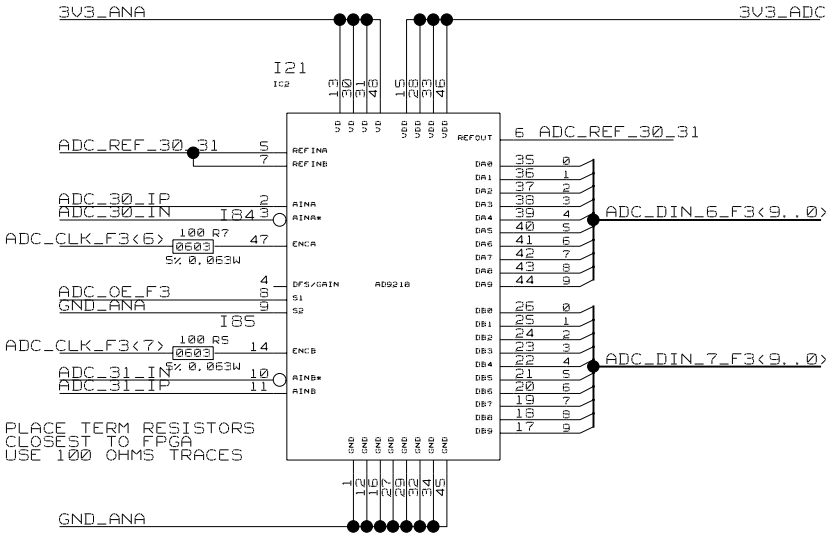


	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		NUMERO PLANCHE S3
SOUS/ENS: ADC CHANNEL 26-27		

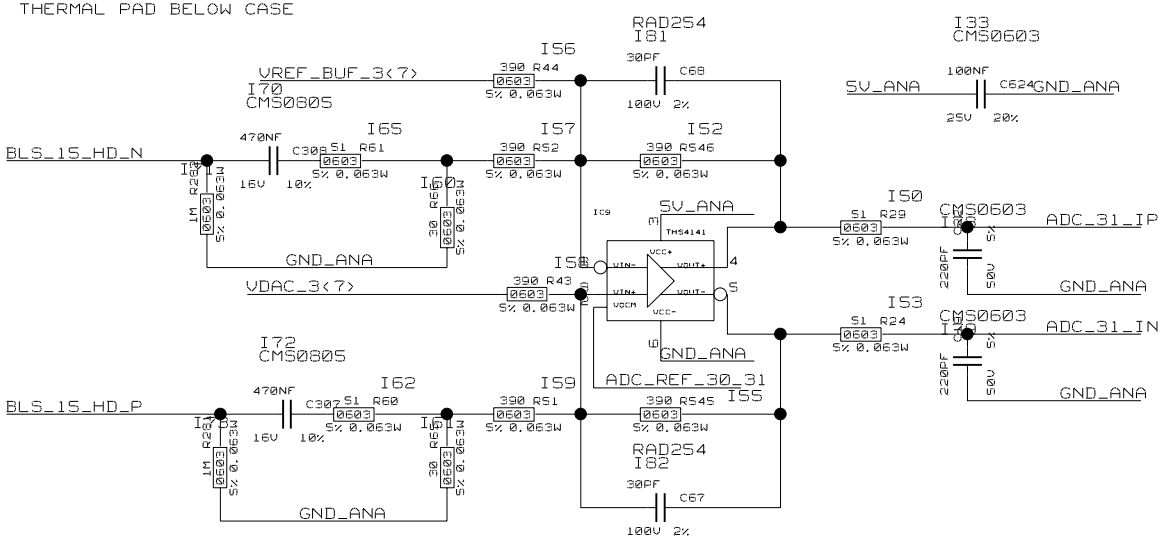


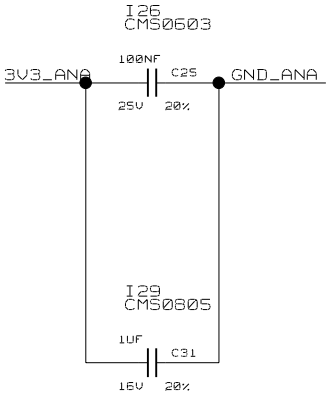
	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: ADC CHANNEL 28-29		NUMERO PLANCHE S4

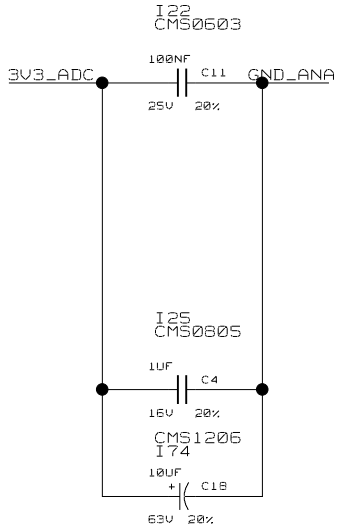




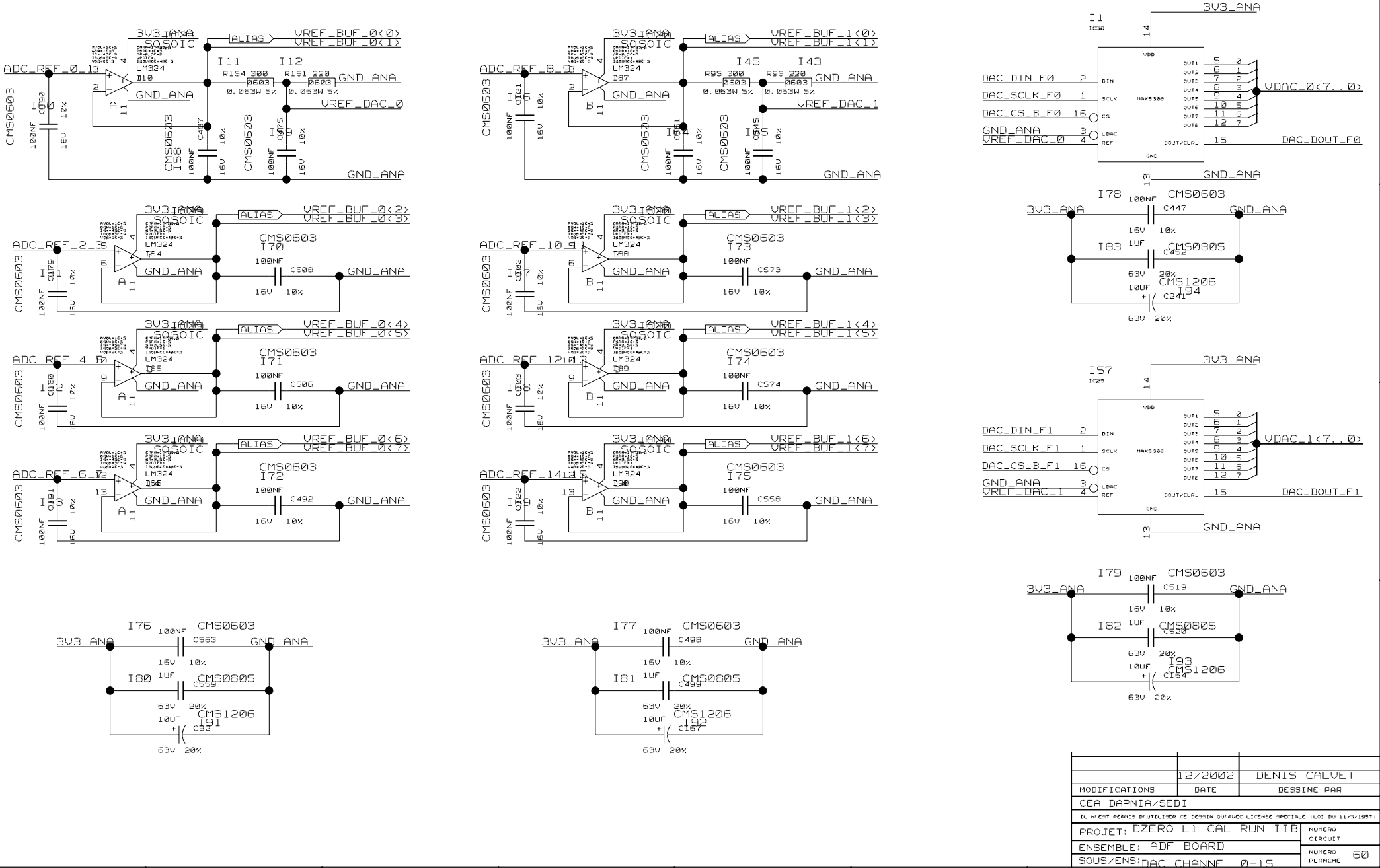
79 OHMS TRACES ON ALL BLS_ SIGNALS
MATCH LENGTH OF _P AND _N SIGNAL TRACES
THERMAL PAD BELOW CASE



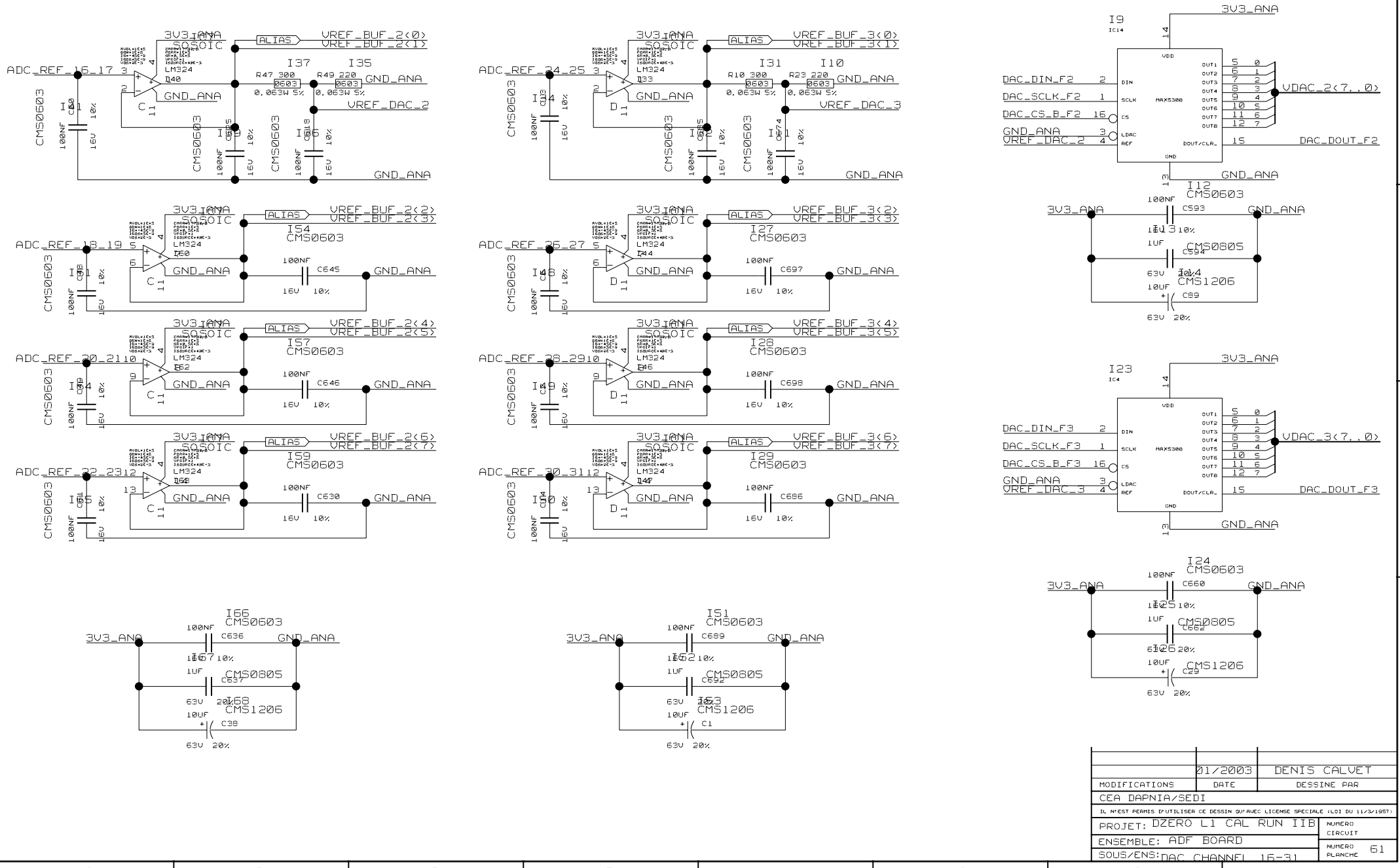




	11/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: ADC CHANNEL 30-31		NUMERO PLANCHE 55



	12/2002	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: DAC CHANNEL 0-15		NUMERO PLANCHE 60



	01/2003	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: ADF BOARD		
SOUS/ENS: DAC CHANNEL 16-31		NUMERO PLANCHE 61