# Virtex-II
# XC2V40/XC2V1000NM
# Reference Board
# User's Guide


**Version 1.2**
**December 2001**

Insight MEMEC

## Revisions

**Rev 1.2**
**Corrected pin numbers in Table 16 – J12 User I/O Connector**

# Table of Contents

## Figures

## Tables

## 1 Overview

The Virtex-II Development Kit provides an easy to use development platform for prototyping and verifying Virtex-II based designs. The Virtex-II family is a platform FPGA developed for high performance, low to high-density designs utilizing IP cores and customized modules. The Virtex-II family delivers complete solutions for telecommunication, wireless, networking, video, and DSP applications. The performance and density of the Virtex-II family along with its supported I/O standards such as LVDS, high performance interfaces such as PCI and DDR enables FPGA designers to meet the design requirements of the next generation telecommunication and Networking applications. The Virtex-II reference board utilizes the Xilinx 40K/1M gate Virtex-II (XC2V40 or XC2V1000) device. The Xilinx Virtex-II FPGA along with its supporting I/O devices on this reference board, will assist FPGA designers to prototype high-performance memory and I/O interfaces such as complete high-performance differential signaling (LVDS) and high speed DDR memory interface.

The Virtex-II reference board utilizes the Xilinx XC18V512 or XC18V04 ISP PROM, allowing FPGA designers to quickly download revisions of a design and verify the design changes in order to meet the final system-level design requirements. In addition to the ISP PROM, the reference board provides a JTAG connector for direct configuration of the Virtex-II FPGA.

The Virtex-II high performance and flexible Digital Clock Manager (DCM) coupled with its on-chip Digital Controlled Impedance (DCI) for source/load terminations, enables the FPGA designers to perform high level of integration, reduces the board level cost, and improve the overall system level reliability and performance. The Virtex-II advanced features, the in-system programmability of the on-board ISP PROM, the complete high-performance differential signaling support, coupled with a library of pre-configured reference designs from the new Reference Design Center, make the Insight kit a perfect solution for FPGA and system designers needing a quick, flexible, and low cost prototyping platform.

The Insight Virtex-II reference board is bundled with VHDL and/or Verilog HDL reference design examples to help FPGA designers to shorten their development time and meet their time-to-market requirements.

## 2 Virtex-II Reference Board Block Diagram

A high-level block diagram of the Virtex-II reference board is shown in Figure 1 followed by a brief description of each sub-section.

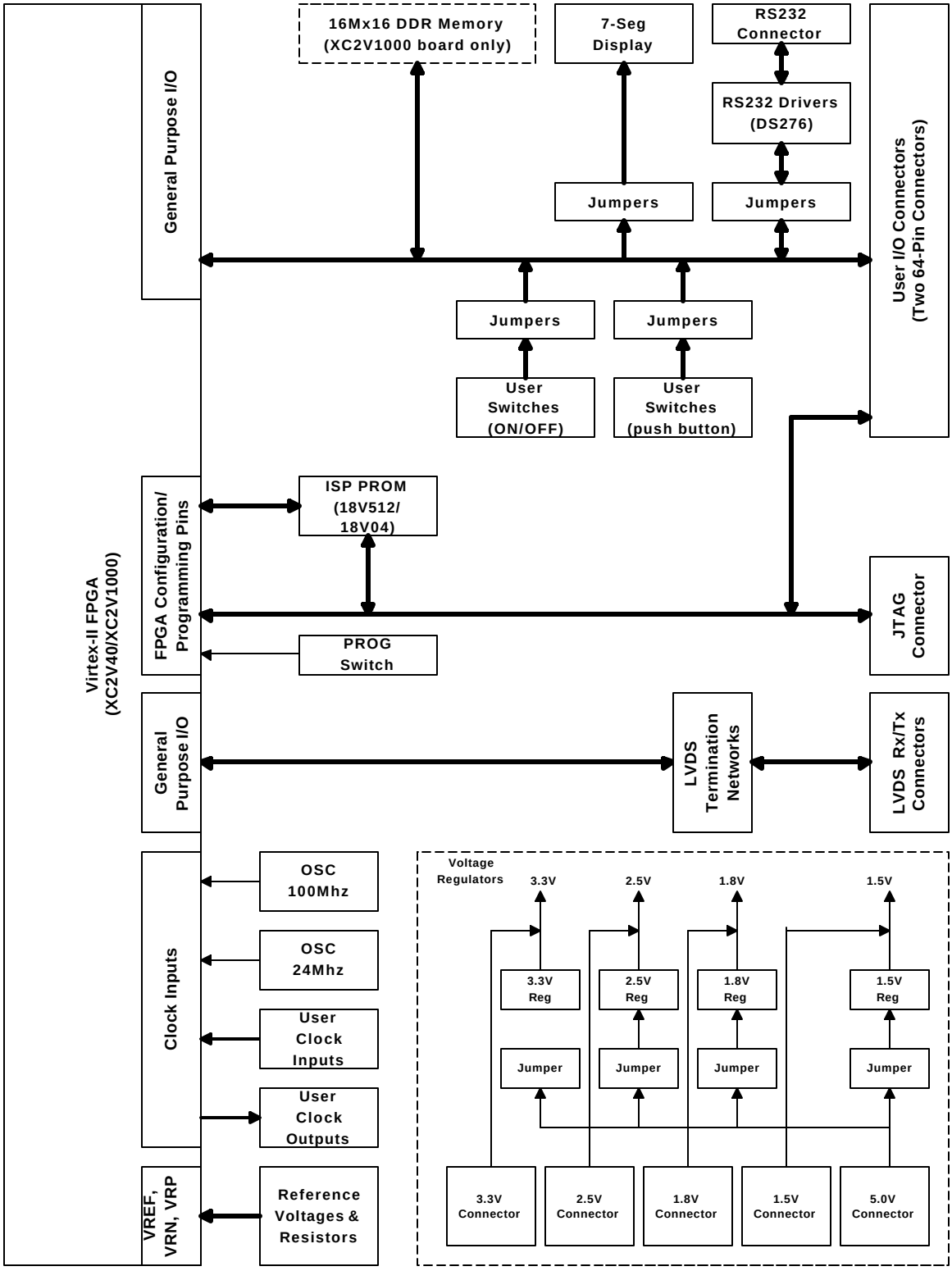


**Figure 1 - XC2V40/XC2V1000 Reference Board Block Diagram**

## 2.1 Virtex-II Device

The Virtex-II reference board utilizes the Xilinx Virtex-II XC2V40-4FG256C or the XC2V1000-4FG256C depending on the development kit part number. The Virtex-II family is a platform FPGA developed for high performance, low to high-density designs utilizing IP cores and customized modules. The Virtex-II family delivers complete solutions for telecommunication, wireless, networking, video, and DSP applications. The performance and density of the Virtex-II family along with its supported I/O standards such as LVDS, high performance interfaces such as PCI and DDR enables FPGA designers to meet the design requirements of the next generation telecommunication and Networking applications. The Xilinx Virtex-II FPGA along with its supporting I/O devices on this reference board, will assist FPGA designers to prototype high-performance memory and I/O interfaces such as complete high-performance differential signaling (LVDS) and high speed DDR memory interface.

## 2.2 Optional DDR User Memory

The Virtex-II reference board provides 32M bytes of user DDR memory. This optional memory, which is only offered on the XC2V1000 board, is implemented using the Toshiba TC59WM815BFT 16Mx16 DDR memory. Due to the high-speed operation of the DDR memory interface, the interface signals must be dedicated and not be multiplexed for the purpose of using them as general-purpose I/O pins when the on-board DDR memory is not used. Since the DDR memory interface takes 40 I/O pins, and the XC2V40 device in the 256-pin package provides a maximum of 88 user I/O pins, the user DDR memory is not provided on the XC2V40 reference board. The following table shows the DDR memory interface signal descriptions.

**Table 1 - DDR Memory Interface Signal Descriptions**

| Signal Name | Description |
|---|---|
| A[0:12] | Address Bus |
| DQ[0:15] | Data Bus |
| BS[0:1] | Bank Select |
| LDM, UDM | Write Mask |
| LDQS, UDQS | Write/Read Data Strobe |
| CSn | Chip Select |
| RASn | Row Address Strobe |
| CASn | Column Address Strobe |
| WEn | Write Enable |
| CLK | Clock |
| CLKn | Clock |
| CKE | Clock Enable |

## 2.3 Clock Generation

The Virtex-II reference board provides four master clock inputs to the Virtex-II FPGA. In addition to the Virtex-II FPGA, these clock inputs are also connected to the User I/O connectors. The following table provides a brief description of these clock signals.

**Table 2 - Virtex-II Reference Board Master Clocks**

| Signal Name | Virtex-II Pin # | Connector Pin # | Direction | Description |
|---|---|---|---|---|
| CLK.CAN1 | T9 | J12 pin 61 | Input | On-board 100 MHz Oscillator |
| CLK.CAN2 | P9 | J12 pin 62 | Input | On-board 24 MHz Oscillator |
| CLK.SMB | R9 | J12 pin 59 & J18 | Input | User Clock Input 1 |
| CLK.SMBALT | N9 | J12 pin 60 & J17 | Input | User Clock Input 2 |
| FPGA.SMB1 | B4 | J16 | Output | User Clock Output 1 |
| FPGA.SMB2 | E4 | J15 | Output | User Clock Output 2 |

### 2.3.1 Oscillators

The Virtex-II reference board provides two on-board oscillators running at 100Mhz (CLK.CAN1) and 24Mhz (CLK.CAN2). The 100Mhz oscillator is enabled when the JP37 jumper is open, while leaving the JP38 jumper open will enable the 24Mhz oscillator. In addition to the Virtex-II FPGA, these clock inputs are also connected to the J12 User I/O connector (pins 61 and 62).

### 2.3.2 User Clock Inputs

The Virtex-II reference board provides two connections (J18 and J17) for user clock inputs to the Virtex-II FPGA (CLK.SMB and CLK.SMBALT). In addition to the Virtex-II FPGA, these clock inputs are also connected to the J12 User I/O connector (pins 59 and 60).

### 2.3.3 User Clock Outputs

The Virtex-II reference board provides two connections (J16 and J15) for user clock outputs. These two clock outputs, which are connected to the Virtex-II pins B4 and E4 respectively (through impedance-controlled traces) can be used to generate system level clock signals utilizing the Virtex-II Digital Clock Manager (DCM). The combination of the impedance-controlled traces, quality SMB connectors (J16 & J15), and the advanced features of the Virtex-II DCM provides a reliable platform for generating high-speed system level user clocks.

## 2.4 User 7-Segment Display

The Virtex-II reference board utilizes a common-cathode 7-segment LED display that can be used during the test and debugging phase of a design. The user can turn a given segment on by driving the associated signal high. The following figure shows the user 7-segment display interface to the Virtex-II FPGA.

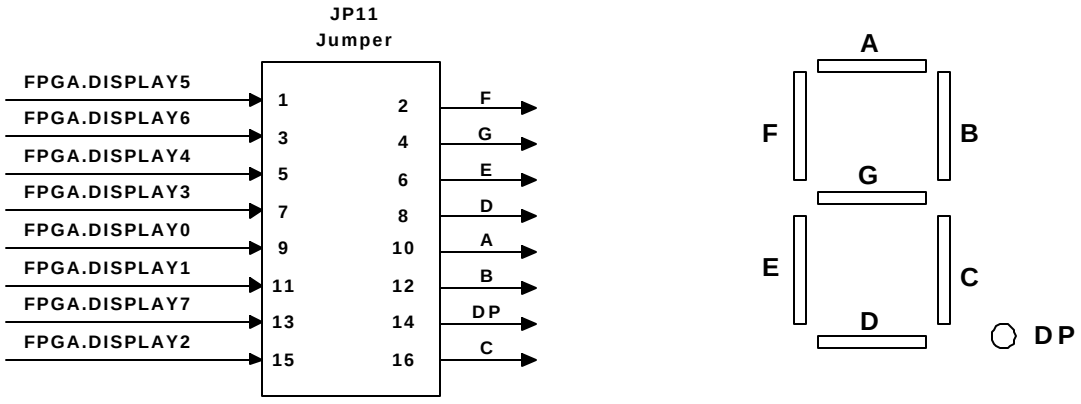


**Figure 2 - 7-Segment LED Display Interface**

### 2.4.1 7-Segment LED Display Jumper Settings

The following figure shows the jumper settings for using the user 7-segment LED display. Removing the jumpers from the headers will disconnect the FPGA I/O pins from the display, allowing the FPGA pins to be used as general-purpose I/O pins.

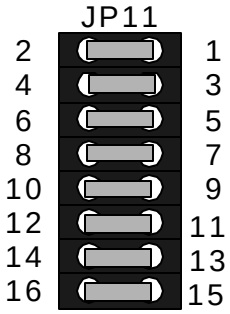


**Figure 3 - 7-Segment LED Display Jumper Settings**

### 2.4.2 7-Segment Display Signal Description

The following table shows the 7-Segment LED display pin descriptions. The 7-segment LED display pins are connected to the Virtex-II FPGA as well as the User I/O connector.

**Table 3 - 7-Segment Display Signal Descriptions**

| Signal Name | Virtex-II Pin # | J12 User I/O Connector Pin # | Description |
|---|---|---|---|
| FPGA.DISPLAY7 | A10 | 19 | 7-Segment LED Display, Blank Input |
| FPGA.DISPLAY6 | D9 | 14 | 7-Segment LED Display, Segment G |
| FPGA.DISPLAY5 | C9 | 13 | 7-Segment LED Display, Segment F |
| FPGA.DISPLAY4 | B9 | 15 | 7-Segment LED Display, Segment E |
| FPGA.DISPLAY3 | A9 | 16 | 7-Segment LED Display, Segment D |
| FPGA.DISPLAY2 | B13 | 20 | 7-Segment LED Display, Segment C |
| FPGA.DISPLAY1 | C12 | 18 | 7-Segment LED Display, Segment B |
| FPGA.DISPLAY0 | D12 | 17 | 7-Segment LED Display, Segment A |

## 2.5 User LED

The Virtex-II reference board provides a single user LED. Pin C13 of the Virtex-II FPGA is used to drive this active low signal. This signal is also connected to the pin 23 of the J12 User I/O connector.

## 2.6 User Push Button Switches (SW3 & SW4)

The Virtex-II reference board design provides two user push button switch inputs to the Virtex-II FPGA. In addition to the Virtex-II FPGA, these switch inputs are also connected to the J11 User I/O connector (pins 61 and 62). Each push button switch can be used to generate an active low signal.

### 2.6.1 User Push Button Switch Interface

The following figure shows the user push button switch interface to the Virtex-II FPGA.

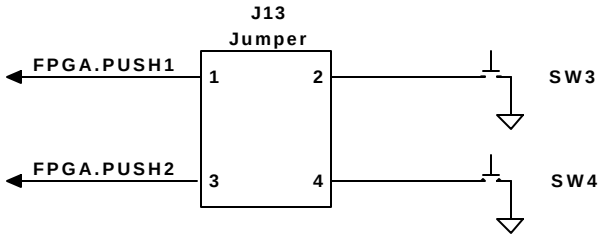


**Figure 4 – User Push Button Switches**

### 2.6.2 User Push Button Switch Jumper Settings

The following figure shows the jumper settings for using the user push button switches. A given switch is not used when its associated jumper is removed. Removing the jumper will disconnect the switch input from the Virtex-II FPGA and the User I/O connector.

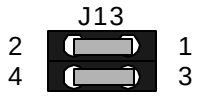


**Figure 5 – User Push Button Switch Jumper Settings**

### 2.6.3 User Push Button Switch Signal Assignments

The following table shows the pin assignments for the user push button switches.

**Table 4 - User Push Button Switch Signal Assignments**

| Signal Name | Virtex-II Pin # | J11 User I/O Connector Pin # | Description |
|---|---|---|---|
| FPGA.PUSH1 | M4 | 61 | User Push Button Switch Input 1 (SW3) |
| FPGA.PUSH2 | T7 | 62 | User Push Button Switch Input 2 (SW4) |

## 2.7 User DIP Switch (SW2)

The Virtex-II reference board provides 8 user switch inputs. These switches can be statically set to a low or high logic level.

### 2.7.1 User DIP Switch Interface

The following figure shows the user DIP switch interface to the Virtex-II FPGA.

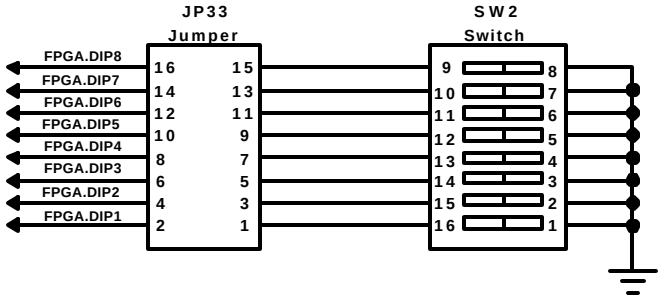


**Figure 6 – User DIP Switch Interface**

### 2.7.2 User DIP Switch Jumper Settings

The following figure shows the jumper settings for using the user DIP switch. A given switch is not used when its associated jumper is removed. Removing the jumper will disconnect the switch input from the Virtex-II FPGA and the User I/O connector.

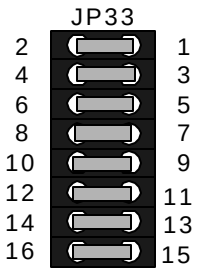


**Figure 7 – User DIP Switch Jumper Settings**

### 2.7.3 User DIP Switch Signal Assignments

The following table shows the user switch pin assignments.

**Table 5 - User DIP Switch Signal Assignments**

| Signal Name | Virtex-II Pin # | J12 User I/O Connector Pin # | Description |
|---|---|---|---|
| FPGA.DIP8 | J15 | 51 | User Switch Input 8 |
| FPGA.DIP7 | J16 | 52 | User Switch Input 7 |
| FPGA.DIP6 | M13 | 53 | User Switch Input 6 |
| FPGA.DIP5 | N16 | 54 | User Switch Input 5 |
| FPGA.DIP4 | P16 | 55 | User Switch Input 4 |
| FPGA.DIP3 | T14 | 56 | User Switch Input 3 |
| FPGA.DIP2 | R13 | 57 | User Switch Input 2 |
| FPGA.DIP1 | T10 | 58 | User Switch Input 1 |

### 2.8 RS232 Port

The Virtex-II reference board provides RS232 drivers and connector that can be driven by the Virtex-II FPGA or the User I/O connector. A subset of the RS232 signals is used on the Virtex-II reference board to implement this interface (RD and TD signals).

### 2.8.1 RS232 Interface

The Virtex-II reference board provides a DB-9 connection for a simple RS232 port. This board utilizes the Dallas Semiconductor DS276S RS232 driver for driving the RD and TD signals. The RS232 UART code, which resides in the Virtex-II FPGA is provided by the user.

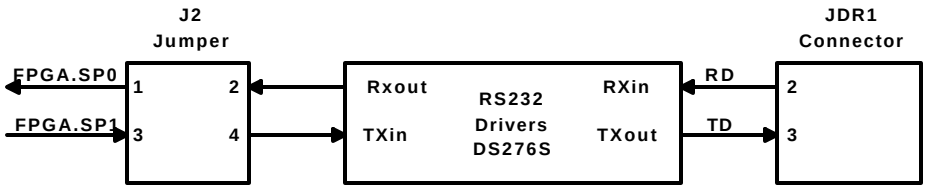


**Figure 8 – RS232 Interface**

### 2.8.2 RS232 Jumper Settings

The following figure shows the jumper settings for the RS232 interface. A specific signal is used when its associated jumper is closed. Removing a jumper will disconnect its associated signals from the Virtex-II and the User I/O connector.

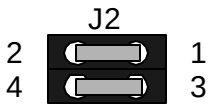


**Figure 9 – RS232 Jumper Settings**

### 2.8.3 RS232 Signal Descriptions

The following table shows the RS232 signals and their pin assignments to the Virtex-II FPGA and the J15 User I/O connector.

**Table 6 - RS232 Signal Descriptions**

| Signal Name | Virtex-II Pin # | J11 User I/O Connector Pin # | Description |
|---|---|---|---|
| FPGA.SP0 | C8 | 25 | Received Data, RD |
| FPGA.SP1 | D8 | 26 | Transmit Data, TD |

## 2.9 JTAG Port

The Virtex-II reference board design provides a JTAG port that can be used to configure and/or program various devices on the board and JTAG devices connected to the User I/O connector.

### 2.9.1 JTAG Connector

The Virtex-II reference board provides a JTAG connector that can be used to program the on-board ISP PROM, configure the Virtex-II FPGA, and program and/or configure JTAG devices connected to the User I/O connector. The following figure shows the pin assignments for the JTAG connector on the Virtex-II reference board.

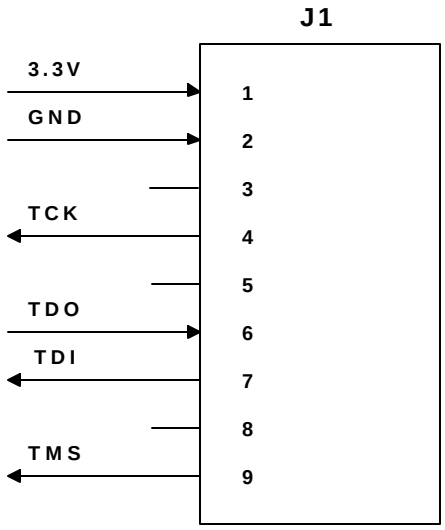


**Figure 10 – JTAG Connector**

### 2.9.2 JTAG Signal Descriptions

The following table provides a brief description of the JTAG signals and their pin assignments to the Virtex-II FPGA and the User I/O connector.

**Table 7 - JTAG Signal Descriptions**

| Signal Name | Virtex-II Pin # | J1 JTAG Connector Pin # | Description |
|---|---|---|---|
| TDI | C2 | 7 | JTAG Data Input |
| TCK | A15 | 4 | JTAG Clock Input |
| TMS | B14 | 9 | JTAG Test Mode Input |
| TDO | C15 | 6 | JTAG Data Output |

### 2.9.3 JTAG Chain

The following figure shows the JTAG chain on the Virtex-II reference board. If any of the devices in the chain are not populated, their associated jumper must be closed in order to maintain the chainintegrity. If no JTAG device is connected to the User I/O connector, the TDI signal connected to this connector must be shorted to the TDO pin. This can be accomplished by closing the JP7 jumper.

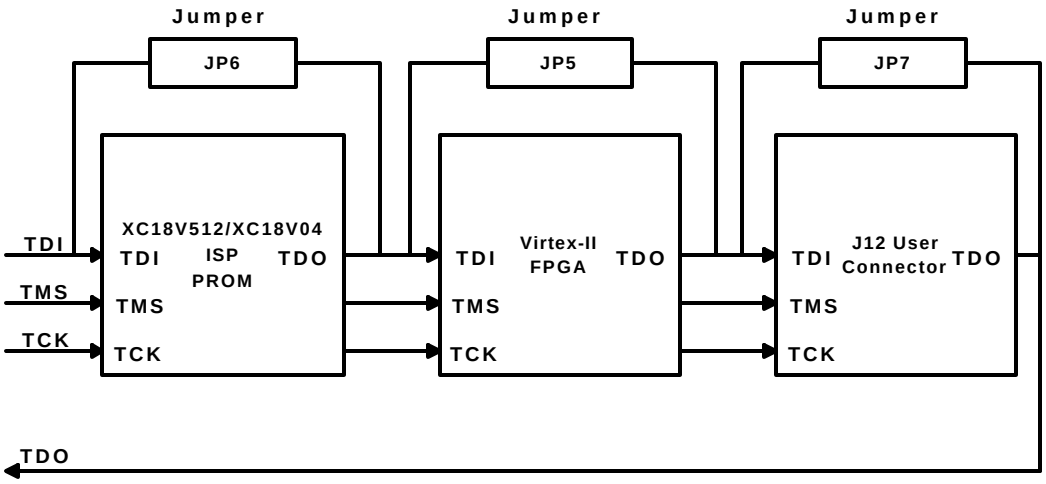


**Figure 11 – Virtex-II Reference Board JTAG Chain**

### 2.9.4 JTAG Chain Jumper Settings

The following table shows the JTAG chain jumper setting on the Virtex-II reference board.

**Table 8 - JTAG Chain Jumper Settings**

| Jumper | Setting | Description |
|---|---|---|
| JP6 | Open | XC18V512/04 ISP PROM is populated |
| | Closed | XC18V512/04 ISP PROM is not populated |
| JP5 | Open | Virtex-II FPGA is populated |
| | Closed | Virtex-II FPGA is not populated |
| JP7 | Open | JTAG device(s) is connected to the User I/O connector |
| | Closed | JTAG device(s) is not connected to the User I/O connector |

## 2.10 Bank I/O Voltage

The Virtex-II reference board allows the Virtex-II I/O pins to be configured for 1.5V, 1.8V, 2.5V, or 3.3V operation. All Virtex-II user I/O pins are grouped in 8 different banks. Each bank of I/O pins on the board can be configured to operate in the 1.5V, 1.8V, 2.5V, or the 3.3V mode. The following figure shows the bank I/O voltage selection on a given Virtex-II bank.

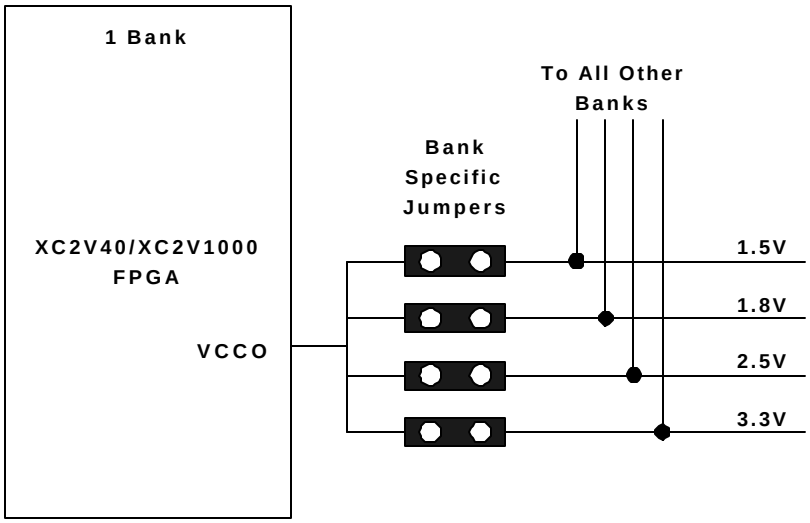


**Figure 12 – XC2V40/XC2V1000 VCCO Connections**

### 2.10.1 Bank I/O Voltage Jumper Settings

The following table shows the jumper settings for the Virtex-II bank I/O voltage (VCCO) selection. Each bank can be set to 1.5V, 1.8V, 2.5V, or 3.3V.

**Table 9 - Bank I/O Voltage Jumper Settings**

| Bank # | Virtex-II Pin # | Jumper | | | | I/O Voltage |
|---|---|---|---|---|---|---|
| | | J6 | | | | |
| | | 1-2 | 3-4 | 5-6 | 7-8 | |
| 0 | F8, F7, E8 | Closed | Open | Open | Open | 3.3V |
| | | Open | Closed | Open | Open | 2.5V |
| | | Open | Open | Closed | Open | 1.8V |
| | | Open | Open | Open | Closed | 1.5V |
| | | J7 | | | | |
| | | 1-2 | 3-4 | 5-6 | 7-8 | |
| 1 | F10, F9, E9 | Closed | Open | Open | Open | 3.3V |
| | | Open | Closed | Open | Open | 2.5V |
| | | Open | Open | Closed | Open | 1.8V |
| | | Open | Open | Open | Closed | 1.5V |
| | | J8 | | | | |
| | | 1-2 | 3-4 | 5-6 | 7-8 | |
| 2 | H12, H11, G11 | Closed | Open | Open | Open | 3.3V |
| | | Open | Closed | Open | Open | 2.5V |
| | | Open | Open | Closed | Open | 1.8V |
| | | Open | Open | Open | Closed | 1.5V |
| | | J9 | | | | |
| | | 1-2 | 3-4 | 5-6 | 7-8 | |
| 3 | J12, J11, K11 | Closed | Open | Open | Open | 3.3V |
| | | Open | Closed | Open | Open | 2.5V |
| | | Open | Open | Closed | Open | 1.8V |
| | | Open | Open | Open | Closed | 1.5V |

| | | | | | | |
|---|---|---|---|---|---|---|
| **4** | L10, L9, M9 | **J10** | | | | |
| | | 1-2 | 3-4 | 5-6 | 7-8 | |
| | | Closed | Open | Open | Open | 3.3V |
| | | Open | Closed | Open | Open | 2.5V |
| | | Open | Open | Closed | Open | 1.8V |
| | | Open | Open | Open | Closed | 1.5V |
| **5** | L8, L7, M8 | **J3** | | | | |
| | | 1-2 | 3-4 | 5-6 | 7-8 | |
| | | Closed | Open | Open | Open | 3.3V |
| | | Open | Closed | Open | Open | 2.5V |
| | | Open | Open | Closed | Open | 1.8V |
| | | Open | Open | Open | Closed | 1.5V |
| **6** | J6, J5, K6 | **J4** | | | | |
| | | 1-2 | 3-4 | 5-6 | 7-8 | |
| | | Closed | Open | Open | Open | 3.3V |
| | | Open | Closed | Open | Open | 2.5V |
| | | Open | Open | Closed | Open | 1.8V |
| | | Open | Open | Open | Closed | 1.5V |
| **7** | H6, H5, G6 | **J5** | | | | |
| | | 1-2 | 3-4 | 5-6 | 7-8 | |
| | | Closed | Open | Open | Open | 3.3V |
| | | Open | Closed | Open | Open | 2.5V |
| | | Open | Open | Closed | Open | 1.8V |
| | | Open | Open | Open | Closed | 1.5V |

### 2.11 Bank Reference Voltage

Some input standards require a user supplied threshold voltage, VREF. In this case, certain user I/O pins are automatically configured as inputs for the VREF voltage.

VREF pins within a bank are interconnected internally, and consequently only one VREF voltage can be used within each bank. However, for correct operation, all VREF pins in the bank must be connected to the external reference voltage source.

In order to support all I/O standards provided by the XC2V40/XC2V1000 FPGA, a number of Reference Voltages must be supplied to the FPGA. The following table shows the I/O standards supported by the XC2V40/XC2V1000 FPGA and their required VREF.

**Table 10 - XC2V40/XC2V1000 Supported I/O Standards and their Required VREF**

| I/O Standard | VREF (Volts) | Comments |
|---|---|---|
| GTL | 0.80 | Not provided on the Virtex-II reference board |
| GTLP | 1.00 | Provided on the Virtex-II reference board |
| HSTL_I | 0.75 | Provided on the Virtex-II reference board |
| HSTL_II | 0.75 | Provided on the Virtex-II reference board |
| HSTL_III | 0.90 | Provided on the Virtex-II reference board |
| HSTL_IV | 0.90 | Provided on the Virtex-II reference board |
| SSTL2_I | 1.25 | Provided on the Virtex-II reference board |
| SSTL2_II | 1.25 | Provided on the Virtex-II reference board |
| SSTL3_I | 1.50 | Provided on the Virtex-II reference board |
| SSTL3_II | 1.50 | Provided on the Virtex-II reference board |
| AGP-2X/AGP | 1.32 | Not provided on the Virtex-II reference board |
| SSTL2_I_DCI | 1.25 | Provided on the Virtex-II reference board |
| SSTL2_II_DCI | 1.25 | Provided on the Virtex-II reference board |

| | | |
|---|---|---|
| SSTL3_I_DCI | 1.50 | Provided on the Virtex-II reference board |
| SSTL3_II_DCI | 1.50 | Provided on the Virtex-II reference board |
| HSTL_I_DCI | 0.75 | Provided on the Virtex-II reference board |
| HSTL_II_DCI | 0.75 | Provided on the Virtex-II reference board |
| HSTL_III_DCI | 0.90 | Provided on the Virtex-II reference board |
| HSTL_IV_DCI | 0.90 | Provided on the Virtex-II reference board |
| GTL_DCI | 0.80 | Not provided on the Virtex-II reference board |
| GTLP_DCI | 1.00 | Provided on the Virtex-II reference board |

### 2.11.1 Bank Reference Voltage Generation

The following figure shows how the bank reference voltage is generated on the Virtex-II reference board. Two 1x3 jumpers are used on each Virtex-II bank to generate various reference voltages ranging from 0.75V to 1.5V. The following circuit is replicated on each bank to allow maximum flexibility for bank reference voltage generation.

The Source Voltage Jumper allows the selection of the 1.5V or the 2.5V supply as the source voltage to the reference voltage generator circuit while the Source Resistor Jumper provides various voltage divide capability for this circuit. The output of the resistor divider is fed into an Operational Amplifier prior to reaching the Virtex-II VREF input pins.

**Reference Voltage in a Virtex-II Bank**

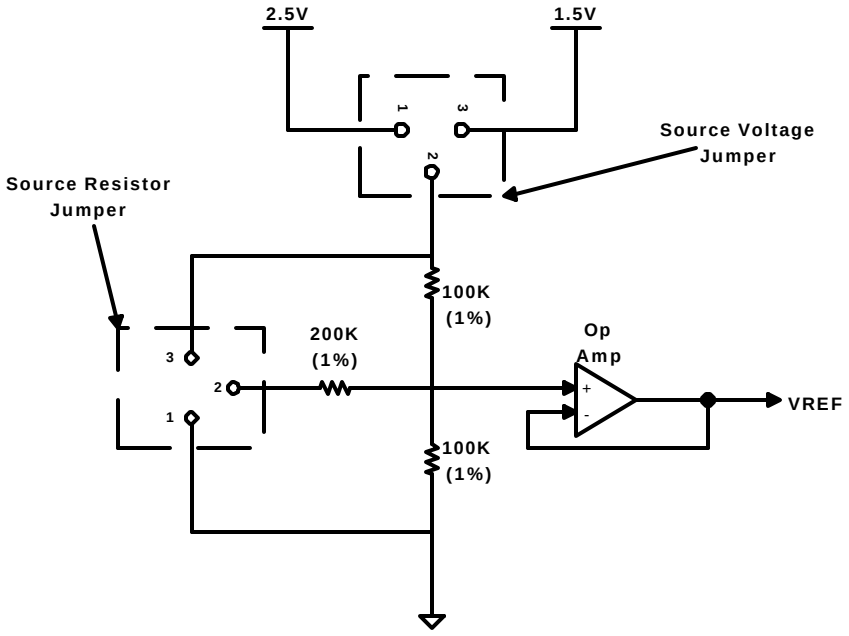


**Figure 13 – Reference Voltage in a Virtex-II Bank**

Each bank of the Virtex-II FPGA has a dedicated Source Voltage jumper and a Source Resistor jumper. The following figure shows the Source Voltage and Resistor jumpers for each Virtex-II bank.

**Table 11 - Virtex-II Bank Source Voltage and Resistor Jumpers**

| Bank # | Source Voltage Jumper | Source Resistor Jumper |
|---|---|---|
| 0 | JP16 | JP18 |
| 1 | JP16 | JP19 |
| 2 | JP16 | JP22 |
| 3 | JP16 | JP23 |
| 4 | JP24 | JP26 |
| 5 | JP24 | JP27 |
| 6 | JP24 | JP30 |
| 7 | JP24 | JP31 |

### 2.11.2 Bank Reference Voltage Jumper Settings

The following figure shows the Source Voltage and Resistor jumper settings for each Virtex-II bank. This table must be used along with the above table (bank specific jumpers) to set the bank reference voltage to the desired value.

**Table 12 - Virtex-II Bank Reference Voltage Jumper Settings**

| Source Voltage Jumper | | Source Resistor Jumper | | Bank VREF |
|---|---|---|---|---|
| 1-2 | 2-3 | 1-2 | 2-3 | |
| Closed | Open | Open | Open | 1.25V |
| Closed | Open | Open | Closed | 1.50V |
| Closed | Open | Closed | Open | 1.00V |
| Open | Closed | Open | Open | 0.75V |
| Open | Closed | Open | Closed | 0.90V |
| Open | Closed | Closed | Open | 0.60V |
| Open | Open | NA | NA | 0.00V |

## 2.12 Bank Reference Resistors

In order to support high-speed I/O interfaces, which require output signals with fast edge rates, terminations would be needed to prevent reflections and maintain signal integrity. High pin count packages (especially ball grid arrays) cannot accommodate external termination resistors. XC2V40/XC2V1000 DCI provides controlled impedance drivers and on-chip termination for single-ended I/Os. This eliminates the need for external resistors, and improves signal integrity.

The DCI feature can be used on any IOB by selecting one of the DCI I/O standards. When applied to inputs, DCI provides input parallel termination. When applied to outputs, DCI provides controlled impedance drivers (series termination) or output parallel termination. DCI operates independently on each I/O bank. When a DCI I/O standard is used in a particular I/O bank, external reference resistors must be connected to two dual-function pins on the bank. These resistors, voltage reference of N transistor (VRN) and the voltage reference of P transistor (VRP) are shown in the following figure.

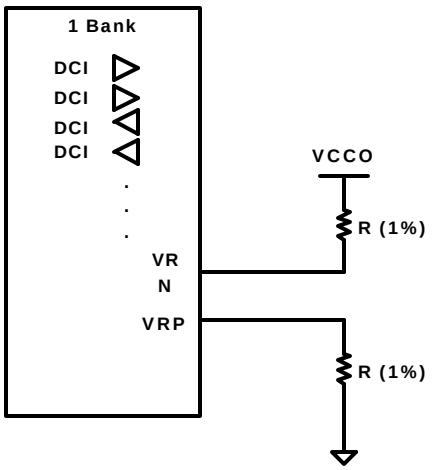


**Figure 14 – DCI in a Virtex-II Bank**

When used with a terminated I/O standard, the value of the resistor is specified by the standard (typically 50 Ohms). When used with a controlled impedance driver, the resistor sets the output impedance of the driver within the specified range (25 Ohms to 150 Ohms). The resistors connected to VRN and VRP do not need to be the same value. 1% resistors are recommended.

The figure below shows the reference resistors connected to the Virtex-II FPGA on the reference board followed by a table that shows a summary of the reference resistors. It should be noted that all resistors for banks 1-4 and bank 7 are 50 Ohms with 1% variation. Bank 5 and 6 of the Virtex-II FPGA are used to implement a 4-bit bi-directional LVDS port. For these two banks, the VRN and VRP pins are used as I/O pins and are utilized in the implementation of the LVDS port. Hence, the reference resistors are not provided for on these two banks.

The VRN and VRP within the bank 0 of the Virtex-II FPGA are connected to two Potentiometers, R56 and R57 respectively. These potentiometers are 500 Ohms in series with 24 Ohms. Hence, the range would be 24-524 Ohms. Utilizing these potentiometers for bank 0 makes this bank extremely flexible for various standard I/O design.

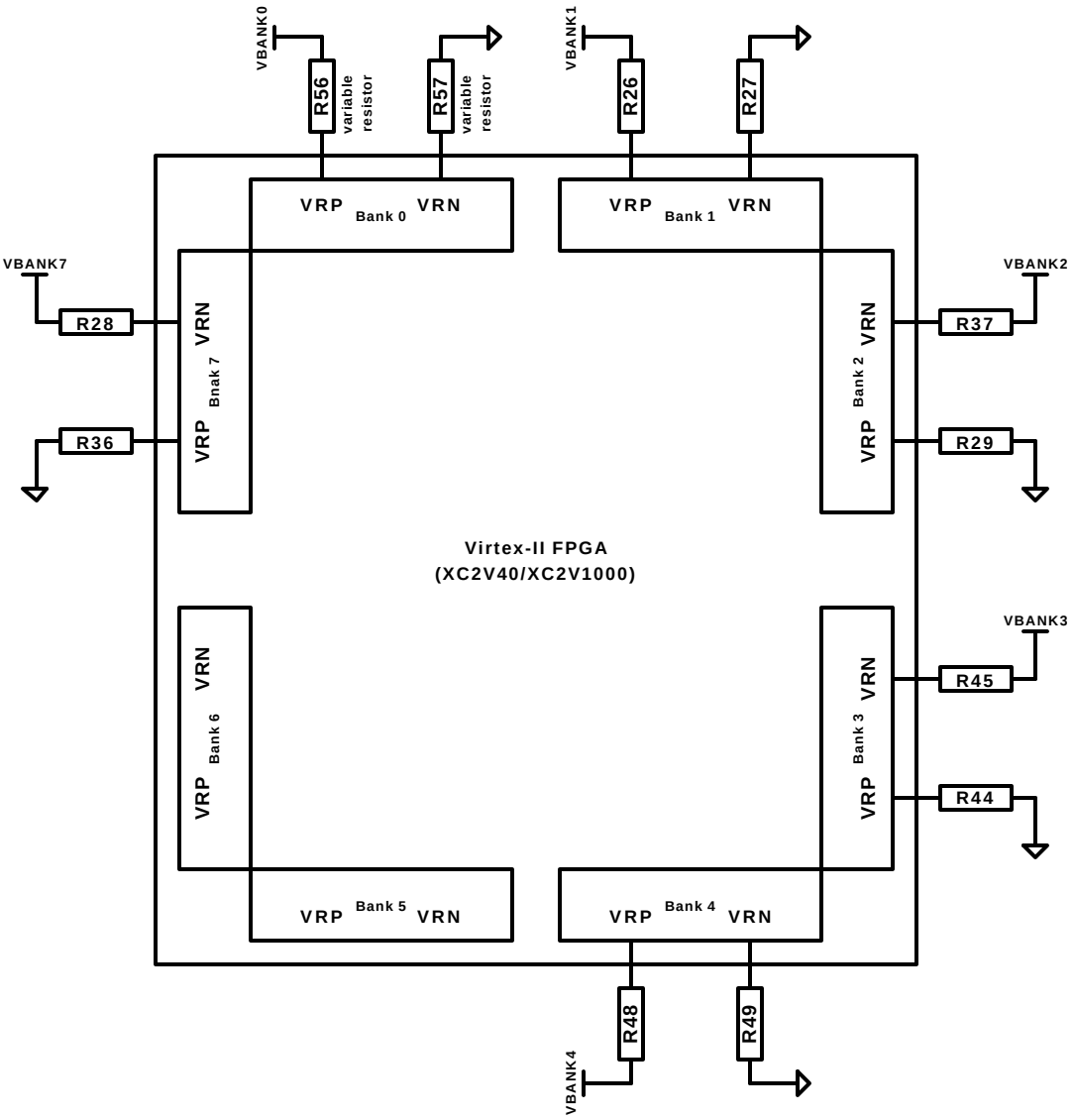


**Figure 15 – Virtex-II DCI Reference Resistors**

**Table 13 - Virtex-II Reference Resistors Summary**

| Bank # | VRN/VRP (Ohms) | Description |
|---|---|---|
| 0 | 24-524 potentiometer | VRN /VRP can be set to a value from 24 to 524 Ohms. |
| 1 | 50/50 Ohms | Both VRN and VRP are set to 50 Ohms resistors. |
| 2 | 50/50 Ohms | Both VRN and VRP are set to 50 Ohms resistors. |
| 3 | 50/50 Ohms | Both VRN and VRP are set to 50 Ohms resistors. |
| 4 | 50/50 Ohms | Both VRN and VRP are set to 50 Ohms resistors. |
| 5 | No resistors | VRN and VRP are used as I/O pins. |
| 6 | No resistors | VRN and VRP are used as I/O pins. |
| 7 | 50/50 Ohms | Both VRN and VRP are set to 50 Ohms resistors. |

## 2.13 DCI Demonstration

The following figure shows how the Virtex-II reference board can be used to demonstrate the effect of DCI. The bank 0 of the Virtex-II FPGA will be used for this demonstration. Two variable reference resistors (24-524 Ohms) are connected to the VRN and VRP pins of this bank. In order to perform this test, the following steps must be taken:

1. Set the VCCO of bank 0 to 2.5V as described earlier
2. Place a jumper on pins 32 and 34 of the J11 User I/O connector (this would provide a loopback, which would effectively provide a load on the Virtex-II output pin D5).
3. Program the Virtex-II FPGA with a design that would take the test_input signal (100Mhz) as an input and sets the dci_out signal to the test_input signal. For this step of the test, no DCI buffer is used for the dci_out output signal.
4. Connect a scope to the test points (JP43 and JP44) and view the dci_out output signal. Document any overshot and/or undershoot present on this signal.
5. Modify the design in step 3 to include DCI input and output buffers (IBUF_LVDS_25 and OBUF_LVDS_25) for the dci_out and dci_in signals. These two buffers would effectively provide source and load terminations for the dci_out signal.
6. Connect a scope to the test points (JP43 and JP44) and view the dci_out output signal while varying R57 and R56 reference resistors. Document any overshot and/or undershoot present on this signal and compare the results with results obtained in step 4.

This test will show how the DCI feature of the Virtex-II FPGA can be used to provide source and load terminations on a high-speed signal and match these terminations to the impedance of the transmission line in order to minimize the signal overshoot and undershoot.

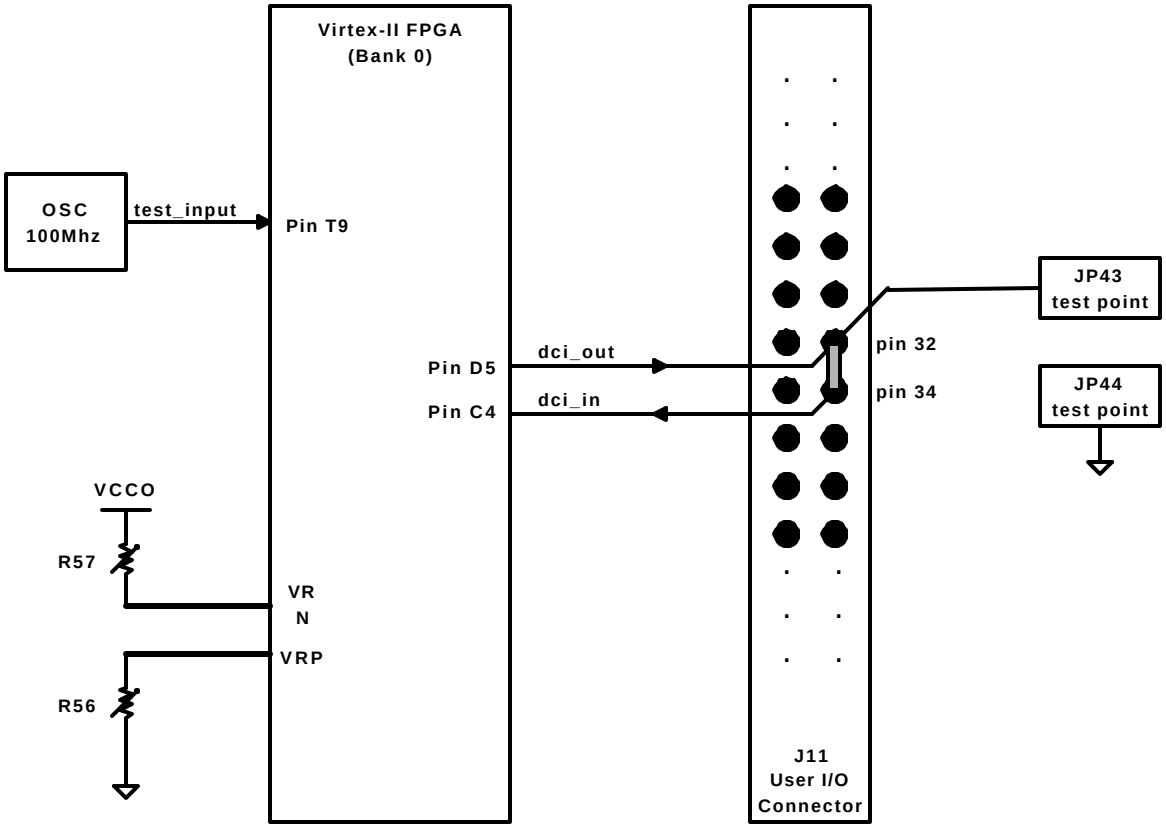


**Figure 16 – DCI Test setup**

## 2.14 Virtex-II Power Down Mode

The Virtex-II FPGA family utilizes a dedicated pin called PWRDWN_B that can be used to place the Virtex-II FPGA into a low-power and inactive state. In the normal operating mode, the PWRDWN_B pin would be pulled up. Forcing the PWRDWN_B pin to logic 0 would place the Virtex-II FPGA in power-down mode. The following figure shows the Virtex-II Power Down on the Virtex-II reference board.

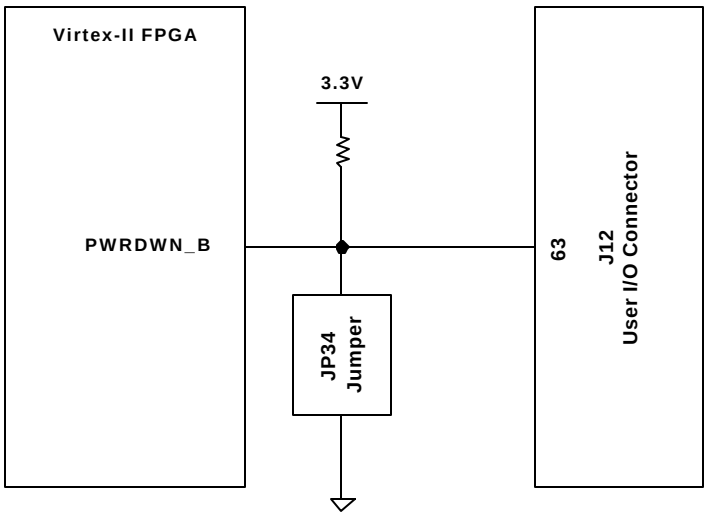


**Figure 17 – Virtex-II Power Down Mode**

As shown in the above figure, the Virtex-II FPGA can be placed in the power-down mode on the Virtex-II reference board by closing the JP34 jumper (permanently placing it in the power-down mode until the jumper is removed), or by forcing the pin 63 of the J12 User I/O connector to logic 0 state. The Virtex-II reference board users can use this pin to place the Virtex-II FPGA in the power-down mode momentarily.

The Virtex-II FPGA provides Power-Down status information via the DONE pin if the PWRDWN_STAT option is selected using BitGen. The DONE pin is asserted upon entry to the power-down mode. After a successful wake-up, the DONE status pin is de-asserted (The wake-up sequence is the reverse of the power-down sequence). While in power-down mode, the only active pins are the PWRDWN_B and DONE. All inputs are off and all outputs are 3-stated.

While in the Power-Down state, the Power On Reset (POR) circuit is still active, but it does not reset the device if VCCINT, VCCO, or VCCAUX falls below its minimum value. The POR circuit waits until the PWRDWN_B pin is released before resetting the device. Also, the PROG_B pin is not sampled while the device is in the Power-Down state. The PROG_B pin becomes active when the PWRDWN_B pin is released. Therefore, the device cannot be reset while in the Power-Down state.

## 2.15 Virtex-II VBAT

The Virtex-II VBAT input pin (pin A14) is connected to the 3.3V supply on the Virtex-II reference board through the JP42 jumper. The 2x1 header for JP42 is not installed on the board allowing customers to install the jumper should they choose to drive the VBAT pin.

## 2.16 ISP PROM

The Virtex-II reference board utilizes the Xilinx XC18V512 or XC18V04 ISP PROM, allowing FPGA designers to quickly download revisions of a design and verify the design changes in order to meet the final system-level design requirements. The XC18V512/04 ISP PROM uses two interfaces to accomplish the configuration of the Virtex-II FPGA. The XC18V512 is used on the XC2V40 board while the XC18V04 is used on the XC2V1000 board.

The JTAG port on the XC18V512/04 device is used to program the PROM with the design bit file. Once the XC18V512/04 has been programmed, the user can initiate the configuration of the Virtex-II device by asserting the PROGn signal. Upon activation of the PROGn signal (SW1), the XC18V512/04 device will use its FPGA Configuration Port to configure the Virtex-II FPGA. The Virtex-II Configuration Port consists of the PROGn, INITn, CEn, CCLK, and the DIN signals. The following figure shows the ISP PROM interface to the JTAG port and the Virtex-II FPGA configuration port.

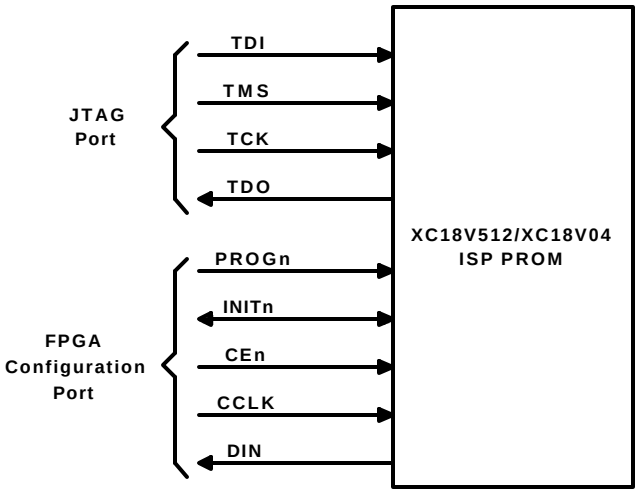


**Figure 18 – ISP PROM Interface**

## 2.17 LVDS Port

The Virtex-II reference board provides a complete high-performance differential signaling (LVDS) interface, enabling the designers to prototype high-speed serial communication links. The Virtex-II I/Os are designed to comply with the IEEE electrical specifications for LVDS to make system and board design easier. With the addition of an LVDS current-mode driver in the IOBs, which eliminates the need for external source termination in point-to-point applications, and with the choice of two different voltage modes and an extended mode, Virtex-II devices provide the most flexible solution for doing an LVDS design in an FPGA.

### 2.17.1 LVDS Port Interface

The design of the LVDS port on this reference board allows data widths of 1 to 4 bits in addition to the LVDS differential clock signal. The 4 transmit data signals, 4 receive data signals, and the transmit and receive clocks can be used to prototype various high performance and high speed interfaces. The following figure shows the LVDS interface on the Virtex-II reference board. LVDS termination networks are provided between the Virtex-II FPGA and the LVDS user connectors. It should be noted that no LVDS source terminations are needed when using the Virtex-II FPGA family in point-to-point applications.

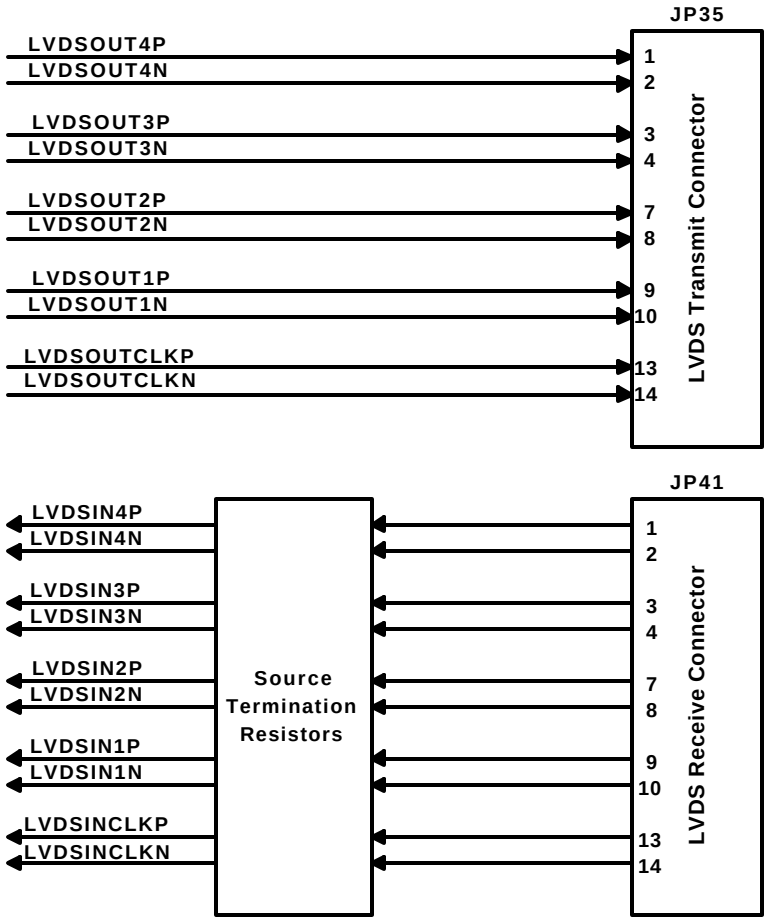


**Figure 19 – LVDS Transmit and Receive Ports**

### 2.17.2 LVDS Port Signal Descriptions

The following table shows the LVDS port signal descriptions and the port signal assignments to the Virtex-II FPGA.

**Table 14 - LVDS Transmit Port Signal Descriptions**

| Signal Name | Virtex-II Pin # | J35 Pin # | Description |
|---|---|---|---|
| LVDSOUT4P | P1 | 1 | Positive Data Transmit Bit 4 |
| LVDSOUT4N | N1 | 2 | Negative Data Transmit Bit 4 |
| LVDSOUT3P | N3 | 3 | Positive Data Transmit Bit 3 |
| LVDSOUT3N | N2 | 4 | Negative Data Transmit Bit 3 |
| GND | NA | 5 | Ground |
| GND | NA | 6 | Ground |
| LVDSOUT2P | J4 | 7 | Positive Data Transmit Bit 2 |
| LVDSOUT2N | J3 | 8 | Negative Data Transmit Bit 2 |
| LVDSOUT1P | J2 | 9 | Positive Data Transmit Bit 1 |
| LVDSOUT1N | J1 | 10 | Negative Data Transmit Bit 1 |
| GND | NA | 11 | Ground |
| GND | NA | 12 | Ground |
| LVDSOUTCLKP | H1 | 13 | Positive Transmit Clock |
| LVDSOUTCLKN | H2 | 14 | Negative Transmit Clock |
| GND | NA | 15 | Ground |
| GND | NA | 16 | Ground |

**Table 15 - LVDS Receive Port Signal Descriptions**

| Signal Name | Virtex-II Pin # | J41 Pin # | Description |
|---|---|---|---|
| LVDSIN4P | N8 | 1 | Positive Data Receive Bit 4 |
| LVDSIN4N | P8 | 2 | Negative Data Receive Bit 4 |
| LVDSIN3P | R8 | 3 | Positive Data Receive Bit 3 |
| LVDSIN3N | T8 | 4 | Negative Data Receive Bit 3 |
| GND | NA | 5 | Ground |
| GND | NA | 6 | Ground |
| LVDSIN2P | N5 | 7 | Positive Data Receive Bit 2 |
| LVDSIN2N | P5 | 8 | Negative Data Receive Bit 2 |
| LVDSIN1P | P4 | 9 | Positive Data Receive Bit 1 |
| LVDSIN1N | R4 | 10 | Negative Data Receive Bit 1 |
| GND | NA | 11 | Ground |
| GND | NA | 12 | Ground |
| LVDSINCLKP | T3 | 13 | Positive Receive Clock |
| LVDSINCLKN | T4 | 14 | Negative Receive Clock |
| GND | NA | 15 | Ground |
| GND | NA | 16 | Ground |

### 2.18 User I/O Connectors

The following figure shows the user I/O connectors located on the Virtex-II reference board. All Virtex-II I/O pins with the exception of the LVDS port, the user clock outputs, and the user DDR memory interface are available to the user via these two 64-pin connectors. The LVDS signals are available to the user via J34 and J36 connectors, while the user clock outputs would be accessible by the user via J17 and J18. The DDR memory interface signals would be available as test points via JP40 and JP41 connectors (the pin assignments to these two connectors are described in a later section).

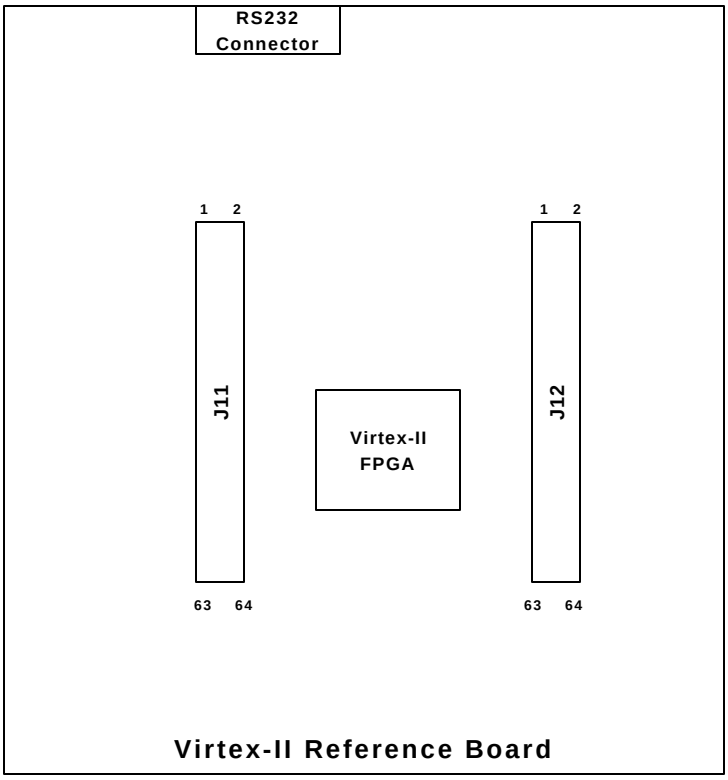


**Figure 20 – Virtex-II Reference Board I/O Connectors**

### 2.18.1 User I/O Connectors Signal Assignments

The following tables show the Virtex-II pin assignments to the user I/O connectors (J11 & J12).

**Table 16 - J12 User I/O Connector**

| Signal Name | Virtex-II Pin # | J12 Pin # | Signal Name | Virtex-II Pin # | J12 Pin # |
|---|---|---|---|---|---|
| 1.5V | NA | 1 | V1000.L14 | L14 | 33 |
| 2.5V | NA | 2 | V1000.L15 | L15 | 34 |
| 1.8V | NA | 3 | V1000.L12 | L12 | 35 |
| 3.3V | NA | 4 | V1000.L13 | L13 | 36 |
| GND | NA | 5 | V1000.M15 | M15 | 37 |
| GND | NA | 6 | V1000.M16 | M16 | 38 |
| TCK | A15 | 7 | V1000.T11 | T11 | 39 |
| TDI | C2 | 8 | V1000.T12 | T12 | 40 |
| TMS | B14 | 9 | V1000.M11 | M11 | 41 |
| TDO | C15 | 10 | V1000.P11 | P11 | 42 |
| GND | NA | 11 | V1000.P10 | P10 | 43 |
| GND | NA | 12 | V1000.N11 | N11 | 44 |
| FPGA.DISPLAY5 | C9 | 13 | V1000.M10 | M10 | 45 |
| FPGA.DISPLAY6 | D9 | 14 | V1000.N10 | N10 | 46 |
| FPGA.DISPLAY4 | B9 | 15 | FPGA.J13 | J13 | 47 |
| FPGA.DISPLAY3 | A9 | 16 | FPGA.J14 | J14 | 48 |
| FPGA.DISPLAY0 | D12 | 17 | GND | NA | 49 |

| | | | | | |
|---|---|---|---|---|---|
| FPGA.DISPLAY1 | C12 | 18 | GND | NA | 50 |
| FPGA.DISPLAY7 | A10 | 19 | FPGA.DIP8 | J15 | 51 |
| FPGA.DISPLAY2 | B13 | 20 | FPGA.DIP7 | J16 | 52 |
| GND | NA | 21 | FPGA.DIP6 | M13 | 53 |
| GND | NA | 22 | FPGA.DIP5 | N16 | 54 |
| FPGA.ULED | C13 | 23 | FPGA.DIP4 | P16 | 55 |
| FPGA.C16 | C16 | 24 | FPGA.DIP3 | T14 | 56 |
| FPGA.D16 | D16 | 25 | FPGA.DIP2 | R13 | 57 |
| FPGA.E13 | E13 | 26 | FPGA.DIP1 | T10 | 58 |
| FPGA.H13 | H13 | 27 | CLK.SMB | R9 | 59 |
| FPGA.H14 | H14 | 28 | CLK.SMBALT | N9 | 60 |
| FPGA.H15 | H15 | 29 | CLK.CAN1 | T9 | 61 |
| FPGA.H16 | H16 | 30 | CLK.CAN2 | P9 | 62 |
| GND | NA | 31 | FPGA.PWRDWN | T15 | 63 |
| GND | NA | 32 | GND | NA | 64 |

**Table 17 - J11 User I/O Connector**

| Signal Name | Virtex-II Pin # | J11 Pin # | Signal Name | Virtex-II Pin # | J11 Pin # |
|---|---|---|---|---|---|
| 3.3V | NA | 1 | NC | NA | 33 |
| 3.3V | NA | 2 | FPGA.C4 | C4 | 34 |
| NC | NA | 3 | 1.8V | NA | 35 |
| NC | NA | 4 | 1.8V | NA | 36 |
| GND | NA | 5 | FPGA.C1 | C1 | 37 |
| GND | NA | 6 | NC | NA | 38 |
| NC | NA | 7 | NC | NA | 39 |
| NC | NA | 8 | FPGA.D1 | D1 | 40 |
| NC | NA | 9 | FPGA.H3 | H3 | 41 |
| NC | NA | 10 | FPGA.H4 | H4 | 42 |
| GND | NA | 11 | GND | NA | 43 |
| GND | NA | 12 | GND | NA | 44 |
| NC | NA | 13 | V1000.L2 | L2 | 45 |
| NC | NA | 14 | V1000.L3 | L3 | 46 |
| NC | NA | 15 | V1000.L4 | L4 | 47 |
| NC | NA | 16 | V1000.M1 | M1 | 48 |
| NC | NA | 17 | GND | NA | 49 |
| NC | NA | 18 | GND | NA | 50 |
| 2.5V | NA | 19 | V1000.M2 | M2 | 51 |
| 2.5V | NA | 20 | V1000.M6 | M6 | 52 |
| NC | NA | 21 | V1000.L5 | L5 | 53 |
| NC | NA | 22 | V1000.T6 | T6 | 54 |
| NC | NA | 23 | V1000.T5 | T5 | 55 |
| FPGA.A7 | A7 | 24 | V1000.N6 | N6 | 56 |
| FPGA.SP0 | C8 | 25 | V1000.P6 | P6 | 57 |
| FPGA.SP1 | D8 | 26 | V1000.P7 | P7 | 58 |
| GND | NA | 27 | V1000.N7 | N7 | 59 |
| GND | NA | 28 | V1000.M7 | M7 | 60 |
| FPGA.A8 | A8 | 29 | FPGA.PUSH1 | M4 | 61 |
| FPGA.B8 | B8 | 30 | FPGA.PUSH2 | T7 | 62 |
| FPGA.C5 | C5 | 31 | GND | NA | 63 |
| FPGA.D5 | D5 | 32 | GND | NA | 64 |

## 2.19 DDR Memory Test Connectors

The following figure shows the DDR memory test connectors (JP14 & JP15). These connectors are provided on the Virtex-II reference board for test purposes and they should not be used as extension of the DDR memory interface.

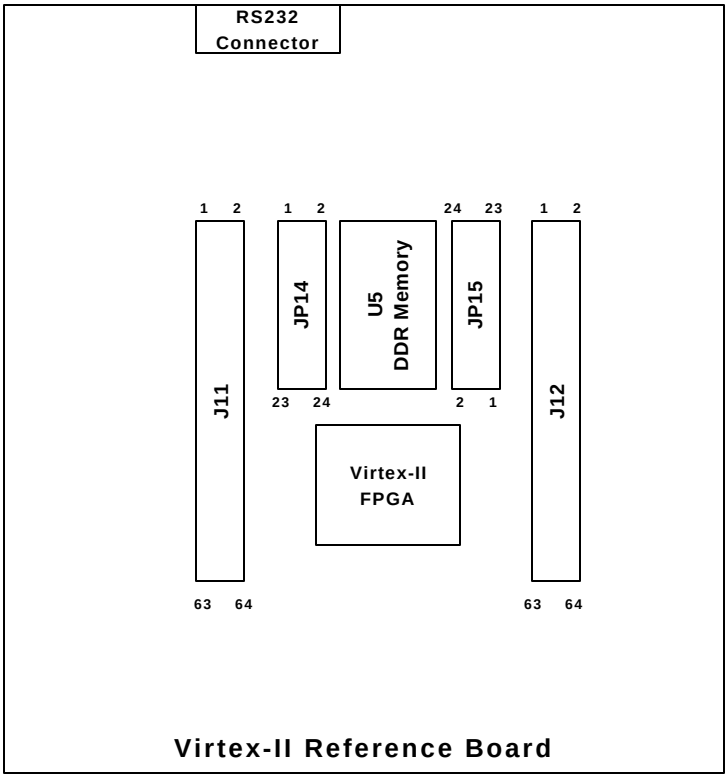


**Figure 21 – DDR Memory Interface Test Connectors**

### 2.19.1 DDR Memory Test Connectors Signal Assignments

The following tables show the Virtex-II pin assignments to the DDR memory test connectors.

**Table 18 – JP14 DDR Memory Test Connector**

| Signal Name | Virtex-II Pin # | JP14 Pin # | Signal Name | Virtex-II Pin # | JP14 Pin # |
|---|---|---|---|---|---|
| GND | NA | 1 | MEM.WEn | F4 | 13 |
| GND | NA | 2 | MEM.CASn | F5 | 14 |
| MEM.D0 | L1 | 3 | MEM.RASn | E1 | 15 |
| MEM.D1 | K2 | 4 | MEM.CSn | E2 | 16 |
| MEM.D2 | K3 | 5 | MEM.BS0 | A6 | 17 |
| MEM.D3 | K4 | 6 | MEM.BS1 | B6 | 18 |
| MEM.D4 | G2 | 7 | MEM.A10/AP | E6 | 19 |
| MEM.D5 | G3 | 8 | MEM.A0 | C6 | 20 |
| MEM.D6 | G4 | 9 | MEM.A1 | C7 | 21 |
| MEM.D7 | F1 | 10 | MEM.A2 | D7 | 22 |
| MEM.LDQS | F2 | 11 | MEM.A3 | E7 | 23 |
| MEM.LDM | F3 | 12 | GND | NA | 24 |

**Table 19 – JP15 DDR Memory Test Connector**

| Signal Name | Virtex-II Pin # | JP15 Pin # | Signal Name | Virtex-II Pin # | JP15 Pin # |
|---|---|---|---|---|---|
| GND | NA | 1 | MEM.CLKn | F14 | 13 |
| GND | NA | 2 | MEM.UDM | F13 | 14 |
| MEM.A4 | E10 | 3 | MEM.UDQS | F15 | 15 |
| MEM.A5 | D10 | 4 | MEM.D8 | F16 | 16 |
| MEM.A6 | C10 | 5 | MEM.D9 | G15 | 17 |
| MEM.A7 | A11 | 6 | MEM.D10 | G14 | 18 |
| MEM.A8 | B11 | 7 | MEM.D11 | G13 | 19 |
| MEM.A9 | C11 | 8 | MEM.D12 | K15 | 20 |
| MEM.A11 | E11 | 9 | MEM.D13 | K14 | 21 |
| MEM.A12 | E16 | 10 | MEM.D14 | K13 | 22 |
| MEM.CKE | E15 | 11 | MEM.D15 | L16 | 23 |
| MEM.CLK | F12 | 12 | GND | NA | 24 |

## 2.20 Program Switch (SW1)

The Virtex-II reference board provi des a push button switch for initiating the configuration of the Virtex-II FPGA. This switch is used when the XC18V512/04 ISP PROM configures the Virtex-II FPGA. After programming of the XC18V512/04 ISP PROM, this switch can assert the PROGn signal. Upon activation of the PROGn signal, the XC18V512/04 ISP PROM initiates the configuration of the Virtex-II FPGA.

## 2.21 Voltage Regulators

The following figure shows the voltage regulators that are used on the Virtex-II reference board to provide various on-board voltage sources. As shown in the following figure, JP12 connector is used to provide the main 5.0V voltage to the board. This voltage source is provided to all on-board regulators to generate the 1.5V, 1.8V, 2.5V, and 3.3V voltages.

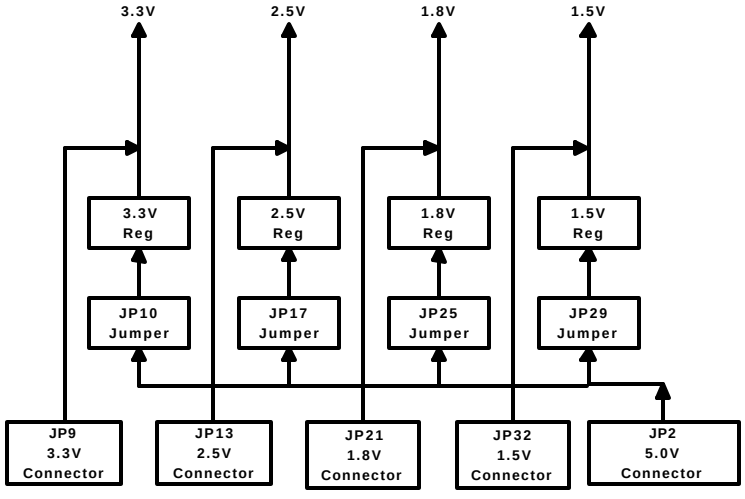


**Figure 22 – Virtex-II Reference Board Voltage Regulators**

For any one of the on-board voltages (1.5V 1.8V, 2.5V, and 3.3V), if the current provided by the on-board regulator is not sufficient for some applications, the user can directly drive the voltage

source and bypass the on-board regulators. This can be accomplished by removing jumpers JP10, JP17, JP25, and JP29 for voltages 3.3V through 1.5V respectively.

### 2.21.1 Voltage Regulators Jumper Settings

The following table shows the jumper setting for the 3.3V, 2.5V, 1.8V, and the 1.5V supply voltages on the Virtex-II reference board.

**Table 20 - Voltage Regulators Jumper Settings**

| Jumper | Jumper Setting | 3.3V Source | 2.5V Source | 1.8V Source | 1.5V Source |
|---|---|---|---|---|---|
| JP10 | Open | External 3.3V supply via JP9 connector | NA | NA | NA |
| | Closed | On-board 3.3V regulator | NA | NA | NA |
| JP17 | Open | NA | External 2.5V supply via JP13 connector | NA | NA |
| | Closed | NA | On-board 2.5V regulator | NA | NA |
| JP25 | Open | NA | NA | External 1.8V supply via JP21 connector | NA |
| | Closed | NA | NA | On-board 1.8V regulator | NA |
| JP29 | Open | NA | NA | NA | External 1.5V supply via JP32 connector |
| | Closed | NA | NA | NA | On-board 1.5V regulator |

### 2.22 Virtex-II Configuration Mode Select

The following table shows the Virtex-II Configuration Mode Select jumper settings. The jumper position 7-8 (M3) is connected to the HSWAP_EN pin of the Virtex-II FPGA. When this jumper is closed, the Virtex-II internal I/O pull-ups are enabled during the configuration.

**Table 21 - Virtex-II Configuration Mode Select**

| Mode | PC Pull-up | J14 | | | |
|---|---|---|---|---|---|
| | | 1-2 (M0) | 3-4 (M1) | 5-6 (M2) | 7-8 (M3) |
| Master Serial | Yes | Closed | Closed | Closed | Closed |
| Master Serial | No | Open | Closed | Closed | Closed |
| Slave Parallel | Yes | Closed | Open | Closed | Closed |
| Slave Parallel | No | Open | Open | Closed | Closed |
| JTAG | Yes | Closed | Closed | Open | Open |
| JTAG | No | Open | Closed | Open | Open |
| Slave Serial | Yes | Closed | Open | Open | Open |
| Slave Serial | No | Open | Open | Open | Open |

## 3 Design Download

The Virtex-II reference board supports multiple methods of configuring the Virtex-II FPGA. The JTAG port on the Virtex-II reference board can be used to directly configure the Virtex-II FPGA, or to program the on-board XC18V512/04 ISP PROM. Once the ISP PROM is programmed, it can be used to configure the Virtex-II FPGA. The following sections provide a brief description of each method of configuring the Virtex-II FPGA.

### 3.1 JTAG Interface

The J1 JTAG connector on the Virtex-II reference board can be used to configure the Virtex-II or to program the on-board XC18V512/04 ISP PROM. The following figure shows the setup for using the JTAG port on the Virtex-II reference board. The Insight JTAG cable is connected to the Virtex-II reference board via J1 at one end and to the PC parallel port at the other end.

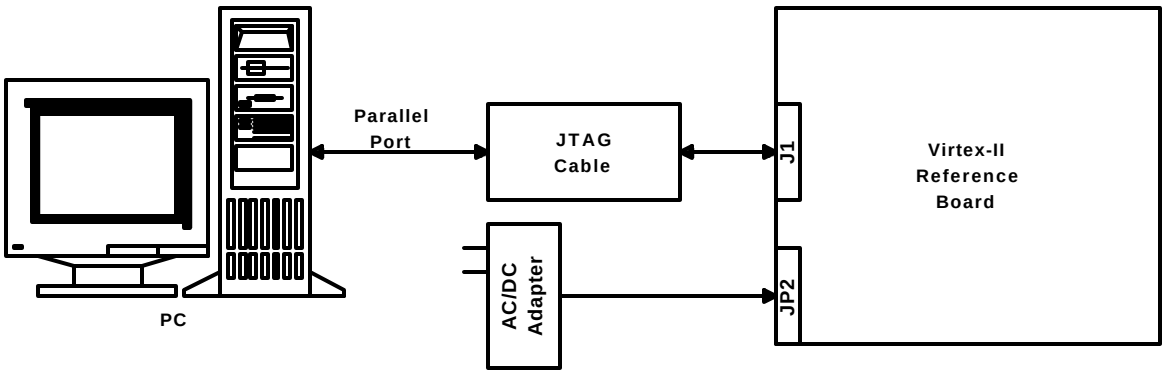


**Figure 23 – JTAG Download Setup**

#### 3.1.1 Configuring the Virtex-II FPGA

When the JTAG port is used to configure the Virtex-II FPGA, the following steps must be taken:

- Using Table 21 set the Configuration Mode of the Virtex-II FPGA to JTAG Mode.
- The on-board 18V512/04 ISP PROM is placed in the Bypass Mode in the Xilinx programming window. You will need to associate the ISP PROM with either a dummy .mcs file, or a .bsd file to allow the JTAG programming software to pass data through the ISP PROM.
- Close jumper JP7 (if no JTAG devices are connected to the USER I/O connector).
- The design .bit file is used to download the design into the Virtex-II FPGA.

#### 3.1.2 Programming the XC18V512/04 ISP PROM

When the JTAG port is used to program the ISP PROM, the following steps must be taken:

- Using Table 21 set the Configuration Mode of the Virtex-II FPGA to Master Serial Mode.
- The Virtex-II FPGA is placed in the Bypass Mode in the Xilinx programming window. You will need to associate the FPGA with either a dummy .bit file or a .bsd file to allow the JTAG programming software to pass data through the FPGA.
- Close jumper JP7 (if no JTAG devices are connected to the USER I/O connector).
- The design .mcs file is used to download the design into the 18V512/04 ISP PROM.
- Upon programming of the 18V512/04 ISP PROM, the on-board PROGn push button switch (SW1) is used to initiate the Virtex-II FPGA configuration.