

SN54AS756, SN74AS756, SN74AS757 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

SDAS040B – DECEMBER 1983 – REVISED JANUARY 1995

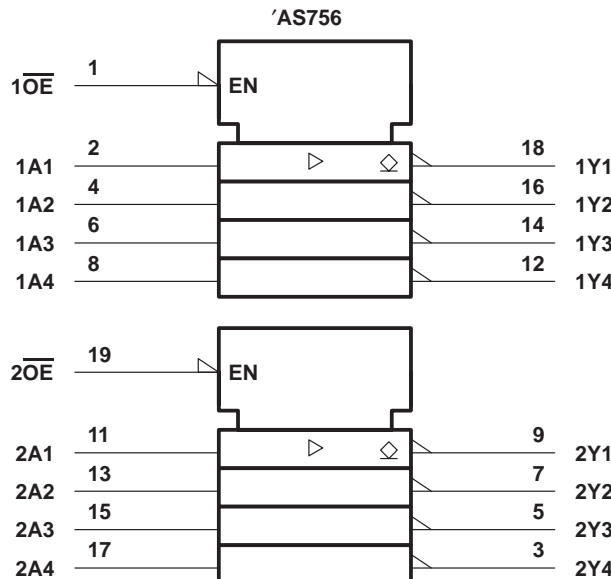
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- Eliminate the Need for 3-State Overlap Protection
- pnp Inputs Reduce dc Loading
- Open-Collector Versions of 'AS240A and 'AS241
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

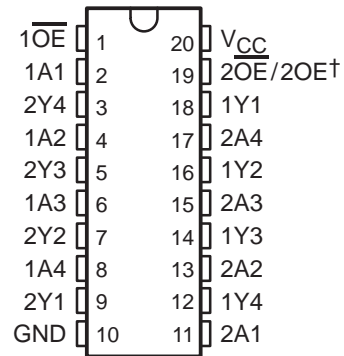
These octal buffers and line drivers are designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for 3-state overlap protection. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable (\overline{OE}) inputs, and complementary OE and \overline{OE} inputs. These devices feature high fan-out and improved fan-in.

The SN54AS756 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS756 and SN74AS757 are characterized for operation from 0°C to 70°C .

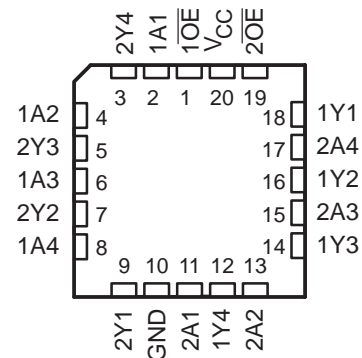
logic symbols†



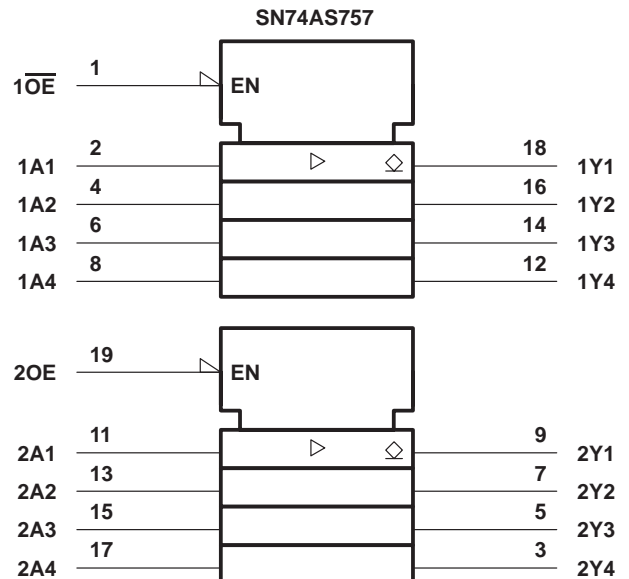
SN54AS756 . . . J PACKAGE
SN74AS756, SN74AS757 . . . DW OR N PACKAGE
(TOP VIEW)



SN54AS756 . . . FK PACKAGE
(TOP VIEW)



† $2OE$ for 'AS756 or $2OE$ for SN74AS757



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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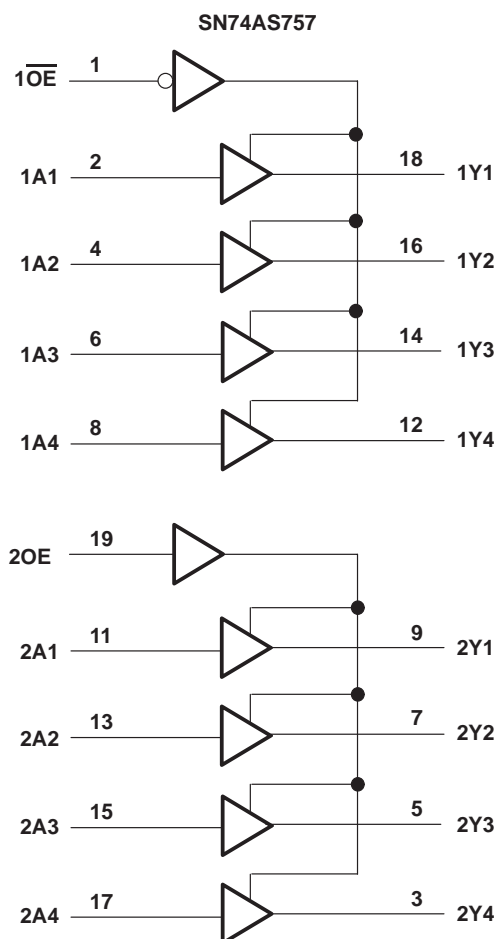
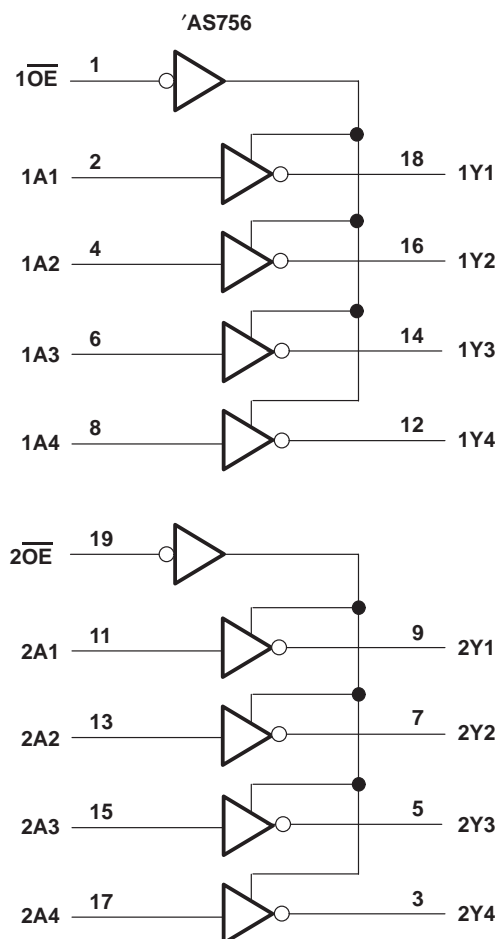
SN54AS756, SN74AS756, SN74AS757

OCTAL BUFFERS AND LINE DRIVERS

WITH OPEN-COLLECTOR OUTPUTS

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logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Off-state output voltage	7 V
Operating free-air temperature range, T_A : SN54AS756	–55°C to 125°C
SN74AS756, SN74AS757	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS756			SN74AS756 SN74AS757			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS756		SN74AS756 SN74AS757		UNIT
				MIN	TYP†	MAX	MIN	
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$				–1.2	–1.2	V
I_{OH}		$V_{CC} = 4.5\text{ V}$, $V_{OH} = 5.5\text{ V}$				0.1	0.1	mA
V_{OL}		$V_{CC} = 4.5\text{ V}$ $I_{OL} = 48\text{ mA}$				0.55		V
		$I_{OL} = 64\text{ mA}$					0.55	
I_I		$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$				0.1	0.1	mA
I_{IH}		$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$				20	20	μA
I_{IL}	A inputs of SN74AS757 only	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$				–1	–1	mA
	All other inputs					–0.5	–0.5	
I_{CC}	'AS756	$V_{CC} = 5.5\text{ V}$	Outputs high	9	15	9	15	mA
			Outputs low	51	80	51	80	
	SN74AS757	$V_{CC} = 5.5\text{ V}$	Outputs high	21	33	21	33	
			Outputs low	61	95	61	95	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

SN54AS756, SN74AS756, SN74AS757

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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54AS756		SN74AS756		
			MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	3	20	3	19	ns
t _{PHL}			1	7	1	6	
t _{PLH}	$\overline{\text{OE}}$	Y	3	22	3	19.5	ns
t _{PHL}			1	8.5	1	7.5	

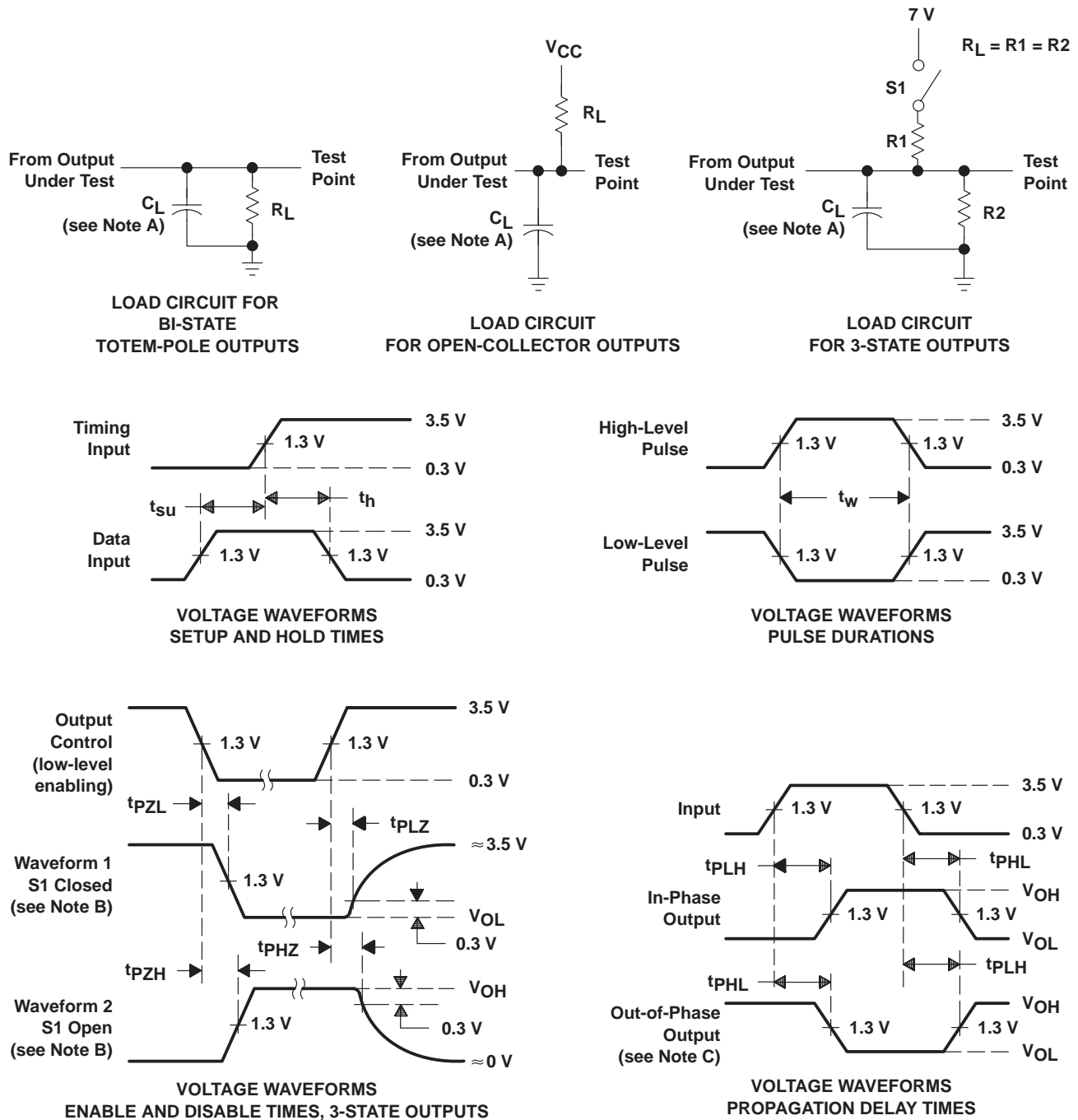
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX†		UNIT
			SN74AS757		
			MIN	MAX	
t _{PLH}	A	Y	3	18.5	ns
t _{PHL}			1	6	
t _{PLH}	1 $\overline{\text{OE}}$	1Y	3	20	ns
t _{PHL}			1	7	
t _{PLH}	2OE	2Y	3	21	ns
t _{PHL}			1	7.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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