Xilinx Parallel Cable IV

DS097 (v2.0) January 15, 2004

Preliminary Product Specification

Features

- Download speed of up to 5 Megabits per second (Mb/s)
- Over eight times faster than Xilinx Parallel Cable III using Xilinx iMPACT (v4.2i or higher) download software
- ChipScope™ Pro compatible
- In-System Programs configures all Xilinx devices
  - Virtex™/Virtex-E/Virtex-II/Virtex-II Pro™
  - Spartan™/Spartan-XL/Spartan-II/Spartan-IIE/ Spartan-3
  - XC9500™/XC9500XL/XC9500XV
  - CoolRunner™ (XPLA3)/CoolRunner-II
  - XC18V00™ ISP PROM family
  - XC4000XL™/XV/EX/E
  - System ACE™ Multi-Package Module (MPM)
  - Platform Flash PROM family
- Automatically senses and adapts to correct I/O voltage
- Interfaces to devices operating at 5V (TTL), 3.3V (LVTTL), 2.5V, 1.8V, and 1.5V
- Supports JTAG (IEEE 1149.1) and Xilinx Slave Serial Modes
- J Drive IEEE 1532 Programming Engine compatible
- Includes high-performance ribbon cable
- Compliant with IEEE 1284 Level 2 Electrical Specification
- Externally powered using keyboard/mouse splitter cable or AC power brick
- LED status indicator
- Compatible with ECP-compliant I/O controllers for high-speed, bidirectional communication

Parallel Cable IV Description

The new Xilinx Parallel Cable IV (PC4) (Figure 1) is a high-speed download cable that configures or programs all Xilinx FPGA, CPLD, ISP PROM, and System ACE MPM devices. The cable takes advantage of the IEEE 1284 ECP protocol and Xilinx iMPACT software to increase download speeds over eight times faster than existing solutions. The cable automatically senses and adapts to target I/O voltages and is able to accommodate a wide range of I/O standards from 1.5V to 5V. PC4 is designed for use in a desktop environment.

PC4 supports the widely used industry standard IEEE 1149.1 Boundary Scan (JTAG) specification using a four-wire interface. It also supports the Xilinx Slave Serial mode for Xilinx FPGA devices. It interfaces to target systems using a ribbon cable that features integral alternating ground leads to reduce crosstalk and improve signal integrity.

The cable is externally powered from either a power “brick” or by interfacing to a standard PC mouse or keyboard connection. A bi-color status LED indicates the presence of operating and target reference voltages.

Figure 1: **Xilinx Parallel Cable IV**

Connecting to Host Computer

The PC4 connects to any PC using Microsoft® Windows® 2000 or Windows® XP operating systems through the standard IEEE 1284 DB25 parallel (printer) port connector. To fully utilize the higher speeds of this cable, the host PC must have a parallel port that is enabled to support extended capability port (ECP) mode

If ECP mode is not enabled, the PC4 will default to compatibility mode and will not run at the optimum speeds listed.

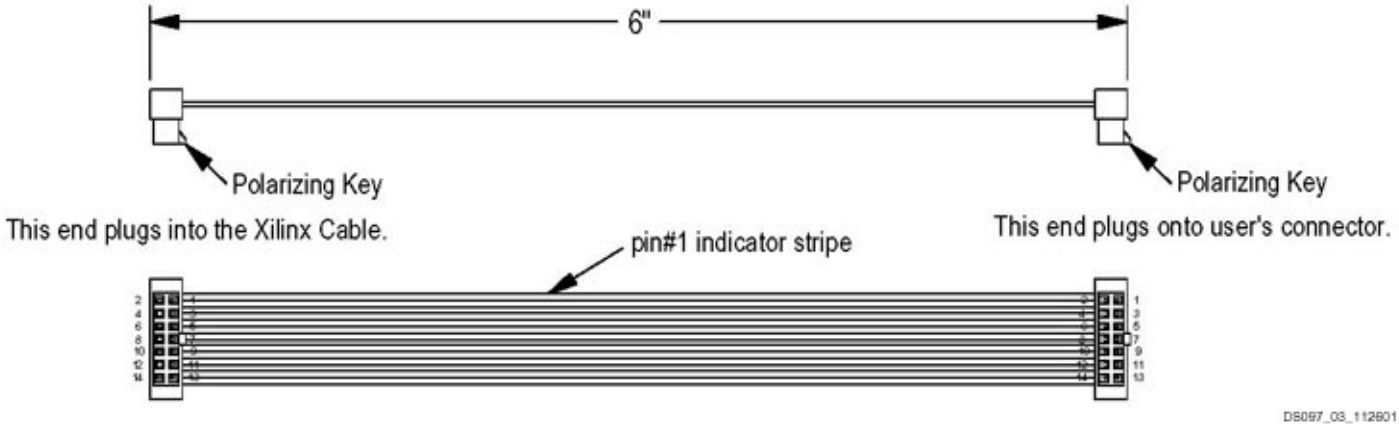
Notes:
1. Refer to host PC BIOS to see if ECP mode is enabled.

High Performance Ribbon Cable

An insulation displacement (IDC) ribbon cable is supplied and recommended for connection to target systems. See Figure 2 and Figure 3. This cable incorporates multiple signal-ground pairs and facilitates error-free connection. A very small footprint, keyed mating connector is all that is required on the target system. Refer to Figure 4 for the appropriate connector pin assignments and sample vendor part numbers. Figure 5 shows the POD and its dimensions.

The Parallel Cable IV can also interface to target systems using "flying lead wires." However, these are not included with PC4 and can be purchased separately from the Xilinx E-Commerce web site.

Figure 2: **High Performance Ribbon Cable**



Notes:
1. Ribbon Cable - 14 conductor 1.0mm centers Round Conductor Flat Cable; 28 AWG (7x36) stranded copper conductors; gray PVC with pin 1 edge marked.
2. 2mm Ribbon Female Polarized Connectors - IDC connection to ribbon; contacts are beryllium copper plated; 30 micro inches gold plating over 50 micro inches nickel; connectors mate to 0.5mm square posts on 2mm centers.

Figure 3: **Ribbon Cable Diagram**

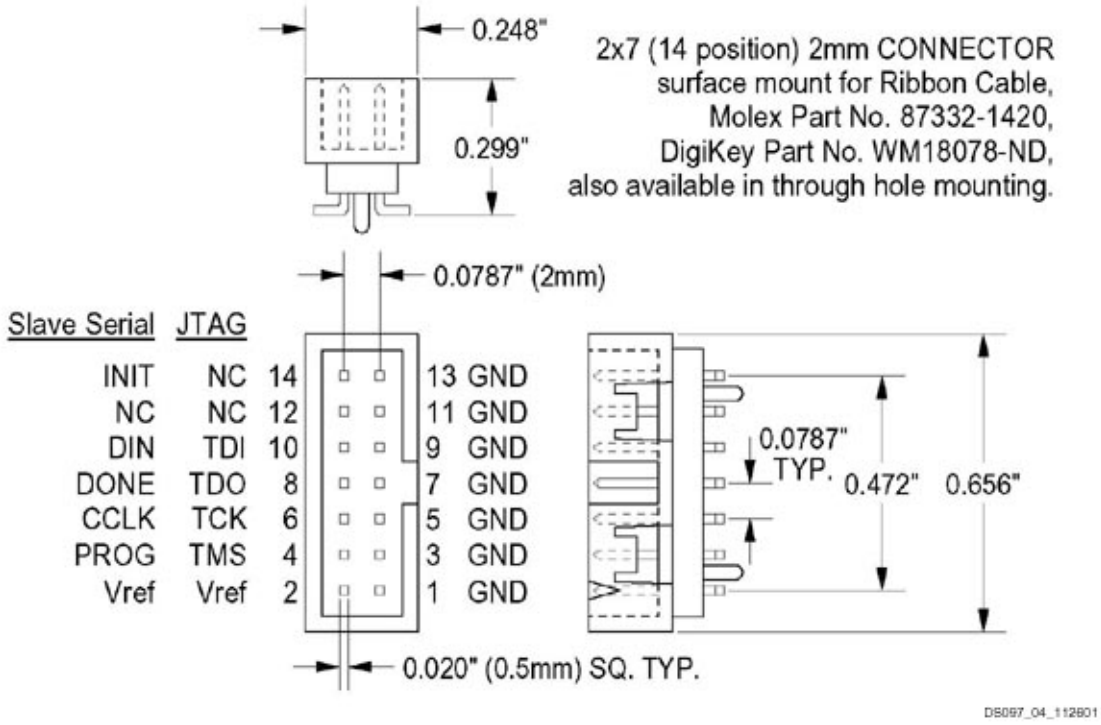


Figure 4: **Target Interface Connector Signal Assignments**

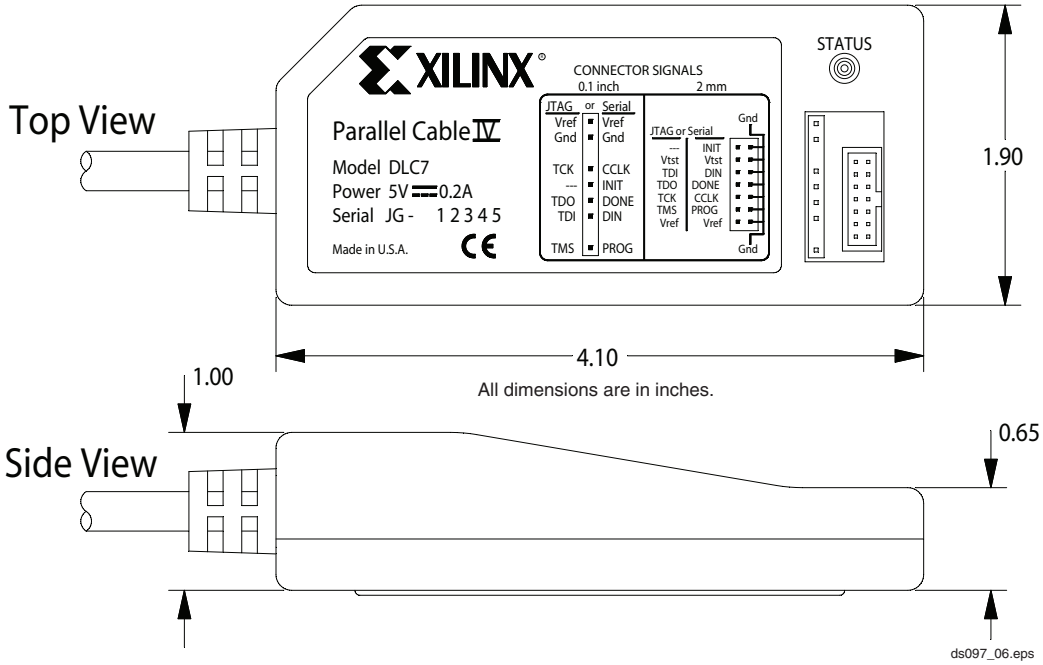


Figure 5: **Diagram of POD with Dimensions**

Table 1 provides some third-party sources for mating connectors that are compatible with the Parallel Cable IV ribbon cable.

Table 1: **Mating Connectors for 2mm pitch, 14 Conductor Ribbon Cable**

Manufacturer	SMT, Vertical	SMT, Right Angle	Through-Hole, Vertical	Through-Hole, Right Angle	Web Site
Molex	87332-1420	N/A	87331-1420	87333-1420	www.molex.com
FCI	98424-G52-14	N/A	98414-G06-14	98464-G61-14	www.fciconnect.com
Comm Con Connectors	2475-14G2	N/A	2422-14G2	N/A	www.commcon.com

Pinout Assignments

Note: Pins not listed are no connects.

Table 2: **PC4 Target Interface Connector Signal Assignments**

Pin Name		Type	Flying Lead Wires	Ribbon Cable	Description
JTAG	Slave Serial				
TDI		Out	2	10	**Test Data In**. This is the target serial input data stream for JTAG operations and should be connected to the TDI pin on the first ISP device in the JTAG chain.
TDO		In	3	8	**Test Data Out**. This is the target serial output data stream for JTAG operations and should be connected to the TDO pin on the last ISP device in the JTAG chain.
TCK		Out	5	6	**Test Clock**. This is the clock signal for JTAG operations and should be connected to the TCK pin on all target ISP devices that share the same data stream.
TMS		Out	1	4	**Test Mode Select**. This is the JTAG mode signal that establishes appropriate TAP state transitions for target ISP devices. It should be connected to the TMS pin on all target ISP devices that share the same data stream.
	INIT	In/Out	4	14	**Configuration Initialize**. This pin indicates that configuration memory is being cleared. It should be connected to the INIT_B pin of the target FPGA in a single device system or to the INIT_B pin on all FPGAs in daisy-chained configurations.
	DIN	Out	2	10	**Configuration Data Input**. This is the serial input data stream for target FPGA(s). It should be connected to the DIN pin of the target FPGA in a single device system or to the DIN pin of the first FPGA in daisy-chained configurations.
	DONE	In	3	8	**Configuration Done**. This pin indicates to PC4 that the target FPGA(s) have received the entire configuration bit stream. It should be connected to the DONE pin on all FPGAs for daisy-chained configurations. Additional CCLK cycles will be issued following the positive transition of DONE to ensure that the configuration process is complete.
	CCLK	Out	5	6	**Configuration Clock**. In slave-serial configuration mode, FPGAs are configured by loading one bit per CCLK cycle. CCLK should be connected to the CCLK pin on the target FPGA for a single device system or to the CCLK pin of all FPGAs in daisy-chained configurations.

Table 2: **PC4 Target Interface Connector Signal Assignments *(Continued)***

Pin Name		Type	Flying Lead Wires	Ribbon Cable	Description
JTAG	Slave Serial				
	PROG	Out	1	4	**Configuration Reset**. This pin is used to force a reconfiguration of the target FPGA(s). It should be connected to the PROG_B pin of the target FPGA in a single device system or to the PROG_B pin of all FPGAs in daisy-chained configurations.
V_{TST}	V_{TST}	Out		12	**Test Driver**. This pin is reserved for Xilinx diagnostics and should not be connected to any target circuitry.
V_{REF}	V_{REF}	In	7	2	**Target Reference Voltage**. This pin should be connected to a voltage bus on the target system that supplies the JTAG or slave serial interface. For example, when communicating with CoolRunner II device using the JTAG interface, V_{REF} should be connected to the target VAUX bus. V_{REF} must be connected to a regulated voltage. There must not be any current limiting resistor.
GND	GND	-	6	1, 3, 5, 7, 9, 11, 13	**Digital Ground**.

TDO Timing Specifications

When using JTAG configuration mode, target systems must guarantee that TDO signal assertion meets a minimum setup time relative to the positive edge of TCK. Buffers or multiplexers in the target hardware can add phase delays as long as the following setup specification is not violated. Figure 6 illustrates the relationship between TCK and TDO for the 5 MHz default PC4 configuration speed.

All PC4 signal transitions are synchronized to an internal 40 MHz system clock (SCLK). TDO is asserted by the last device in the target JTAG chain on the negative edge of TCK. Setup and hold times for TDO are referenced to the next positive edge of TCK.

In Figure 6, TDO represents the signal from the last device in the JTAG chain. TDO_internal is the worst case representation of the same signal at the PC IV connector accounting for propagation delays introduced by target buffers and/or multiplexers.

TDO_internal is sampled on a positive edge of SCLK 12.5 ns prior to the negative edge of TCK. When using TCK as the reference, TDO_internal must be stable no later than 42 ns after the positive edge of TCK and must remain valid until 88 ns after the positive edge of TCK.

When the PC IV configuration clock rate is changed to a lower frequency, there is additional margin for propagation delay through target buffers. Any design that complies with the margins specified for 5 MHz operation is guaranteed to operate at lower frequencies.

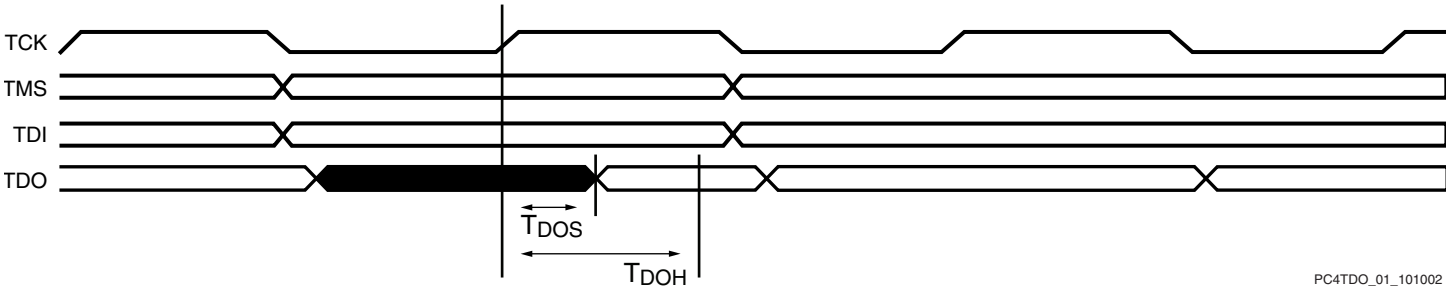


Figure 6: **TDO Timing Diagram**

Table 3: **TDO Timing Specifications**

Selected Frequency	Symbol	Parameter	Min	Max	Units
5 MHz	T_{DOS}	TDO setup time	–42		nS
	T_{DOH}	TDO hold time	88		nS
200 kHz	T_{DOS}	TDO setup time	–2442		nS
	T_{DOH}	TDO hold time	2488		nS

Cable Power

The host interface cable (Figure 7) includes a short power jack for connection to one of two possible +5V DC power sources: (1) the keyboard or mouse part of the host PC or (2) an external AC adapter. The supplied power splitter cable is required when using the first option. The splitter cable is installed between the mouse cable and the standard 6-pin mini-DIN connector on the host PC.

PC4 operating current is less than 100 mA. It draws approximately 15 mA from the target reference voltage bus to power the JTAG/Slave Serial buffers.

Figure 8 shows a PC4 cable connection to a laptop.

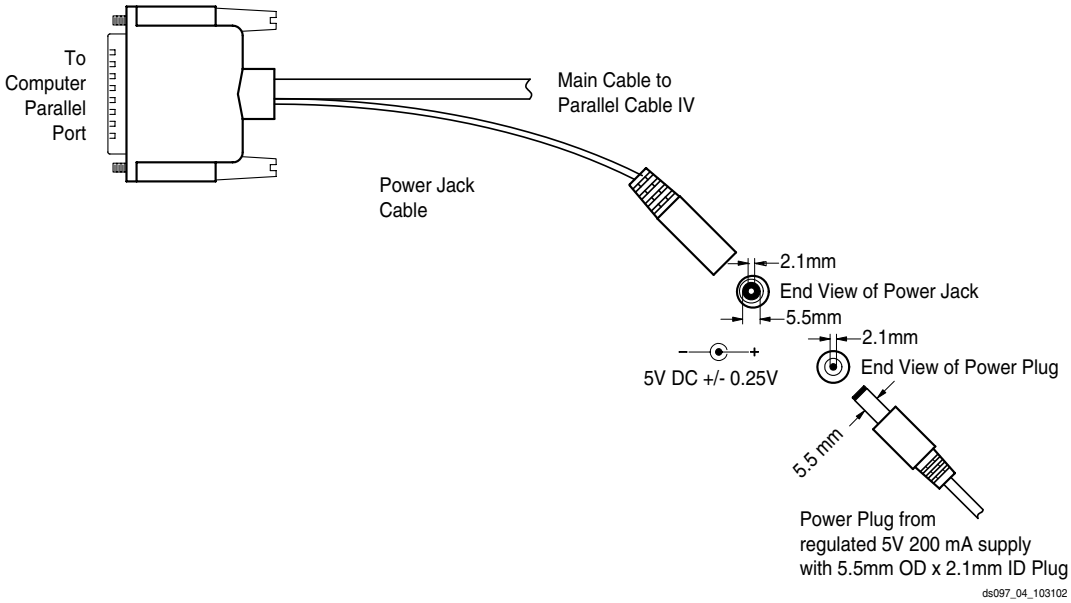


Figure 7: **Optional Power Brick Connection to Parallel Cable IV**

Figure 8: **Laptop PC4 Cable Connection**

Power Supply Sources

Table 4 provides some third-party sources for power supplies that are compatible with the Parallel Cable IV.

Table 4: **Power Supply Sources**(1,2)

Part Number	Description	Manufacturer	URL	Distributor	Distributor Part Number
DTS050240U/AC1-P5P(3)	5V, 12W, 3 Prong Inlet	CUI Stack	www.cuistack.com	DigiKey	T805-P5P-ND
DTS050250SUDC-P5P	5V, 12W, 2 Prong Inlet	CUI Stack	www.cuistack.com	DigiKey	T850-P5P-ND
FW1805-S760(3)	5V, 15W, 3 Prong Inlet	Elpac	www.elpac.com	-	-

Notes:
1. The external power supply must provide a regulated +5.0V DC @ 200 mA minimum.
2. The PC4 *pigtail* connector will only mate with a power supply that uses a 2.1mm plug on its DC output cable.
3. The 3-Prong Inlet power supplies are recommended for international use so that a variety of AC plug styles can be accommodated with a single power supply.

Status LED

The Status LED will indicate one of two possible conditions as shown in the following table.

LED State	Operating Condition
Solid Green	Power available to POD and V_{REF} detected.
Solid Amber	Power available to POD but no V_{REF} detected.

Notes:
1. If LED does not turn on, check to make sure that power has been connected to the PC4 either through the mouse/keyboard port, or through the external power connector.

Automatic I/O Voltage Sensing

Although JTAG configuration pins have typically operated at 3.3V or 5.0V, new devices support voltages as low as 1.5V. Voltage levels for Slave-Serial configuration pins follow the respective I/O bank voltage, which can be in the range from 1.5V to 5.0V. Consequently, the PC4 output buffers must be capable of driving at the voltage level expected by the receiving devices. The V_{REF} pin on the target device is used to bias the PC4 output buffers.

A sensing circuit continuously monitors the V_{REF} pin. If V_{REF} drops below 1.3V DC, all output buffers are 3-stated to avoid any possible damage when connected to a non-powered target system.

All pins are protected against continuous shorts to ground or voltages up to 5.5V DC.

IEEE 1284 Cable Specifications

Level 1 compliant host ports are designed to operate over a maximum cable length of 10 ft. Level 2 compliant host ports will operate over a maximum cable length of 33 ft. PC4 uses a Level 2 compliant cable interface buffer.

For more cable information, see the following web site:
http://www.xilinx.com/support/programr/cables.htm

Signal Integrity Issues

The PC4 uses high slew rate buffers to drive TCK, TMS, and TDI. Users should pay close attention to proper PCB layout and signal termination to avoid transmission line effects. Users are encouraged to refer to the Xilinx "Signal Integrity" documentation and the application note XAPP361 on the Xilinx web site.

PC4 Operating Characteristics

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply Voltage	5.5	V
T_A	Operating Temperature Range	0° to +70°	C
T_{STG}	Storage Temperature Range	–40° to +85°	C
P_D	Power Dissipation	750	mW
I_{OUT}	DC Output Current (TDI, TCK, TMS, INIT)	±32	mA

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	DC Supply Voltage	External P/S	4.75	5.25	V
V_{REF}	Target Reference Voltage		1.5	5.5	V
I_{CC}	Operating Current		60	100	mA
I_{REF}	Reference Current		6.0	15.0	mA
V_{OH}	High Level Output Voltage	V_{REF} = 3.3V DC, I_{OH} = –4 mA	2.7	-	V
V_{OL}	Low Level Output Voltage	V_{REF} = 3.3V DC, I_{OL} = +4 mA	-	0.36	V
V_{IH}	High Level Input Voltage	V_{REF} > 1.5V	1.2	-	V
V_{IL}	Low Level Input Voltage	V_{REF} > 1.5V	-	0.4	V

Ordering Information

The device number is HW-PC4.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/26/01	1.0	Initial Xilinx release.
11/30/01	1.1	Changed to Advance Product Specification.
01/21/02	1.2	Fixed the links in Table 4.
02/06/02	1.3	Added **Signal Integrity Issues** on page 5.
03/08/02	1.4	Added Ordering Information.
03/12/02	1.5	Updated **Features** on page 1.
03/03/03	1.6	Added TDO timing specification, pinout descriptions, desktop environment statement, Figure 8, fixed broken link.
04/14/03	1.7	Added Spartan-3 to supported devices list, plus other edits.
04/29/03	1.8	Added "Platform Flash family" to **Features**.
05/21/03	1.9	Fixed broken link on page 7.

Date	Version	Revision
01/15/04	2.0	• Changed status of data sheet from Advance to Preliminary. • Updated compatible PC operating systems (Win2000 and WinXP). • Added Figure 5 (POD diagram). • Updated FCI connector part numbers, Table 1. • Changed textual references to cable from "PC IV" to "PC4".