Device Packaging and Thermal Characteristics

UG112 (v1.0) January 31, 2004

XILINX®

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The following table shows the revision history for this document.

Date	Version	Revision
01/31/04	1.0	Initial release

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Chapter 1

Package Information

Package Overview

Introduction to Xilinx Packaging

Electronic packages are interconnectable housings for semiconductor devices. The major functions of the electronic packages are to provide electrical interconnections between the IC and the board and to efficiently remove heat generated by the device.

Feature sizes are constantly shrinking, resulting in increased number of transistors being packed into the device. Today's submicron technology is also enabling large-scale functional integration and moving toward system-on-a-chip solution. In order to keep pace with these new advancements in silicon technologies, semiconductor packages have also evolved to provide improved device functionality and performance.

Feature size at the device level is driving package feature sizes down to the design rules of the early transistors. To meet these demands, electronic packages must be flexible to address high pin counts, reduced pitch and form factor requirements. At the same time, packages must be reliable and cost effective.

Packaging Technology at Xilinx

At Xilinx, a wide range of leaded as well as array packages have been developed to meet the design / performance requirements of today's advanced IC devices. Array package families such as standard overmolded PBGAs, thermally enhanced "Cavity Down" BGAs, and small form factor CSPs (Chip Scale Packages) are offered to address the issues of pin counts / density requirements while offering superior electrical performance as compared to their leaded counterparts.

Package Drawings

Package drawings are available online at the Package Drawings page on xilinx.com.

Specifications and definitions

Inches vs. Millimeters

The JEDEC standards for PLCC, CQFP, and PGA packages define package dimensions in inches. The lead spacing is specified as 25, 50, or 100 mils (0.025", 0.050" or 0.100").

The JEDEC standards for PQFP, HQFP, TQFP, VQFP, CSP, and BGA packages define package dimensions in millimeters. The leadframe packages have lead spacings of 0.5 mm,

0.65 mm, or 0.8 mm. The CSP and BGA packages have ball pitches of 0.5, 0.8, 1.00, or 1.27 mm.

Because of the potential for measurement discrepancies, this Data Book provides measurements in the controlling standard only, either inches or millimeters.

Pressure Handling Capacity

For the Flipchip BGA that has been surface mounted, a direct compressive (non varying) force applied NORMALLY to the lid with a tool head that coincides with the lid or is slightly bigger will not cause any damage to the flipchip balls or external balls, provided the force does not exceed 3.0 grams per external ball and the device and board are supported to prevent any flexing or bowing. Forces greater than this may work, however if the forces will exceed this limit, a careful finite element analysis will be in order.

The PC board needs to be properly supported to prevent any flexing resulting from such a force. Any bowing resulting from such a force can likely damage the package to board connections. It is suggested that any complicated mounting arrangement needs to be modeled with respect to the thermal stresses that can result from the heating of the device.

Clockwise or Counterclockwise

The orientation of the die in the package and the orientation of the package on the PC board affect the PC board layout. PLCC and PQFP packages specify pins in a counterclockwise direction, when viewed from the top of the package (the surface with the Xilinx logo). PLCCs have pin 1 in the center of the beveled edge while all other packages have pin 1 in one corner, with one exception: The 100-pin and 165-pin CQFPs (CB100 and CB164) for the XC3000 devices have pin 1 in the center of one edge.

CQFP packages specify pins in a clockwise direction, when viewed from the top of the package. The user can make the pins run counterclockwise by forming the leads such that the logo mounts against the PC board. However, heat flow to the surrounding air is impaired if the logo is mounted down.

‘Cavity-Up’ or ‘Cavity-Down’

Most Xilinx devices attach the die against the inside bottom of the package (the side that does not carry the Xilinx logo). Called “cavity-up,” this has been the standard IC assembly method for over 25 years. This method does not provide the best thermal characteristics. Pin Grid Arrays (greater than 130 pins), copper based BGA packages, and Ceramic Quad Flat Packs are assembled “Cavity Down,” with the die attached to the inside top of the package, for optimal heat transfer to the ambient air. More information on Xilinx's “Cavity-Up” packages and “Cavity-Down” packages can be found in the Packaging Technology Briefs section.

For most packages this information does not affect how the package is used because the user has no choice in how the package is mounted on a board. For Ceramic Quad Flat Pack (CQFP) packages however, the leads can be formed to either side. Therefore, for best heat transfer to the surrounding air, CQFP packages should be mounted with the logo up, facing away from the PC board.

Package Technology Briefs

‘Cavity-Up’ Plastic BGA Packages

BGA is a plastic package technology that utilizes area array solder balls at the bottom of the package to make electrical contact with the system circuit board. The area array format of solder balls reduces package size considerably when compared to leaded products. It also results in improved electrical performance as well as having higher manufacturing yields.

The substrate is made of a mutilayer BT (bismaleimide triazene) epoxy-based material. Power and ground pins are grouped together and the signal pins are assigned in the perimeter format for ease of routing on to the board. The package is offered in a die up format and contains a wirebonded device that is covered with a mold compound.

Package Construction

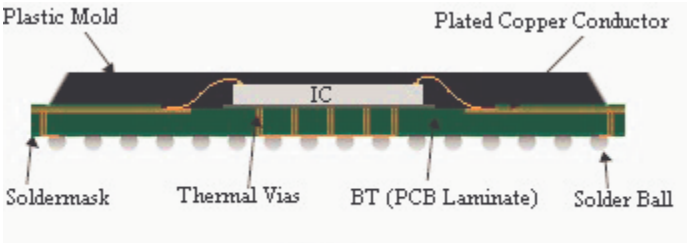


Figure 1-1: **BGA Package ‘Cavity-Up’ Ball Grid Array Packages**

As shown in the cross section of Figure 1-1, the BGA package contains a wire bonded die on a single-core printed circuit board with an overmold. Beneath the die are the thermal vias which can dissipate the heat through a portion of the solder ball array and ultimately into the power and ground planes of the system circuit board. This thermal management technique provides better thermal dissipation than a standard PQFP package. Metal planes also distribute the heat across the entire package, enabling a 15–20% decrease in thermal resistance to the case.

Key Features/Advantages of Xilinx ‘Cavity-Up’ BGA Packages

- High board assembly yield since board attachment process is self-centering
- SMT compatible, resulting in minimum capital investment
- Extendable to multichip modules
- Low profile and small footprint
- Improved electrical performance (short wire length)
- Enhanced thermal performance
- Passes Jedec L3 moisture level conditioning
- Excellent board level reliability

Xilinx ‘Cavity-Up’ BGA Offerings

Xilinx BGAs come in three different pitches: 1.27 mm, 1.5 mm, and 1.00 mm. The 1.0 mm pitch BGAs are part of the Fine Pitch BGA family. By using the Fine Pitch BGAs, a significant reduction in PCB real estate can be achieved. Furthermore, Fine Pitch BGAs provide more I/Os for the same real estate as compared to the standard BGA packages.

Table 1-1: **'Cavity-Up' BGA Packages**

Package Code	Ball Count	Body Size (mm)	Ball Pitch (mm)	Ball Pattern
BG225	225	27 x 27	1.5	Full Array
BG256	256	27 x 27	1.27	Full Array
FT256	256	17 x 17	1.0	Full Array
BG388	388	35 x 35	1.27	Peripheral Array
FG256	256	17 x 17	1.0	Full Array
FG484	484	23 x 23	1.0	Full Array
FG556	556	31 x 31	1.0	Peripheral Array
FG324	324	23 x 23	1.0	Peripheral Array
FG456	456	23 x 23	1.0	
FG320	320	19 x 19	1.0	Full Array
BG492	492	35 x 35	1.0	
FG676	676	27 x 27	1.0	Full Array
FG900	900	31 x 31	1.0	Full Array
FG1156	1156	35 x 35	1.0	Full Array
BG575	575	31 x 31	1.27	Full Array
BG728	728	35 x 35	1.27	Full Array

Note: For a more complete list and detailed package drawing, see the Package Drawings page on xilinx.com.

'Cavity-Down' Metal BGA Packages

What are 'Cavity-Down' BGAs?

Copper-based "cavity-down" BGAs are high-performance, low-profile packages that offer superior electrical and thermal characteristics. This technology is especially applicable for high-speed, high-power semiconductors such as Xilinx's Virtex device family.

Package Construction

Figure 1-2 depicts the cross-section of the "cavity-down" BGA package. It should be noted that this is a solid construction without any internal cavity. The backside die is attached directly to the copper heat spreader and conducts heat out of the package through an epoxy die attach adhesive. The larger the die size and the package body size, the better the thermal performance. The incorporation of the copper heat spreader also results in thermal resistance values that are lowest among the packages offered by Xilinx.

Attached to the heatspreader is a copper stiffener with cavity out to accommodate the die. Along with the heatspreader, this stiffener provides the mechanical flexural strength and warpage control for the package. On the exposed surface of the stiffener is a laminate or build-up structure that contains the circuit traces, the power and ground planes if any, and

the sites for the connecting solder balls. The laminate is made of either a glass reinforced high glass transition Temperature (Tg) Bismaleimide Triazine (BT) or Build up structure. Up to four layers may be used to implement a design that may contain power and ground planes.

This package has two different ball pitches (1.27 mm and 1.00 mm). The 1.00 mm pitch packages are part of the Fine Pitch BGA family. All cavity-down BGA packages are qualified for Jedec Level-3 moisture level.

Key Attributes of Xilinx 'Cavity-Down' BGA

- Lowest Thermal Resistance (theta ja < 15°C / W)
- Superior Electrical Performance
- Low Profile and Light Weight Construction
- Pincount offered by Xilinx: 352 - 860, Package size: 35 mm to 42.5 mm
- Excellent board level reliability

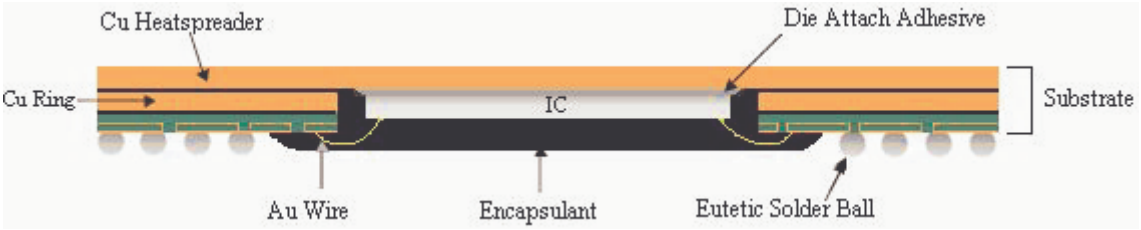


Figure 1-2: **'Cavity-Down' BGA Packages**

Table 1-2: **Xilinx 'Cavity-Down' BGA Offerings**

Package Code	Ball Count	Body Size (mm x mm)	Ball Pitch (mm)	Ball Pattern
BG352	352	35 x 35	1.27	4 perimeter rows
BG432	432	40 x 40	1.27	4 perimeter rows
BG560	560	42.5 x 42.5	1.27	5 perimeter rows
FG680	680	40 x 40	1.00	5 perimeter rows
FG860	860	42.5 x 42.5	1.00	6 perimeter rows

Note: For a more complete list and detailed package drawing, see the Package Drawings page on xilinx.com.

Flip Chip BGA Packages

Flip chip is a packaging interconnect technology that replaces peripheral bond pads of traditional wirebond interconnect technology with area array interconnect technology at the die / substrate interface. The bond pads are either redistributed on the surface of the die or in some very limited cases, they are directly dropped from the core of the die to the surface. Because of this inherent distribution of bond pads on the surface of the device, more bond pads and I / Os can be packed into the device.

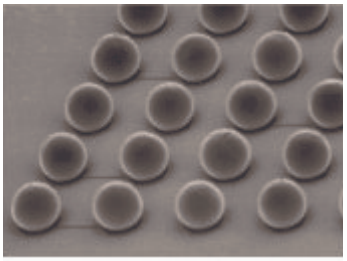


Figure 1-3: **Eutectic Bumps**

Unlike traditional packaging technology in which the interconnection between the die and the substrate is made possible using wire, flip chip utilizes conductive bumps that are placed directly on the area array pads of the die surface. The area array pads contain wettable metallization for solders (either eutectic or high lead) where a controlled amount of solder is deposited either by plating or screen-printing. These parts are then reflowed to yield bumped dies with relatively uniform solder bumps over the surface of the device. The device is then flipped over and reflowed on a ceramic or organic laminate substrate. The solder material at molten stage is self-aligning and produces good joints even if the chips are placed offset to the substrates. After the die is soldered to the substrate, the gap (standoff) formed between the chip and the substrate is filled with an organic compound called underfill. The underfill is a type of epoxy that helps distribute stresses from these solder joints to the surface of the whole die and hence improve the reliability and fatigue performance of these solder joints.

This interconnect technology has emerged in applications related to high performance communications, networking and computer applications as well as in consumer applications where miniaturization, high I/O count, and good thermal performance are key attributes.

Cross-Section/Package Construction

Flip Chip BGA Packages for high performance applications are built on high-density multi-layers organic laminate substrates. Since the flip chip bump pads are in area array configuration, it requires very fine lines and geometry on the substrates to be able to successfully route the signals from the die to the periphery of the substrates. Multilayer build up structures offers this layout flexibility on flip chip packages. The cross section of a Xilinx flip chip package with all essential elements is shown in Figure 1-4.

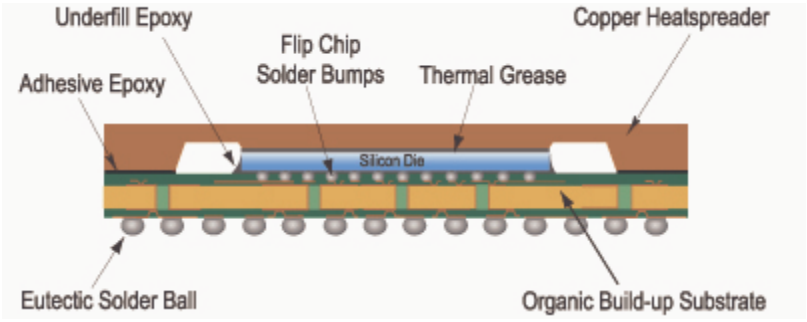


Figure 1-4: **Flip Chip Package**

Certain packages have a different lid design, as shown in Figure 1-5.

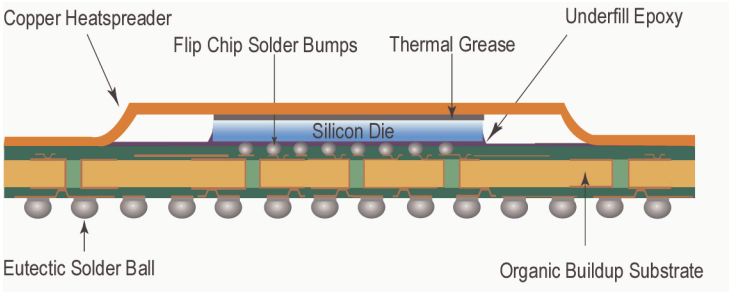


Figure 1-5: **Flip Chip BGA Package With Type II Lid Design**

Reliability

Temperature Cycles (-40 to 125°C) >=1000 Cycles

THB 85°C / 85 RH, Biased, 1000 hrs

Unbiased 85 / 85 85°C / 85 RH, 1000 hrs

Moisture Sensitivity JEDEC Level 4

Benefits

If well implemented, Flip Chip Interconnect Technology offers the following benefits:

- Easy access to core power / ground, resulting in better electrical performance
- Excellent Thermal Performance (Direct heatsinking to backside of the die)
- Higher I / O density since bond pads are in area array format
- Higher frequency switching with better noise control

Table 1-3: **Xilinx Package Offering**

Package Code	Ball Count	Body Size (mm)	Ball Pitch (mm)	Ball Pattern
BF957	957	40 x 40	1.27	Full Array
FF896	896	31 x 31	1.0	Full Array
FF672(1) / 668(1)	672 / 668	27 x 27	1.0	Full Array
FF1152 / 1148(1)	1152 / 1148	35 x 35	1.0	Full Array
FF1517 / 1513	1517 / 1513	40 x 40	1.0	Full Array
FF1696 / 1704	1696 / 1704	42.5 x 42.5	1.0	Full Array

Notes:

1. Figure 1-5
2. For a more complete list and detailed package drawing, see the Package Drawings page on xilinx.com.

Chip Scale Packages

Chip Scale Packages have emerged as a dominant packaging option for meeting the demands of miniaturization while offering improved performance. Applications for Chip Scale Packages are targeted to portable and consumer products where real estate is of utmost importance, miniaturization is key, and power consumption / dissipation must be low. A Chip Scale Package is defined as a package that fits the definition of being between 1 to 1.2 times the area of the die that the package contains while having a pitch of less than 1 mm.

CSP packages bring you the benefits of:

- An extremely small form factor which significantly reduces board real estate for such applications as PCMCIA cards, portable and wireless designs, and PC add-in cards
- Lower inductance and lower capacitance
- The absence of thin, fragile leads found on other packages
- A very thin, light weight package
- Leveraging existing assembly and board level infrastructure

Package Construction

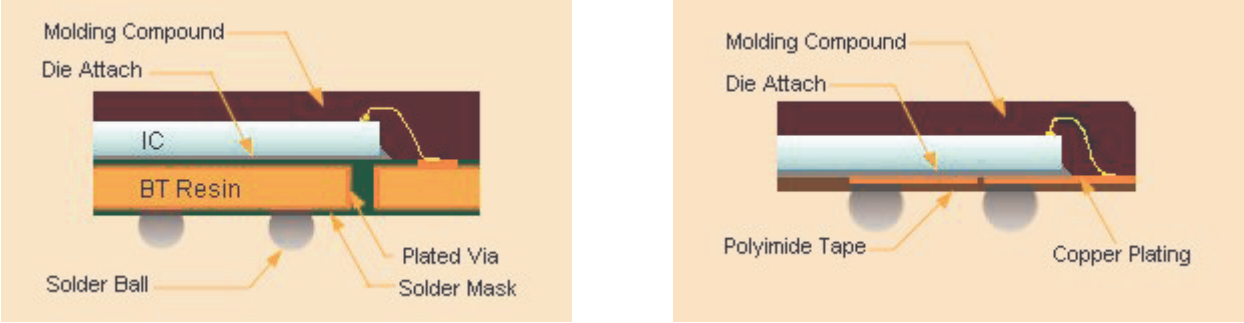


Figure 1-6: **Rigid BT-based Substrate Chip Scale Packages, left; Flex-Based Tape Substrate, right**

Xilinx Chip Scale Packages

Although there are currently more than 50 different types of CSPs available in the market, Xilinx's CSP packages fall into two categories: (1) Flex-based substrates shown in Figure 1 and (2) Rigid BT-based substrates. Although, both types of meet the reliability requirement at the component and board level, BT-based substrate was chosen for the newer devices because of the large vendor base producing / supporting the BT-based substrates.

By employing Xilinx's CSP packages, system designers can dramatically reduce board real estate and increase the I / O counts.

Table 1-4: **Xilinx CSP Offerings**

Package Code	Ball Count	Body Size (mm)	Ball Pitch (mm)	Substrate Type	Ball Pattern
CS48	48	7 x 7	0.80	2 Metal BT	7 x 7 matrix
CS144	144	12 x 12	0.80	Single metal layer tape	4 perimeter rows
CS280	280	16 x 16	0.80	Single metal layer tape	5 perimeter rows
CP56	56	6 x 6	0.50	2 Metal BT	2 perimeter rows
CP132	132	8 x 8	0.50	Single metal layer tape	3 perimeter rows

Notes: For a more complete list and detailed package drawing, see the Package Drawings page on xilinx.com.

Thermally Enhanced Leadframe Packaging

The Package Offering

Table 1-5: **Package Offering**

Xilinx Code	Body (mm)	THK (mm)	Mass (g)	Heatsink Location	JEDEC No.	Xilinx No.
HQ160	28 X 28	3.40	10.8	Down	MO-108-DDI	OPQ0021
HQ208	28 X 28	3.40	10.0	Down	MO_143-FA	OPQ0020
HQ240	32 X 32	3.40	15.0	Down	MO-143-GA	OPQ0019
HQ304	40 X 40	3.80	26.2	Top	MO-143-JA	OPQ0014

Overview

Xilinx offers thermally enhanced quad flat pack packages on XC4000 Series devices and some earlier Virtex devices. This section discusses the performance and usage of these packages (designated HQ). In summary:

- The HQ-series and the regular PQ packages conform to the same JEDEC drawings.
- The HQ and PQ packages use the same PCB land patterns.
- The HQ packages have more mass
- Thermal performance is better for the HQ packages

Applications of HQ Packages

- HQ packages are offered as the thermally enhanced equivalents of PQ packages. They are used for high gate count or high I/O count devices in packages, where heat dissipation without the enhancement may be a handicap for device performance. Such devices include XC4013E, XC4020E, XC4025E, and XC5215.

- The HQ series at the 240-pin count level or below are offered with the heatsink at the bottom of the package. This was done to ensure pin to pin compatibility with the existing PQ packages.

  At the 304-pin count level, the HQ is offered with the heatsink up. This arrangement offers a better potential for further thermal enhancement by the designer.

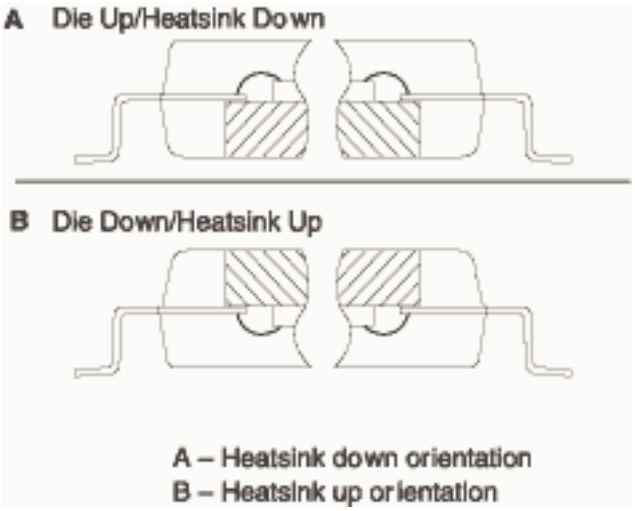


Figure 1-7: **Heatsink Orientation**

- In the die-up / heatsink-down configuration, the heatsink surface is insulated.

Mass Comparison

Because of the copper heatsink, the HQ series of packages are about twice as heavy as the equivalent PQ. Table 1-6 offers a quick comparison.

Table 1-6: **Weight Comparisons for Copper Heatsinks**

	HQ (g)	PQ (g)
160-pin	10.8	5.8
208-pin	10.8	5.3
240-pin	15.0	7.1
304-pin	26.2	N / A

Thermal Data for the HQ

The data for individual devices may be obtained from Xilinx.

Table 1-7: **Still Air Data Comparison**

	HQ $Theta_{JA}$ (°C/Watt)	PQ $Theta_{JA}$ (°C/Watt)
160-pin	13.5 - 14.5	20.5 - 38.5
208-pin	14 – 15	26 - 35
240-pin	12 – 13	19 - 28
304-pin	10 – 11	N / A

Note:

$Theta_{JC}$ is typically between 1 and 2°C / Watt for HQ and MQ Packages. For PQ's, it is between 2 and 7°C / Watt.

Table 1-8: **Data Comparison at Airflow - 250 LFM**

	HQ $Theta_{JA}$ (°C/Watt)	PQ $Theta_{JA}$ (°C/Watt)
160-pin	9 – 10	15 - 28.5
208-pin	9 – 10	14 - 26
240-pin	8 – 9	11 - 21
304-pin	6.5 – 8	N / A

Other Information

- Leadframe: Copper EFTEC-64 or C7025
- Heat Slug: Copper - Nickel plated = Heatsink metal is Grounded
- Lead Finish 85 / 15 Sn / Pb 300 microinches minimum
- D / A material: Same as PQ
- Mold Cpd: Same as PQ
- Packed in the same JEDEC trays

Recommended PCB Design Rules

Recommended PCB Design Rules for Leadframe Packages

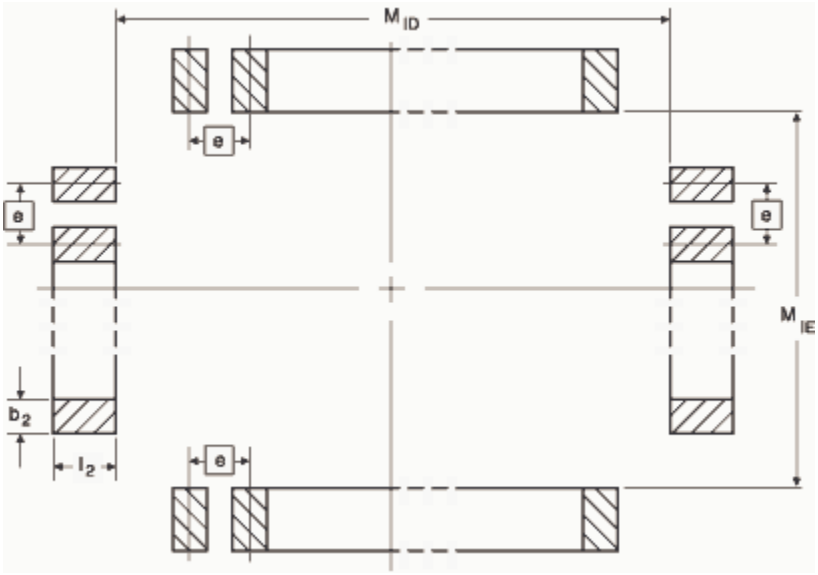


Figure 1-8: **EIA Standard Board Layout of Soldered Pads for QFP Devices**

Table 1-9: **Dimensions for Xilinx Quad Flat Packs(1)**

Dim.	VQ44	VQ64	PQ100	HQ160 PQ160	HQ208 PQ208	VQ100 TQ100	TQ144	TQ176	HQ240 PQ240	HQ304
MID	9.80	9.80	20.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
MIE	9.80	9.80	14.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
E	0.80	0.50	0.65	0.65	0.50	0.50	0.50	0.50	0.50	0.50
B2	0.4-0.6	0.3-0.4	0.3-0.5	0.3-0.5	0.3-0.4	0.3-0.4	0.3-0.4	0.3-0.4	0.3-0.4	0.3-0.4
I2	1.60	1.60	1.80(2)	1.80	1.60	1.60	1.60	1.60	1.60	1.60

Notes:

1. Dimensions in millimeters.
2. For 3.2 mm footprint per MS022, JEDEC Publication 95.

Recommended PCB Design Rules for BGA, CSP Packages

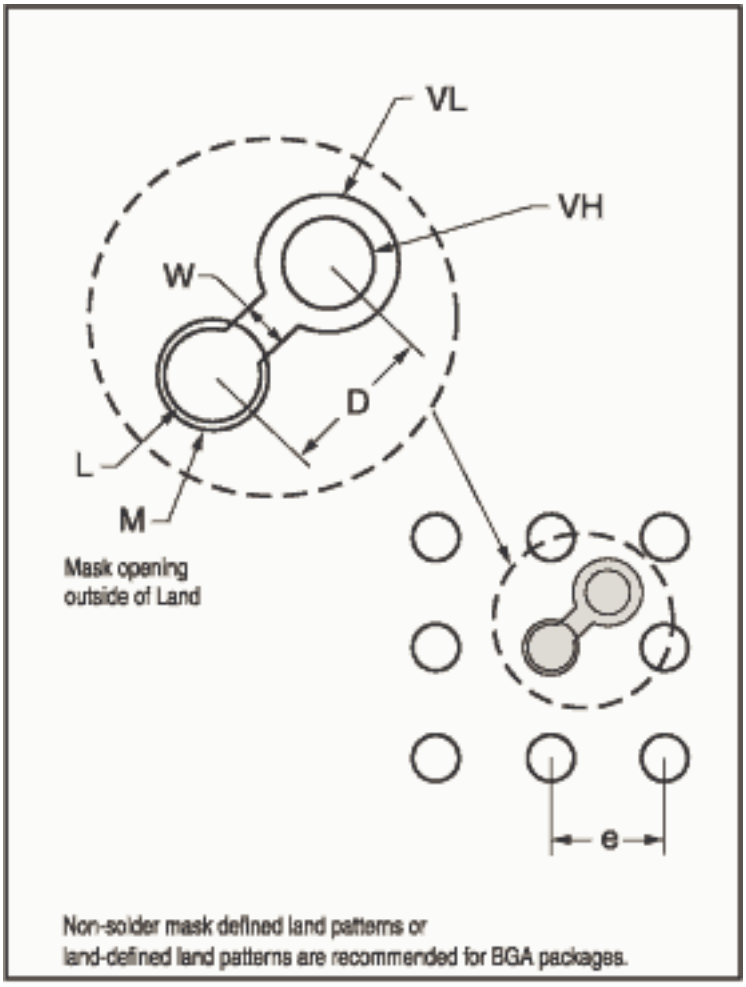


Figure 1-9: **Suggested Board Layout of Soldered Pads for BGA Packages(1)**

Table 1-10: **Recommended PCB Design Rules (Dimensions in mm), Section 1**

	FG256 / FT256	FG324 / FT456	FG676	FG680	FG860	FG900	FG1156	FF896	FF1152	FF1517
Component land Pad Diameter (SMD)(2)	0.45 / 0.40	0.45	0.45	0.50	0.50	0.45	0.45	0.48	0.48	0.48
Solder Land (L) Diameter	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.45	0.45	0.45
Opening in Solder Mask (M) Diameter	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.55	0.55	0.55
Solder (Ball) Land Pitch (e)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Line Width Between Via and Land (w)	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13
Distance Between Via and Land (D)	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70
Via Land (VL) Diameter	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61
Through Hole (VH) Diameter	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300
Pad Array	Full	Full	Full	Full	Full	Full	Full	Full	Full	Full
Matrix or External Row	16 x 16	22 x 22	26 x 26	39 x 39	42 x 42	30 x 30	34 x 34	30 x 30	34 x 34	39 x 39
Periphery Rows	-	7(3)	-	5	6	-	-	-	-	-

Table 1-11: **Recommended PCB Design Rules (Dimensions in mm), Section 2**

	BG225	BG256	BG352	BG432	BG560	BG575	BG728	BF957	CS144	CP56
Component land Pad Diameter(2) (SMD)	0.63	0.63	0.63	0.63	0.63	0.61	0.61	0.61	0.35	0.30
Solder Land (L) Diameter	0.58	0.58	0.58	0.58	0.58	0.56	0.56	0.56	0.33	0.27
Opening in Solder Mask (M) Diameter	0.68	0.68	0.68	0.68	0.68	0.66	0.66	0.66	0.44	0.35
Solder (Ball) Land Pitch (e)	1.50	1.27	1.27	1.27	1.27	1.27	1.27	1.27	0.80	0.50
Line Width Between Via and Land (w)	0.300	0.203	0.203	0.203	0.203	0.203	0.203	0.203	0.13	0.13
Distance Between Via and Land (D)	1.06	0.90	0.90	0.90	0.90	0.90	0.90	0.90	0.56	-
Via Land (VL) Diameter	0.65	0.65	0.65	0.65	0.65	0.65	0.65	0.65	0.51	0.51
Through Hole (VH) Diameter	0.356	0.356	0.356	0.356	0.356	0.356	0.356	0.356	0.250	0.250
Pad Array	Full	-	-	-	-	Full	Full	Full	-	-
Matrix or External Row	15 x 15	20 x 20	26 x 26	31 x 31	33 x 33	24 x 24	27 x 27	31 x 31	13 x 13	10 x 10
Periphery Rows	-	4	4	4	5	-	-	-	4	1

Notes:

1. 3x3 matrix for illustration only, one land pad shown with via connection.
2. Component land pad diameter refers to the pad opening on the component side (solder mask defined).
3. FG456 package has solder balls in the center in addition to periphery rows of balls.

Component Mass Table

Table 1-12 lists Component Mass (Weight) by Package Type

Table 1-12: **Component Mass (Weight) by Package Type**

Package	Description	JEDEC Outline#	Xilinx #	Mass (g)
BF957	957 Ball-Flip Chip BGA 40x40 Body (1.27mm Pitch)	MS-034-BAU-1 (Depopulated)	OBG0036	18.49
BG225	Molded BGA 27mm Full Matrix	MO-151-CAL	OBG0001	2.2
BG256	Molded BGA 27mm SQ	MO-151-CAL	OBG0011	2.2
BG352	SuperBGA - 35 x 35mm Peripheral	MO-151-BAR	OBG0008	7.1
BG432	SuperBGA - 40 x 405mm Peripheral	MO-151-BAU	OBG0009	9.1
BG492	Molded BGA - 35mm - 1.27mm Pitch	MO-151-BAR	OBG0026	5.0
BG560	SuperBGA - 42.5 x 42.5mm SQ	MO-151-BAV	OBG0010	11.5
BG575	575 BGA 31 x 31mm Body (1.27mm Pitch)	MS-034-BAN-1 (Depopulated)	0BG0039	4.58
BG728	728 BGA 35 X 35mm BodyY (1.27mm Pitch)	MS-034-BAR-1	OBG0030	6.2
CB100	NCTB Top Braze 3K / 4K VER	MO-113-AD(3)	OCQ0008 / OCQ0006	10.8
CB164	NCTB Top Braze 3K / 4K VER	MO-113-AA-AD(3)	OCQ0003 / OCQ0007	11.5
CB196	NCTB Top Braze 4K VER	MO-113-AB-AD(3)	OCQ0005	15.3
CB228	NCTB Top Braze 4K VER	MO-113-AD(3)	OCQ0012	17.6
CP56	CSP 56 BGA - 6mm (0.5 pitch)	N / A	OBG0029	0.0
CS48	CSP 48 BGA - 7mm (0.8 pitch)	MO-195	OBG0012	0.2
CS144	CSP 144 BGA - 12mm (0.8 pitch)	MO-205-BE	OBG0015	0.3
CS280	CSP 280 BGA - 16mm (0.8 pitch)	MO-205-AH	OBG0024	0.0
DD8	300 Cerdip Package	MO-03-AA	OPD0005	1.1
FF896	896 BallL - Flip Chip BGA 31 X 31mm Body (1.0mm Pitch)	MS-034-AAN-1	OBG0032	10.7
FF1152	1152 BallL - Flip Chip BGA 35 X 35mm Body (1.0mm Pitch)	MS-034-AAR-1 (depopulated)	OBG0033	14.24
FF1517	1517 BallL - Flip Chip BGA 40 X 40mm Body (1.0mm Pitch)	MS-034-AAU-1 (depopulated)	OBG0034	18.53
FG256	Fine Pitch BGA 17 x 17 mm, 1.0 mm ball pitch	MO-151-AAF-1	OBG0021	0.8
FG324	Molded BGA 23 mm - 1.0 mm Pitch	MO-151-AAJ	OBG0013	2.2

Table 1-12: **Component Mass (Weight) by Package Type *(Continued)***

Package	Description	JEDEC Outline#	Xilinx #	Mass (g)
FG456	Fine Pitch BGA 23 x 23 mm, 1.0 mm ball pitch	MO-151-AAJ-1	OBG0019	2.1
FG556	Fine Pitch BGA 31 x 31 mm, 1.0 mm ball pitch	MO-151-AAN-1	OBG0020	3.92
FG676	Fine Pitch BGA 27 x 27 mm, 1.0 mm ball pitch	MO-151-AAL-1	OBG0018	3.3
FG680	Fine Pitch BGA 40 x 70 mm, 1.0 mm ball pitch	MO-151-AAU-1	OBG0022	10.3
FG860	Fine Pitch BGA 42.5 x 42.57 mm, 1.0 mm ball pitch	MS-034-AAV	OBG0025	13.8
FG900	Fine Pitch BGA 31 x 31 mm, 1.0 mm ball pitch	MO-151-AAN-1	OBG0027	4.0
FG1156	Fine Pitch BGA 35 x 35 mm, 1.0 mm ball pitch	MO-151-AAR-1	OBG0028	5.5
FT256	256 Thin PBGA 17 X 17mm Body (1.0mm Pitch)	MO-151	OBG0040	0.9
HQ160	Metric 28 x 28 - 0.65mm 1.6H / S Die Up	MO-108-DDI	OPQ0021	10.8
HQ208	Metric 28 x 28 - H / S Die Up	MO-143-FA1	OPQ0020	10.8
HQ240	Metric QFP 32 x 32 H / S Die Up	MO-143-GA	OPQ0019	15.0
HQ304	Metric QFP 40 x 40 - H / S Die Down	MO-143-JA	OPQ0014	26.2
MQ208	28 x 28 metal Quad EIAJ Outline	N / A	OPQ0006	6.1
MQ240	32 x 32 metal Quad EIAJ Outline	N / A	OPQ0011	8.0
PC20	PLCC Jedec MO-047	MO-047-AA	OPC0006	0.8
PC28	PLCC Jedec MO-047	MO-047-AB	OPC0001	1.1
PC44	PLCC Jedec MO-047	MO-047-AC	OPC0005	1.2
PC68	PLCC Jedec MO-047	MO-047-AE	OPC0001	4.8
PC84	PLCC Jedec MO-047	MO-047-AF	OPC0001	6.8
PD8	DIP .300 Standard	MO-001-AA	OPD0002	0.5
PD48	DIP .600 Standard	N / A	OPD0001	7.9
PG68	Ceramic PGA "Cavity Up" 11 x 11	MO-067-AC	OPG0002	7.0
PG84	Ceramic PGA "Cavity Up" 11 x 11	MO-067-AC	OPG0003	7.2
PG84	Windowed CPGA "Cavity Up" 11 x 11	MO-067-AC	OPG0013	7.5
PG120	Ceramic PGA 13 x 13 Matrix	MO-067-AE	OPG0012	11.5
PG132	Ceramic PGA 14 x 14 Matrix	MO-067-AF	OPG0004	11.8
PG156	Ceramic PGA 16 x 16 Matrix	MO-067-AH	OPG0007	17.1

Table 1-12: **Component Mass (Weight) by Package Type *(Continued)***

Package	Description	JEDEC Outline#	Xilinx #	Mass (g)
PG175	Ceramic PGA 16 x 16 Standard Version	MO-067-AH	OPG0009	17.7
PG191	Ceramic PGA 18 x 18 Standard - All	MO-067-AK	OPG0008	21.8
PG223	Ceramic PGA 18 x 18 Type	MO-067-AK	OPG0016	26.0
PG299	Ceramic PGA 20 x 20 Heatsink	MO-067-AK	OPG0022	37.5
PG299	Ceramic PGA 20 x 20 Type	MO-067-AK	OPG0015	29.8
PG411	Ceramic PGA 39 x 39 Stagger	MO-128-AM	OPG0019	36.7
PG475	Ceramic PGA 41 x 41 Stagger	MO-128-AM	OPG0023	39.5
PG559	Ceramic PGA 43 x 43	MO-128	OPG0025	44.5
PP132	Plastic PGA 14 x 14 Matrix	MO-83-AF	OPG0001	8.1
PP175	Plastic PGA 16 x 16 Buried	MO-83-AH	OPG0006	11.1
PQ44	EIAJ 10 x 10 x 2.0 QFP	MS-022-AB	OPQ0015	0.5
PQ100	EIAJ 14 x 20 QFP - 1.60 (default)	MO-108-CG1	OPQ0013	1.6
PQ100	EIAJ 14 x 20 QFP - 1.80 (not used)	EIAJ-Old	OPQ0016	1.6
PQ100	EIAJ 14 x 20 QFP - 1.95 (old version)	MO-108-CC2	OPQ0013	1.6
PQ160	EIAJ 28 x 28 0.65mm 1.60	MO-108-DD1	OPQ0002	5.8
PQ208	EIAJ 28 x 28 0.5mm 1.30	MO-143-FAI	OPQ0003	5.3
PQ240	EIAJ 32 x 32 0.5mm	MO-143-GA	OPQ0010	7.1
PQ304	Metric QFP 40 x 40 - H / S Die Down	MO-143-JA	OPQ0014	26.2
SO8	Version 1 - 0.150 / 50 mil	Mo-150	OPD0006	0.1
SO20	300 mil SOIC	MS-1-3	OPD0009	0.5
SO24	300 mil SOIC	MS-113	OPD0010	0.6
TQ100	Thin QFP 1.4mm thick	MS-026-BDE	OPQ0004	0.7
TQ128	Thin QFP 1.4mm thick - RECT	MS-026-BHB	OPQ0028	0.8
TQ144	Thin QFP 1.4mm thick	MS-026-BFB	OPQ0007	1.4
TQ176	Thin QFP 1.4mm thick	MS-026-BGA	OPQ0008	1.9
VO8	Thin SOIC - II	N / A	OPQ0007	0.1
VQ44	Thin QFP 1.0 thick	MS-026-AED	OPQ0017	0.4
VQ64	THIN QFP 1.0 thick	MS-026-ACD	OPQ0009	0.5
VQ100	Thin QFP 1.0 thick	MS-026-AED	OPQ0012	0.6
WC44	Jedec Windowed Cerquad	MO-087	QCQ0004	2.9
WC84	Windowed Cerquad	MO-087	QCQ0010	11

Chapter 2

Thermal Management & Thermal Characterization Methods & Conditions

Introduction

This document addresses the need to manage the heat generated in CMOS logic devices, an industrywide pursuit, and describes the measures Xilinx uses and recommends to its customers to quantify and manage potential thermal problems in FPGAs.

Thermal Management

Modern high-speed logic devices consume an appreciable amount of electrical energy. This energy invariably turns into heat. Higher device integration drives technologies to produce smaller device geometry and interconnections. With chip sizes getting smaller and circuit densities at their highest levels, the amount of heat generated on these fast-switching CMOS circuits can be very significant. As an example, Xilinx Virtex-II Pro FPGA devices incorporate multiple processors, multiple-gigabit transceivers, digital-controlled impedance I/Os, and I/Os capable of supporting various high current standards. Special attention must be paid to addressing the heat removal needs for these devices.

The need to manage the heat generated in a modern CMOS logic device is not unique to Xilinx. This is a general industry pursuit. However, unlike the power needs of a typical industry application-specific integrated circuit (ASIC) gate array, the field-programmable device's power requirement is not determined in the factory. Customers' designs can vary in power as well as physical needs. This is the challenge in predicting FPGA thermal management needs.

There is no sure way of anticipating accurate power dissipation of an FPGA device short of actual measurement. Xilinx has developed several software-based power-estimator tools to help the end user predict power consumption. The tools can be useful as a first step. Like most tools, however, the predicted output depends on the work put into the predicting effort. In assigning packages to devices, effort has been made to tailor the packages to the power needs of typical users. For each device, suitable packages are typically chosen to handle "typical" designs and gate utilization for the device. For the most part, the choice of a package as the primary or internal heat removal casing works well without any external heat management. Increasingly, with highly integrated devices, the need arises for customers to utilize an FPGA device beyond "typical" design parameters. For these situations, the use of the primary package without external enhancement may not be adequate to address the heat removal needs of the device. It is for these cases that the need to manage the heat removal through external means becomes essential.

Heat has to be removed from a device to ensure that the device is maintained within its functional and maximum design temperature limits. If heat buildup becomes excessive,

the device's temperature may exceed the temperature limits. A consequence of this is that the device may fail to meet speed-files performance specifications. In addition to performance considerations, there is also the need to satisfy system reliability objectives by operating at a lower temperature. Failure mechanisms and failure rate of devices have an exponential dependence on devices' operating temperatures. Thus, the control of the package, and by extension device temperature, is essential to ensure product reliability.

Package Thermal Characterization Methods and Conditions

Characterization Methods

Xilinx uses several methods to obtain thermal performance characteristics of integrated circuit packages. The methods include thermal simulation using finite element software tools, and an indirect electrical method utilizing an isolated diode on a special thermal test die or even on a Xilinx FPGA housed in the package of interest. The majority of the data reported by Xilinx is based on the indirect diode method, with a few instances of using simulation tools.

Calibration of Isolated Diode

In the direct electrical method, the forward-voltage drop of an isolated diode residing on a special test die or the temperature diode of the Xilinx FGPA is calibrated by applying a constant forcing current (from 0.100 mA to 0.500 mA) over a temperature range of 0 - 125 °C (degrees Celsius). The calibrated packaged device is then mounted on an appropriate board and placed in the testing environment — *e.g.*, still air or forced convection. Power ($\mathbf{P_D}$) is applied to the device through diffused resistors on the same thermal die. In the FPGA case, a known self-heating program is loaded and clocked to generate the monitored power. Usually, between 0.5 Watts to 4 Watts may be applied. Higher power (up to 10 watts) is possible, depending on the package. The resulting rise in junction temperature is monitored with the forward-voltage drop of the precalibrated diode.

Measurement Standards

Previously, Xilinx Thermal lab used the SEMI thermal test methods (#G38-87) and associated SEMI-based boards (#G42-87) to do thermal characterization. Most of our recent measurements and simulations are based on provision of the JEDEC and EIA Standard — JESD51-n series specifications. It is our assessment that the latter standard offers some options that are not available in the SEMI method. We will continue to quote the SEMI-based data (designated by SEMI in the comment column) for older packages measured in the earlier era, and when we quote new data, they will be designated as JESD in the comment section.

It is also essential to note that these standard-based measurements give characterization results that allow packages and conditions to be compared. Like miles per gallon (MPG) figures quoted on new cars, the numbers should be used with caution. As specific user environments will not be identical to the conditions used in the characterization, the numbers quoted may not precisely predict the performance of the package in an application-specific environment.

Definition of Terms

$\mathbf{T_J}$ Junction Temperature, defined as the maximum temperature on the die, expressed in °C (degrees Celsius).

T_A Ambient Temperature, defined as the temperature of the surrounding environment, expressed in °C (degrees Celsius).

T_C Temperature of the package taken at a defined location on the body. In most situations, it is taken at the primary heat flow path on the package and will represent the hottest part on the package, expressed in °C. See the next item for when **T_C** is taken at the top.

T_t Temperature of the package body taken at the top location on the package. This is a special case of **T_C**.

T_B This is the board Temperature taken at a predefined location on the board near the component under test, expressed in °C.

T_I This is the isothermal fluid temperature when junction to case temperature is taken, expressed in °C.

P_D The total device power dissipation, expressed in Watts.

Junction-to-Reference General Setup

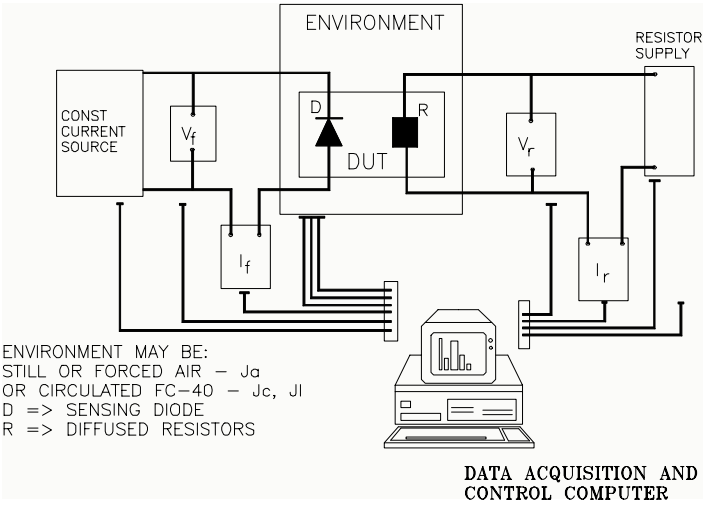


Figure 2-1: **Thermal Measurement Setup (Schematic for Junction to Reference)**

Junction-to-Case Measurement — θ_{JC}

Theta-jc (θ_{JC}) measures the heat flow resistance between the die surface and the surface of the package (case). This data is relevant for packages used with external heatsinks. It assumes that heat is flowing through the top to the exclusion of the others. In the ideal case, all the heat is forced to escape the package at the path where **T_C** is taken. The lateral heat flow is not allowed or minimized so that the source of temperature differential will be attributable to the total known heat input.

Figure 2-2: **Theta JC Measurement Setup**

A copper heatsink plate at the top of the package is used in θ_{JC} methods to achieve the forced preferred directional flow.

Prior to 1999, the junction-to-case characterization on some heatsink packages was accomplished in a 3M Flourinert (FC-40) isothermal circulating fluid stabilized at 25°C. Current Xilinx data on θ_{JC} is simulated using the cold plate approach.

With applied power ($\mathbf{P_D}$) and under stabilized conditions, case temperature ($\mathbf{T_C}$) is measured with a low gauge thermocouple (36-40 AWG) at the primary heat-flow path of the particular package. Junction temperature ($\mathbf{T_J}$) is calculated from the diode forward-voltage drop from the initial stable condition before power is applied, *i.e.*,

$$\theta_{JC} = (T_J - T_C) / P_D$$

where the terms are as defined above. A poorly defined θ_{JC} condition usually leads to lower numbers being reported. In such cases, the recorded temperature difference (Tj-Tc) is the result of having a fraction of the power going through the path. However, in the calculation, the full power is used.

Junction-to-Top Measurement — Ψ_{JT}

Psi-jt (Ψ_{JT}) is a junction to the top thermal parameter (*not thermal resistance*), defined in the JEDEC specification that shadows θ_{JC} in a real-world situation. This parameter provides correlation between chip junction temperature and the temperature of the package at the top. It is measured on a defined FR4-based PC board as described under θ_{JA}**.** The reference temperature is the temperature monitored at the top of the component, $\mathbf{T_t}$. Though the cause of the temperature rise may not be caused by all the power applied, the full power is used in the calculation, *i.e.*,

$$\Psi_{JT} = (T_J - T_t) / P_D$$

where $\mathbf{P_D}$ is the full applied power.

The parameter value depends on airflow conditions. In heatsink type packages (some BGs and most FF packages) where the primary heat flow is almost one dimensional and the heat flux is confined to the top, $\mathbf{T_C}$ and $\mathbf{T_t}$ are taken at the same point and Ψ_{JT} approaches θ_{JC}.

In molded packages like Xilinx FG676, FG900 and FG1156, the one-dimensional condition is difficult to meet. At best, a fraction of the heat flux (~40 – 60%) goes to the top in the standardized setup. In an end-user application, the heat flux division may follow a similar pattern. Under such cases, psi-jt (Ψ_{JT}) and theta-jc (θ_{JC}) tend to diverge from each other. If the total power is known, and the top temperature can be carefully measured, Ψ_{JT} is used to predict the T_J in application environment.

In some plastic molded packages, we may be able to apply Ψ_{JT} numbers relevant to our setup.

Junction-to-Ambient Measurement — θ_{JA}

Figure 2-3: **Theta JA Measurement Setup**

SEMI method: Some of the data reported are based on the SEMI standard methods and associated board standards. θ_{JA} data reported as based on SEMI were measured on FR4-based PC boards measuring 4.5” x 6.0 x .0625” (114.3mm x 152.4mm x 1.6mm) with edge connectors. Several versions are available to handle various surface mount (SMT) devices. They are, however, grouped into two main types. Type I board (the equivalent of the JEDEC low-conductivity board) is single layer with two signal planes (one on each surface) and no internal Power / GND planes. This is the 2L / 0P or 2S / 0P board and the trace density on this board is less than 10% per side. The type II board (the equivalent of the JEDEC 2S / 2P board) has two internal copper planes — one power and one ground. These planes are in addition to the two signal trace layers on both surfaces. This is the 4L / 2P (four-layer, also referred to as 2S / 2P) board.

JEDEC measurements: Packages are measured in a one foot-cube enclosure based on JEDS51-2. Test boards are fashioned per test board specification JESD51-3 and JESD51-7. The board sizes depend on the package and are typically 76.2mm x 114.3mm x 1.6mm or 101.6mm x 114.3mm x 1.6mm. These come in low-conductivity as well as high-conductivity versions.

Thermal resistance data may be taken with the package mounted in a socket or with the package mounted directly on traces on the board. Socket measurements typically use the 2S / 0P or low-conductivity boards. SMT devices, on the other hand, may use either board. Published data always reflect the board and mount conditions used (ref 2S / 0P or 4L / 2P).

The board with the device under test (DUT) is mounted in the test enclosure and data is taken at the prevailing temperature and pressure conditions — between 20°C and 30°C ambient (T_A). Appropriate power is used, depending on the anticipated thermal resistance of the package. Applied power, signal monitoring — including the enclosure (ambient) temperatures are noted. The junction to ambient thermal resistance is calculated as follows:

$$\theta_{JA} = (T_J - T_A) / P_D$$

In the case of airflow measurement, this is done in a special airflow enclosure section of a suction-type low-velocity wind tunnel. Airflow velocities from 0-1000 Linear Feet per Minute (LFM), *i.e.*, 0-5.08 m/s, are used with very low turbulence. The controlling specification is JESD51-6. Airflow measurements use similar boards as θ**ja** with air conditions noted with hot wire anemometer.

Thermal Resistance: Junction-to-Board — θ_{JB}

This is defined as:

$$\theta_{JB} = (T_J - T_B) / P_D$$

where T_B is the board temperature at steady state measured at specified location on the board. P_D is the actual power in Watts that produces the change in temperature.

T_B is monitored on a board with a 40-gauge thermocouple at specific location in the proximity of the package leads or balls. As an example, for BGA package, the thermocouple is attached to a trace midway along the side of the package with the attachment point within 1mm of the package body.

Like **Theta-jc, Theta-jb** depends on constrained flow in a preferred direction. In actual measurement or simulations the heat flow is forced to go preferably through the board by excluding other paths with insulation. The measurement conditions are not likely to be reproduced in a real application.

Junction-to-Board Measurement — Ψ_{JB}

Junction-to-board thermal parameter — Ψ_{JB} is a thermal parameter (*not thermal resistance*) defined by JEDEC specification that approximates θ_{JB} in a real-world situation. This parameter provides correlation between chip junction temperature and the temperature of the board. It is measured on a high effective thermal conductivity board as described under θ_{JA}. The reference temperature is the temperature monitored on the board, T_B. Though the temperature rise may not be caused entirely by all the power applied, the full power is used in the calculation, *i.e.*,

$$\Psi_{JB} = (T_J - T_B) / P_D$$

where P_D is the full applied power. This parameter is used to obtain chip temperature (T_J) in applications where the board temperature can be monitored as described.

Though currently Xilinx does not publish θ_{JB} and Ψ_{JB}, some limited data on Ψ_{JB} exist for some of the high-performance Xilinx packages. These may be requested for the specific device package combination through the Xilinx hotline.

Since the board selection (copper trace density, absence or presence of ground planes, etc.) affects the results of the thermal resistance, the data from these tests should be qualified with the board mounting information as well as the test standard.

Data Acquisition and Package Thermal Database

Data for a package type is gathered for various die sizes, power levels, cooling modes (air flow and sometimes heatsink effects) with a Data Acquisition and Control System (DAS). The system controls and conditions the power supplies and other ancillary equipment for a hands-free data taking. A package is completely characterized with respect to the major variables that influence the thermal resistance. A database is generated for the package. From the database, thermal resistance data is interpolated as typical values for the individual Xilinx devices that are assembled in the characterized package. Table 2-1 shows

the typical values for various packages. It must be noted that specific device data may not be the same as the typical data listed for the package. However, the data will fall within the min. and max. ranges given. The more widely a package is used across FPGA and EPLD families, the wider the range quoted here. If specific device data is required, customers may contact the Xilinx hotline for a detailed listing applicable to the device.

More detailed data is also available for the newer packages.

Table 2-1: **Summary of Thermal Resistance for Packages**

Pkg-Code	θ_{JA} still air (Max)	θ_{JA} still air (Typ)	θ_{JA} still air (Min)	θ_{JA} 250 LFM (Typ)	θ_{JA} 500 LFM (Typ)	θ_{JA} 750 LFM (Typ)	θ_{JC} (Typ)	Comments
	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	
BF957	11.2	10.9	10.6	6.8	5.4	4.6	0.5	JESD: 4L / 2P-SMT Simulation
BG225	37.2	30.3	23.9	21.9	19.3	18.5	3.6	SEMI: 4L / 2P-SMT
BG256	38.8	27.0	21.2	19.5	17.2	16.5	3.9	SEMI: 4L / 2P-SMT
BG352	13.3	12.6	11.8	8.8	7.2	6.5	1.0	SEMI: 4L / 2P-SMT
BG432	11.8	11.2	10.7	7.9	6.5	5.9	0.9	SEMI: 4L / 2P-SMT
BG492	17.2	17.2	17.2	12.2	11.9	11.9	0.8	SEMI: 4L / 2P-SMT
BG560	11.2	10.6	10.2	7.4	6.1	5.6	0.8	SEMI: 4L / 2P-SMT
BG575	16.9	15.8	14.7	12.1	11.4	11.0	2.8	JESD: 4L / 2P-SMT Simulation
BG728	13.7	13.6	13.2	10.2	9.3	8.7	1.9	JESD: 4L / 2P-SMT Simulation
CB100	48.8	41.9	38.5	25.4	19.7	17.8	5.8	SEMI:Socketed
CB164	29.8	26.7	25.0	16.6	12.4	10.6	3.7	SEMI:Socketed
CB196	26.2	25.0	23.8	15.6	11.6	10.0	2.5	SEMI:Socketed
CB228	21.3	18.5	16.3	11.5	8.6	7.4	1.9	SEMI:Socketed
CC20	105.0	105.0	105.0	72.8	57.7	35.0	7.0	SEMI:Socketed
CC44	48.6	45.8	44.5	37.6	30.8	25.2	8.3	SEMI:Socketed
CD8	121.0	112.9	103.9	80.0	65.7	58.0	7.1	SEMI:Socketed
CD48	40.0	40.0	40.0	-	-	-	5.0	SEMI:Socketed
CG560	14.3	14.3	14.3	9.2	7.2	6.3	1.6	SEMI:Socketed
CP56	65.0	65.0	65.0	-	-	-	15.0	Estimated
CP132	72.4	67.4	62.3	62.8	60.4	58.5	13.4	JESD: 4L / 2P-SMT Simulation
CS48	45.0	45.0	45.0	-	-	-	5.0	Estimated
CS144	65.0	35.7	34.0	25.9	23.9	23.2	2.5	Estimated
CS280	30.5	30.5	30.5	25.0	23.1	22.2	0.8	Estimated
DD8	115.9	109.3	94.0	89.8	73.5	60.2	8.3	Socketed
FF672	15.7	14.6	13.8	10.5	8.5	7.5	0.7	JESD: 4L / 2P-SMT Simulation
FF896	11.8	11.8	11.8	8.2	6.7	5.9	0.5	JESD: 4L / 2P-SMT Simulation

Table 2-1: **Summary of Thermal Resistance for Packages *(Continued)***

Pkg-Code	θ_{JA} still air (Max)	θ_{JA} still air (Typ)	θ_{JA} still air (Min)	θ_{JA} 250 LFM (Typ)	θ_{JA} 500 LFM (Typ)	θ_{JA} 750 LFM (Typ)	θ_{JC} (Typ)	Comments
	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	
FF1148	11.0	10.95	10.9	6.7	5.2	4.5	0.6	JESD: 4L / 2P-SMT Simulation
FF1152	11.9	11.7	11.4	7.6	6.1	5.2	0.5	JESD: 4L / 2P-SMT Simulation
FF1517	10.5	10.5	10.5	6.5	5.1	4.4	0.5	JESD: 4L / 2P-SMT Simulation
FF1704	9.0	8.8	8.6	5.5	4.3	3.7	0.4	JESD: 4L / 2P-SMT Simulation
FG256	33.6	25.1	18.4	21.2	19.7	19.1	3.9	SEMI: 4L / 2P-SMT
FG324	29.4	26.0	21.1	19.3	17.2	16.5	3.4	SEMI: 4L / 2P-SMT
FG456	23.5	19.6	16.5	15.5	14.1	13.6	2.2	SEMI: 4L / 2P-SMT
FG556	13.7	13.6	13.5	9.7	9.4	9.4	2.1	SEMI: 4L / 2P-SMT
FG676	16.7	16.6	16.6	13.2	12.0	11.5	2.0	SEMI: 4L / 2P-SMT
FG680	11.1	10.8	10.4	7.5	6.2	5.6	0.9	SEMI: 4L / 2P-SMT
FG860	10.5	10.2	10.0	7.2	5.9	5.4	0.8	SEMI: 4L / 2P-SMT
FG900	14.1	13.7	13.5	9.8	9.5	9.5	2.0	Estimated
FG1156	13.7	13.4	13.2	9.7	9.2	9.0	2.0	JESD: 4L / 2P-SMT Simulation
FT256	34.6	30.9	27.5	26.2	24.4	23.7	4.3	SEMI: 4L / 2P-SMT
HQ160	16.5	15.6	14.7	10.8	8.6	7.7	2.0	SEMI: 4L / 2P-SMT
HQ208	16.7	15.8	14.4	10.9	8.7	7.8	2.1	SEMI: 4L / 2P-SMT
HQ240	14.5	13.2	11.8	9.1	7.3	6.5	1.5	SEMI: 4L / 2P-SMT
HQ304	11.3	10.6	10.0	7.1	5.6	4.9	1.1	SEMI: 4L / 2P-SMT
HT144	19.1	18.5	18.2	12.6	10.7	10.1	2.1	SEMI: 4L / 2P-SMT
HT176	15.6	15.3	15.2	10.4	8.9	8.4	2.0	SEMI: 4L / 2P-SMT
HT208	13.6	13.4	13.3	9.0	7.6	7.2	1.9	SEMI: 4L / 2P-SMT
MQ208	18.4	17.9	17.4	14.0	12.6	11.9	1.3	SEMI: 2L / 0P-SMT
MQ240	16.8	16.7	16.4	12.0	10.8	10.5	1.2	SEMI: 2L / 0P-SMT
PC20	87.3	82.3	72.0	62.1	55.5	51.8	24.2	SEMI: 2L / 0P-SMT
PC28	67.6	66.1	63.0	49.8	44.6	41.6	17.8	SEMI:Socketed
PC44	53.7	46.5	42.3	35.1	31.4	29.3	14.9	SEMI:Socketed
PC68	46.2	41.9	38.4	31.6	28.2	26.4	9.5	SEMI:Socketed
PC84	41.7	33.3	27.9	25.8	20.8	16.8	5.6	SEMI:Socketed
PD8	83.0	78.9	71.3	59.4	53.2	49.6	21.5	SEMI:Socketed
PD48	43.2	43.2	43.2	32.6	29.1	27.2	11.6	SEMI:Socketed
PG68	38.8	37.0	34.1	25.6	19.9	17.3	7.8	SEMI:Socketed
PG84	38.5	34.4	31.3	23.8	18.5	16.1	6.0	SEMI:Socketed
PG120	37.8	27.8	24.6	19.3	15.2	13.3	4.0	SEMI:Socketed

Table 2-1: **Summary of Thermal Resistance for Packages *(Continued)***

Pkg-Code	θ_{JA} still air (Max)	θ_{JA} still air (Typ)	θ_{JA} still air (Min)	θ_{JA} 250 LFM (Typ)	θ_{JA} 500 LFM (Typ)	θ_{JA} 750 LFM (Typ)	θ_{JC} (Typ)	Comments
	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	
PG132	32.0	28.7	23.9	20.3	16.7	14.8	2.9	SEMI:Socketed
PG144	25.8	24.5	23.3	17.4	14.3	12.6	3.7	SEMI:Socketed
PG156	25.6	23.9	20.7	14.9	11.6	10.3	2.7	SEMI:Socketed
PG175	25.2	23.3	19.9	14.5	11.3	10.0	2.6	SEMI:Socketed
PG191	25.7	21.8	18.5	15.5	12.7	11.2	1.5	SEMI:Socketed
PG223	25.3	21.1	17.7	15.0	12.3	10.8	1.5	SEMI:Socketed
PG299	21.0	17.3	15.1	10.4	8.7	8.3	2.0	SEMI:Socketed
PG411	16.1	14.7	14.3	9.5	7.4	6.5	1.4	SEMI:Socketed
PG475	15.1	14.6	14.3	9.4	7.3	6.4	1.4	SEMI:Socketed
PG559	13.7	13.4	13.2	8.6	6.7	5.9	1.3	Estimated
PP132	35.4	34.4	32.8	23.5	17.9	17.1	6.1	SEMI:Socketed
PP175	29.5	28.9	28.0	19.0	15.0	13.0	2.5	SEMI:Socketed
PQ44	52.2	51.3	50.1	39.8	36.4	35.4	12.4	SEMI: 4L / 2P-SMT
PQ100	35.0	33.5	32.0	29.5	27.6	26.6	5.6	SEMI: 4L / 2P-SMT
PQ160	38.1	31.8	20.6	23.5	20.8	19.2	5.0	SEMI: 4L / 2P-SMT
PQ208	36.9	30.4	18.9	22.4	19.8	18.4	4.8	SEMI: 4L / 2P-SMT
PQ240	28.5	19.9	14.0	14.7	13.0	12.0	3.8	SEMI: 4L / 2P-SMT
SO8	147.1	147.1	147.1	112.2	104.6	98.6	48.3	IEEE-(Ref)
SO16	106.0	106.0	106.0	-	-	-	47.0	Vendor data
SO20	86.0	86.0	86.0	65.4	61.1	57.6	36.0	Vendor data
SO24	80.0	80.0	80.0	60.8	56.8	53.6	28.0	Vendor data
TQ44	76.5	76.2	75.8	59.2	50.0	45.1	8.2	SEMI: 4L / 2P-SMT
TQ100	39.5	31.8	30.6	25.9	24.0	23.5	7.5	SEMI: 4L / 2P-SMT
TQ128	31.5	30.6	30.0	26.9	25.2	24.3	5.3	SEMI: 4L / 2P-SMT
TQ144	57.6	33.5	29.8	26.1	22.3	20.9	5.5	SEMI: 4L / 2P-SMT
TQ160	28.9	28.9	28.9	21.8	18.5	17.0	5.6	SEMI: 4L / 2P-SMT
TQ176	29.7	28.1	26.7	21.3	18.0	16.5	5.3	SEMI: 4L / 2P-SMT
VO8	160.0	160.0	160.0	137.6	129.6	123.2	60.0	Estimated
VO24	76.0	76.0	76.0	57.8	54.0	50.9	28.0	Estimated
VQ44	46.9	42.2	38.9	35.2	32.8	32.1	8.2	SEMI: 4L / 2P-SMT

Table 2-1: **Summary of Thermal Resistance for Packages *(Continued)***

Pkg-Code	θ_{JA} still air (Max)	θ_{JA} still air (Typ)	θ_{JA} still air (Min)	θ_{JA} 250 LFM (Typ)	θ_{JA} 500 LFM (Typ)	θ_{JA} 750 LFM (Typ)	θ_{JC} (Typ)	Comments
	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	
VQ64	46.9	42.3	39.3	35.2	32.9	32.1	8.2	SEMI: 4L / 2P-SMT
VQ100	53.2	38.8	32.4	32.3	30.1	29.3	9.3	SEMI: 4L / 2P-SMT

Notes:

- The maximum, typical and minimum numbers reported here are based on numbers for all the devices for the specific package at the time of compilation. The numbers do not necessarily reflect the absolute limits of that package. Specific device data should lie within the limits. Packages used for a broader spectrum of devices have a wider range in the table. Specific device data in a package may be obtained from the factory.
- Data is listed alphabetically by the Xilinx package code. Package configurations and drawings corresponding to these codes can be found in the section of the databook with package outline drawings.
- In the comment section, 2L / 0P-SMT implies that the data was taken from a surface-mount type I board or low-conductivity type board — no internal planes on the board.
- 4L / 2P-SMT (2S / 2P) implies that the data was taken from a four-layer SMT board incorporating two internal planes. We have included SEMI and JESD to designate what method the data came from.
- Socketed data is also specified where applicable.
- Thermal data is in degrees Celsius / Watt. JA refers to θ_{JA}. Airflow is in linear feet per minute (LFM). 500 LFM = 2.5 meters per second.

Application of Thermal Resistance Data

Thermal resistance data is used to gauge the IC package thermal performance. There are several ways to express the thermal resistance between two points. The following are a few of them:

- θ_{JA} = Junction to ambient thermal resistance (°C / W).
- θ_{JC} = Junction to case thermal resistance (°C / W)
- θ_{JB} = Junction to board thermal resistance (°C / W)
- θ_{CA} = Case to ambient thermal resistance (°C / W)
- θ_{CS} = Case to heatsink thermal resistance (°C / W)
- θ_{SA} = Heatsink to ambient thermal resistance (°C / W)

Other thermal parameters include

- Ψ_{JB} = Junction to board thermal characteristic parameter (°C / W)
- Ψ_{JT} = Junction to package thermal characteristic parameter (°C / W)

θ_{JC} measures the internal package resistance to heat conduction from the die surface, through the die mount material to the package exterior. θ_{JC} strongly depends on the package material's heat conductivity and geometrical considerations.

θ_{JA} measures the total package thermal resistance including θ_{JC}. θ_{JA} depends on the package material properties and such external conditions as convective efficiency and board mount conditions. For example, a package mounted on a socket may have a θ_{JA} value 20% higher than the same package mounted on a four-layer board with power and ground planes.

In general, θ_{MN} expresses the thermal resistance between points **M** and **N**. In the above expression, the "source" and "end" points are indicated.

In situations where a heatsink is used with a heatsink compound, thermal resistance of heatsink is referenced as θ_{SA} (sink-to-ambient) and the attached material as θ_{CS} (case-

to-heatsink). These thermal resistances may be added. For example, $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ is an expression used in heatsink situations with interface material resistance θ_{CS}.

Thermal Data Usage

The following are some data requirements for using thermal resistance in an application.

- Xilinx-supplied data:
  - θ_{JA} — quoted from Xilinx database. Data may obtained by contacting Xilinx hotline.
  - θ_{JC} — quoted from Xilinx database. Data may obtained by contacting Xilinx hotline.
  - θ_{SA} — quoted by heatsink supplier.
- Items that the user may need to supply.
  - $\mathbf{T_J}$-max:
    - This may go as high as the absolute maximum temperature for the package — typically 125°C to 135°C for plastic
    - Beyond 85°C for commercial specified parts, speed files may have to be derated. Contact Xilinx application group for more information. The temperature limit before derating is activated is higher for industrial-grade and military-temperature-grade parts.
    - The user will have to pick a $\mathbf{T_J}$-max for reliability considerations, and plan the thermal budget around that
  - $\mathbf{T_A}$: Ambient in a system
    - This is also another variable that the user can control. Typically, this is set to approximately 45°C to 55°C.
- Items usually calculated:
  - Power dissipation. The thermal equation may be used to determine a power range that can satisfy some given conditions
  - Also, if power is known, $\mathbf{T_J}$-max may be calculated from the equations
  - If the temperature on the top of a bare part is well monitored in a system (not the way θ_{JC} is measured), the thermal parameter Ψ_{JT} can be used to get junction temperature
  - Similarly, a well monitored board temperature can be used to predict junction with the Ψ_{JB} parameter

In nonheatsink situations, the following inequality formula should hold.

$$\mathbf{T_J}(\text{max}) > \theta_{JA} * \mathbf{P_D} + \mathbf{T_A}$$

The two examples below illustrate the use of the above inequality formula. Specific packages have been used in the examples but any package—Quad, BGA, FGs, or even FlipChip-based BGs—will be applicable.

Example 1:

The manufacturer's goal is to achieve Tj (max) < 85°C

A module is designed for a Ta = 45°C max.

An XCV300 in a FG456 has a θ_{JA} = 16.5°C / watt. θ_{JC} = 2.0°C / Watt.

Given a XCV300 with a logic design with a rated power $\mathbf{P_D}$ of 2.0 Watts.

With this information, the maximum die temperature can be calculated as:

$\mathbf{T_J}$ = 45 + (16.5 x 2.0) = 78°C.

The system manufacturer's goal of $\mathbf{T_J}$ < 85°C is met in this case.

Example 2:

A module has a $\mathbf{T_A}$ = 55°C max.

The Xilinx FPGA XC4013E is in a PQ240 package (HQ240 is also considered).

A logic design in XC4013E is determined to be 2.50 Watts. The module manufacturer's goal is to achieve $\mathbf{T_J}$(max.) < 100°C.

Table 2-2 shows the package and thermal enhancement combinations required to meet the goal of $\mathbf{T_J}$ < 100°C.

Table 2-2: **Thermal Resistance for XC4013E in PQ240 and HQ240 Packages**

Device Name	Package	θ_{JA} still air	θ_{JA} (250 LFM)	θ_{JA} (500 LFM)	θ_{JA} (750 LFM)	θ_{JC}	Comments
XC4013E	PQ240	23.7	17.5	15.4	14.3	2.7	Cu, SMT 2L / 0P
XC4013E	HQ240	12.5	8.6	6.9	6.2	1.5	4-Layer Board data

For all solutions, the junction temperature is calculated as: $\mathbf{T_J}$ = Power x θ_{JA} + $\mathbf{T_A}$. All solutions meet the module requirement of less than 100°C, with the exception of the PQ240 package in still air. In general, depending on ambient and board temperatures conditions, and most importantly the total power dissipation, thermal enhancements such as forced air cooling, heat sinking, etc., may be necessary to meet the $\mathbf{T_J}$(max) conditions set.

Possible Solutions to meet the module requirements of 100°C:

a. Using the standard PQ240: $\mathbf{T_J}$ = 55 + (23.7 x 2.50) = 114.25°C.

b. Using standard PQ240 with 250 LFM forced air: $\mathbf{T_J}$ = 55 + (17.5 x 2.50) = 98.75°C

c. Using standard HQ240: $\mathbf{T_J}$ = 55 + (12.5 x 2.50) = 86.25°C

d. Using HQ240 with 250 LFM forced air: $\mathbf{T_J}$ = 55 + (8.6 x 2.50) = 76.5°C.

Heatsink Calculation:

Example illustrating the use of heatsink:

Device is **XCV1000E-FG680** –

There is a need for external thermal enhancements

Data supplied from Xilinx on XCV1000E-FG680 is shown in Table 2-3

Table 2-3: **Data supplied from Xilinx on XCV1000E-FG680**

Package Code	JA(0) °C/W	JC °C/W	JA-250 °C/W	JA-500 °C/W	JA-750 °C/W
FG680	10.6	0.9	7.5	6.1	5.6

- Customer requirements
  - Ta = 50°C
  - Power = 8.0 Watts (user's estimate)
  - User does not want to exceed $\mathbf{T_J}$(max) of 100°C
- Determination with base Still Air data:
  - $\mathbf{T_J} = \mathbf{T_A} + (\theta_{JA}) * P$
  - $\mathbf{T_J} = 50 + 8 * 10.6 = 134.8°C$
  - Unacceptable! θ_{JA} in still air will not work since the 134.8°C is beyond the stated goal of 100°C or less.
- Calculating acceptable thermal resistance:
  - Determine what θ_{JA} will be required to stay below 100°C with the 8 Watts power?
  - Thermal budget = $(\mathbf{T_J} - \mathbf{T_A})$ = 50°C.
  - $\theta_{JA} = (50) / 8 = 6.25°C / Watt$.
  - The package and any enhancement to it need to have an effective thermal resistance from the junction to ambient less than 6.25°C / Watt. That becomes the goal any thermal solution ought to meet.
- **Solution Options**:
  - The bare package with 500 LFM (2.54 meters / s) of air will give θ_{JA} = 6.1°C / Watt. (from the data table above). That will be a workable option, if that much airflow will be tolerable.
  - Heatsink calculation. With a heatsink, heat will now pass through the package (θ_{JC}) then through an interface material (θ_{CS}), and from the heatsink to ambient (θ_{SA}). This can be expressed as follows:
    - $\theta_{JA} \leq \theta_{JC} + \theta_{CS} + \theta_{SA}$
    - $6.25 \leq 0.9+0.1+ \theta_{SA}$

    where
    - 6.25°C / Watt is the condition to be met
    - 0.9°C / Watt — θ_{JC} from data
    - 0.1°C / Watt — θ_{CS} from interface material data
  - From above $\theta_{SA} \leq 5.25°C / Watt$
  - Objective will be to look for a heatsink with θ_{SA} **< 5.25°C/Watt** that meets the physical constraints in the system
  - Passive heatsink with some air flow — 250 LFM (1.25m / s) can be selected
  - Active heatsinks — it may be possible to use small low-profile heatsinks with DC fans

Thermal Data Comparison

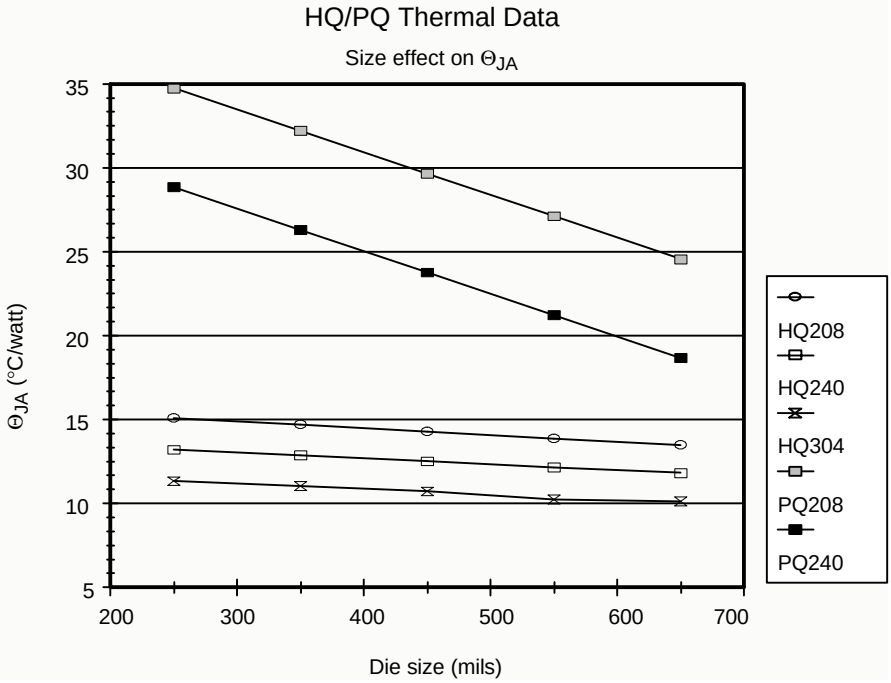


Figure 2-4: **HQ/PQ Thermal Data**

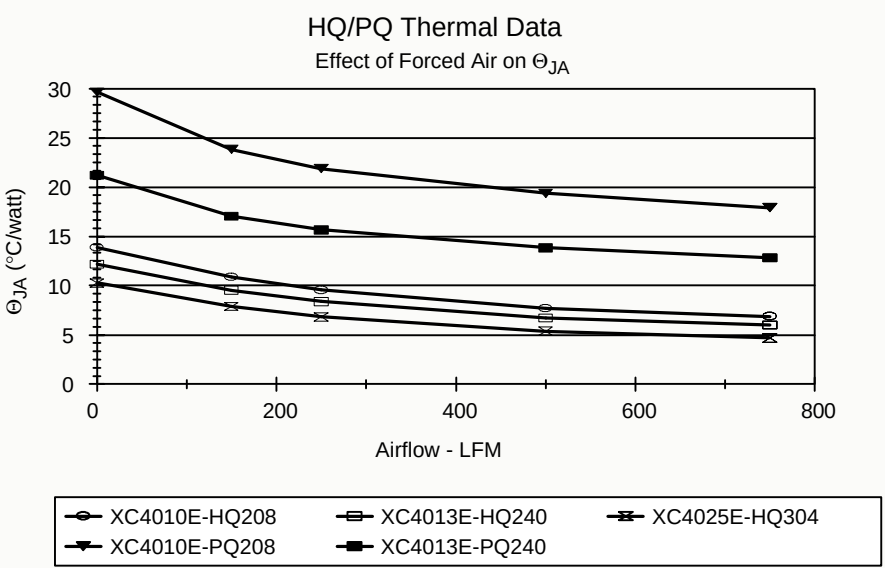


Figure 2-5: **HQ/PQ Thermal Data**

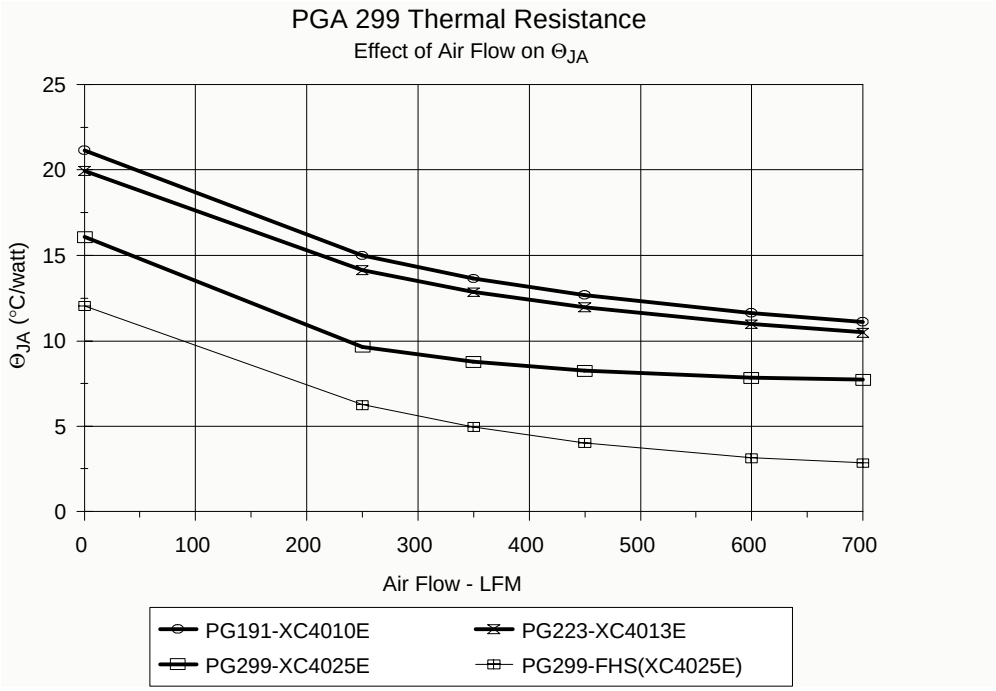


Figure 2-6: **PGA299 Thermal Resistance**

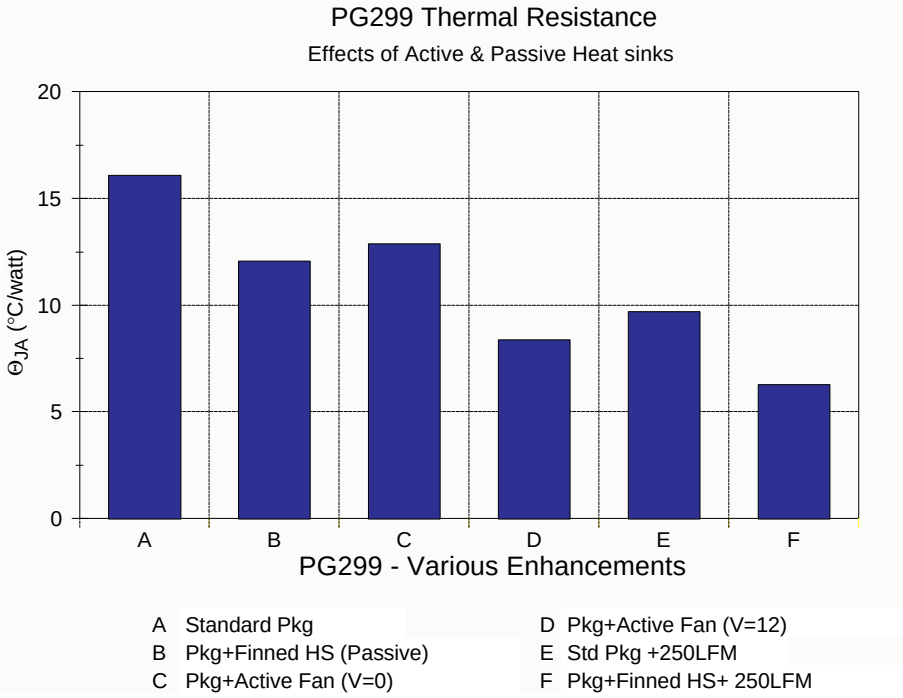


Figure 2-7: **PG299 Thermal Resistance**

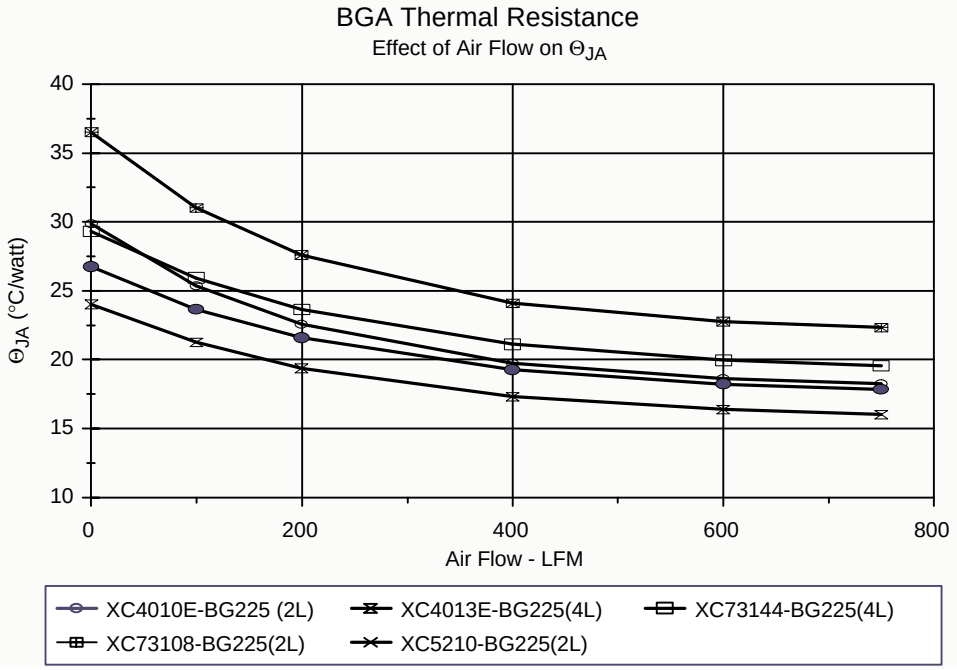


Figure 3: **BGA Thermal Resistance**

Some Power Management Options

The variety of applications that the FPGA devices are used in makes it a challenge to anticipate the power requirements and thus the thermal management needs a particular user may have. While Xilinx programmable devices may not be the dominating power consumers in some systems, it is conceivable that high-gate-count FPGA devices will be exercised sufficiently to generate considerable heat.

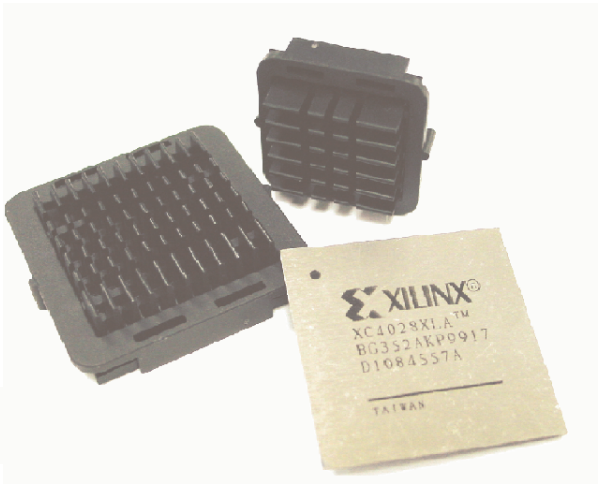
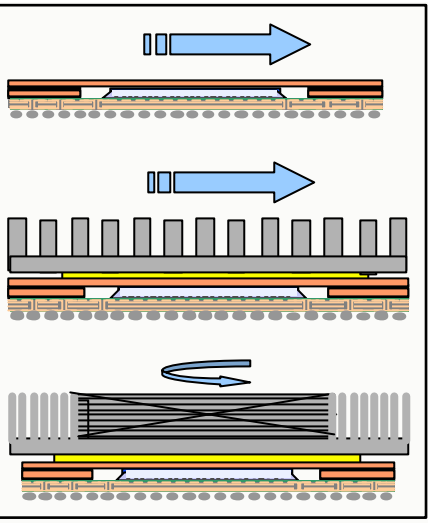


Table 2-4: **Enhanced BGA with Low Profile Retainer Type Passive Heatsinks**

In general, high-I/O and high-gate-count Virtex™-class devices have the potential of being clocked to produce high wattage. Being aware of this potential in power needs, the package offering for these devices includes medium- and high-power-capable package options. This allows a system designer to further enhance these high-end BGA packages to handle more power.

When the actual or estimated power dissipation appears to be more than the specification of the bare package, some thermal management options can be considered. The accompanying Thermal management chart illustrates the incremental nature of the recommendations — ranging from simple airflow to schemes that can include passive heatsinks and active heatsinks.

Low End 1-6 Watts	Bare Package with Moderate Air 8-12˚C/Watt	Bare Package. Package may be used with moderate airflow within a system.	
Mid Range 4-10 Watts	Passive H/S + Air 5-10˚C/Watt	Package used with various forms of Passive Heatsinks and Heat spreader techniques.	
High End 8-20 Watts	Active Heatsink 2-3˚C/Watt or better	Package used with Active Heatsinks TEC and Board level Heat spreader techniques.	

DS076_09_111200

Figure 2-1: **Thermal Management — Incremental Options**

The use of heatpipes, and even liquid-cooled heat plates, may be considered in the extreme for some of these packages. Details on the engineering designs and analysis of some of these suggested considerations may require the help of thermal management consultants. The references listed at the end of this section can provide heatsink solutions for industry-standard packages.

Some of the options available in thermal management may include the following:

- Most high-gate-count Xilinx devices come in more than two package types. Explore thermally enhanced package options available for devices. The quad packages and some BGA packages have heat enhancement options. Typically, 25% to 40% improvement in thermal performance can be expected from these heatsink-embedded packages.
- In a system design, natural convection can be enhanced with venting in the system enclosure. This will effectively lower the Ta and increase available thermal budget for moderate power dissipation.
- The use of forced-air fans is the next step beyond natural convection, and it can be an effective way to improve thermal performance. As seen on the graphs and the calculations above, forced air (200-300 LFM) can reduce junction-to-ambient thermal resistance by up to 30%.

- For moderate power dissipation (2 to 5 Watts), the use of passive heatsinks and heat spreaders attached with thermally conductive double-sided tapes or retainers can offer quick solutions.
- The use of lightweight finned external passive heatsinks can be effective for dissipating up to 8 Watts on some packages. If implemented with forced air as well, the benefit can be a 40% to 50% reduction as illustrated in the XCV1000E-FG680 example. The more efficient external heatsinks tend to be tall and heavy. When using a bulky heatsink, it is advisable to use spring-loaded pins or clips to reduce heatsink-induced stress on the solder joints of the component as these pins or clips help transfer the mounting stress to the circuit board. The diagonals of some of these heatsinks may be designed with extensions to allow direct connection to the board (see Figure 2-2).

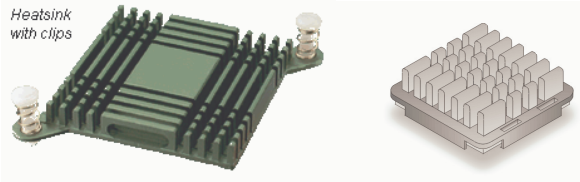


Figure 2-2: **Heatsink with Clips**

- Exposed metal heatsink packages: All thermally enhanced BGAs with dies facing down (including these package codes - BG352, BG432, BG560, FG680, FG860, and FlipChip BGAs) are offered with exposed metal heatsink at the top. These are considered high-end thermal packages and they lend themselves to the application of external heatsinks (passive or active) for further heat removal efficiency. Again, precautions should be taken to prevent component damage when a bulky heatsink is attached.
- Active heatsinks may include a simple heatsink incorporating a mini fan or even Peltier Thermoelectric Coolers (TECs) with a fan to carry away any heat generated. Any consideration of applying TEC in heat management should include consultation with experts in using the devices, as these devices can be reversed and this may damage components. Also, condensation can be an issue.
- Molded packages (FG456, FG676, FG1156, PQs, etc.) without exposed metal at the top also can use these heatsinks at the top for further heat reduction. These BGA packages are similar in construction to those used in graphic cards in PC applications, and heatsinks used for those applications can easily be used for these packages as well. In this case, the θ_{JC} resistance will be the limiting consideration.

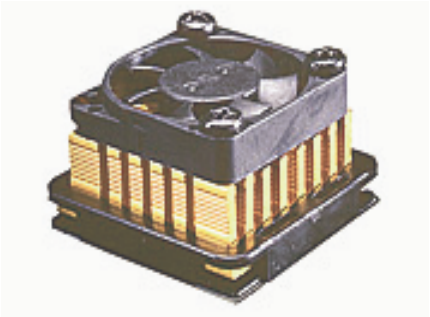


Figure 2-3: **Example of Active Heatsink for BGA (Malico)**

- Outside the package itself, the board on which the package sits can have a significant impact on thermal performance. Board designs can be implemented to take advantage of a board's ability to spread heat. Heat flows to the outside of a package and is sunk into the board to be conducted away – through heatpipes or by normal convection. The effect of the board will be dependent on the size and how it conducts heat. Board size, the level of copper traces on it, and the number of buried copper planes all lower the θ_{JA} thermal resistance for a package mounted on it. Some of the heatsink packages – like HQ, with the exposed heatsink on the board side – can be glued to the board with thermal compound to enhance heat removal into the board. BGA packages with full matrix of balls can be cooled with this scheme. Users need to be aware that a direct heat path to the board from a component also exposes the component to the effect of other heat sources, particularly if the board is not cooled effectively. An otherwise cooler component can be heated by other heat-contributing components on the board.
- A Xilinx lower voltage version of the equivalent circuit in the same or similar package. With the product and speed grade of choice, a power reduction of up to a 40% can be anticipated for a 5.0V to a 3.3V version. Not all products have equivalent lower voltage versions.

See "Websites for Heatsink Sources" in Appendix for lists of websites that offer more information on heat management and sources for interface material.

Chapter 3

Package Electrical Characteristics

Introduction

In high-speed systems, the effects of electrical package parasitics become very critical when optimizing for system performance. Such problems as ground bounce and crosstalk can occur due to the inductance, capacitance, and resistance of package interconnects. In digital systems, such phenomena can cause logic error, delay, and reduced system speed. A solid understanding and proper usage of package characterization data during system design simulation can help prevent such problems.

Theoretical Background

Three major electrical parameters are used to describe package performance: resistance, capacitance, and inductance. Also known as interconnect parasitics, they can cause many serious problems in digital systems. For example, a large resistance can cause RC and RL off-chip delays, power dissipation, and edge-rate degradation. Large capacitance can cause RC delays, crosstalk, edge-rate degradation, and signal distortion. Lead inductance, perhaps the most damaging parasitic in digital circuitry, can cause such problems as ground bounce (also known as simultaneous switching noise or delta-I noise), RL delays, crosstalk, edge rate degradation, and signal distortion.

Ground bounce is the voltage difference between any two grounds (typically between an IC and circuit board ground) induced by simultaneously switching current through bondwire, lead, or other interconnect inductance.

When IC outputs change state, large current spikes result from charging or discharging the load capacitance. The larger the load capacitance and faster the rise / fall times, the larger the current spikes are: $I = C * dv / dt$. Current spikes through the IC pin and bondwire induces a voltage drop across the leads and bondwires: $V = L * di / dt$. The result is a momentary voltage difference between the internal IC ground and system ground, which show up as voltage spikes and unswitched outputs.

Factors that affect ground bounce include:

- rise and fall times
- load capacitance
- package inductance
- number of output drivers sharing the same ground path
- device type

Analytical Formulas for Lead Inductance

Rectangular Leadframe / Trace (straight)

$$L_{self} = 51\left[\text{in}\left(\frac{21}{w + t} \right) + 1/2 \right] \quad \text{nH}$$

(no ground)

$$L_{self} = 51\left[\text{in}\left(\frac{8h}{w + t} \right) + \left(\frac{w + t}{4h} \right) \right] \quad \text{nH}$$

(above ground)

l = lead / trace length

w = lead / trace width

t = lead / trace thickness

h = ground height

unit = inches

Bondwire (gold wire)

$$L_{wire} = 51\left[\text{in}\left(\frac{21}{r} \right) + 3/4 \right] \quad \text{nH}$$

L = wire length

r = wire radius

unit = inches

General Measurement Procedure

Xilinx uses the Time-Domain Reflectometry (TDR) method for parasitic inductance and capacitance measurements. The main components of a TDR setup includes: a digitizing sampling oscilloscope, a fast rise time step generator (<17 ps), a device-under-test (DUT) interface, and an impedance-profile analysis software to extract parasitic models from the TDR reflection waveforms. In this method, a voltage step is propagated down the package under test, and the incident and reflected voltage waves are monitored by the oscilloscope at a particular point on the line. The resulting characteristic impedance of the package interconnect shows the nature (resistive, inductive, and capacitive) of each discontinuity.

Package and Fixture Preparation

Before performing the measurements, the package and the DUT interface must be fixtured. Proper fixturing ensures accurate and repeatable measurements. The mechanical sample for all inductance (self and mutual) measurements are finished units with all leads shorted to the internal ground. For packages without an internal ground (i.e., QFP, PLCC, etc.) the die-paddle is used instead. The mechanical sample for all capacitance (self and mutual) measurements are finished units with all internal leads floating.

The DUT interface provides a physical connection between the oscilloscope and the DUT with minimum crosstalk and probe / DUT reflection. It also provides a small ground loop to minimize ground inductance of the fixture.

Inductance and Capacitance Measurement Procedure

For inductance measurements, a minimum of 25% and maximum of 50% of packages leads, including all leads that are adjacent to the lead(s) under test, are insulated from the DUT fixture ground. All other leads, except for the lead(s) under test, are grounded. This insulation forces the current to return through a low impedance path created on the opposite side of the package. It also eliminates mutual coupling from the neighboring leads. Self-inductance is measured by sending a fast risetime step waveform through the lead under test. The inductive reflection waveform through the lead and the bondwire is then obtained. This reflection waveform, which includes the inductance of the die-paddle (for QFP and PLCC-type packages) and parallel combination of leads in the return path, is the self-inductance. The parasitic effects of the return path are small enough to ignore in the context of this method. For mutual-inductance measurement, two adjacent leads are probed. A fast risetime step waveform is sent through one of the leads. The current travels through the lead / bondwire and returns by the path of the low-impedance ground. On the adjacent "quiet" lead, a waveform is induced due to mutual coupling. This waveform is measured as the mutual inductance.

For capacitance measurements, all external leads except for the lead(s) under test are grounded to the DUT fixture. For QFP, PLCC, and Power Quad-type of packages, the die-paddle and the heat slug are left floating. Self-capacitance is measured by sending a fast risetime step waveform through the lead under test. The reflection waveform from the lead, which includes the sum of all capacitive coupling with respect to the lead under test, is then measured. Appropriately, the self-capacitance can also be called the "bulk" capacitance since the measured value includes the capacitance between the lead under test and all surrounding metal, including the ground plane and the heat slug. For mutual-capacitance measurement, two adjacent leads are probed. An incident waveform is sent through one lead, and the induced waveform on the neighboring lead is measured as the mutual capacitance.

In order to de-embed the electrical parasitics of the DUT fixture and the measuring probes, the short and the open compensation waveforms are also measured after each package measurement. This procedure compensates the DUT fixture to the very tip of the probes.

Inductance and Capacitance Model Extraction

All measured reflection waveforms are downloaded to a PC running the analysis software for package parasitic model extraction. The software uses a method called the Z-profile algorithm, or the impedance-profile algorithm, for parasitic analysis. This method translates the downloaded reflection waveforms into true impedance waveforms, from which package models for inductance and capacitance are extracted.

Data Acquisition and Package Electrical Database

Xilinx acquires electrical parasitic data only on the longest and the shortest lead / traces of the package. This provides the best and the worst case for each package type (defined by package design, lead / ball count, pad size, and vendor). For convenience, the corner interconnects are usually selected as the longest interconnect, while the center interconnects are usually selected as the shortest.

For symmetrical quad packages, all four sides of the package are measured and averaged. Three to five samples are usually measured for accuracy and continuity purposes. The average of these samples is then kept as the official measured parasitic data of that package type in the database.

Chapter 4

Moisture Sensitivity of PSMCs

Moisture-Induced Cracking During Solder Reflow

The surface mount reflow processing step subjects the Plastic Surface Mount Components (PSMC) to high thermal exposure and chemicals from solder fluxes and cleaning fluids during board mount assembly. The plastic mold compounds used for device encapsulation are, universally, hygroscopic and absorb moisture at a level determined by storage environment and other factors. Entrapped moisture can vaporize during rapid heating in the solder reflow process generating internal hydrostatic pressure. Additional stress is added due to thermal mismatch, and the Thermal Coefficient of Expansion (TCE) of plastic, metal lead frame, and silicon die. The resultant pressure may be sufficient to cause delamination within the package, or worse, an internal or external crack in the plastic package. Cracks in the plastic package can allow high moisture penetration, inducing transport of ionic contaminants to the die surface and increasing the potential for early device failure. Cracks in the plastic package can also result in broken / lifted bond wires.

How the effects of moisture in plastic packages and the critical moisture content result in package damage or failure is a complex function of several variables. Among them are package construction details—materials, design, geometry, die size, encapsulant thickness, encapsulant properties, TCE, and the amount of moisture absorbed. The PSMC moisture sensitivity has, in addition to package cracking, been identified as a contributor to delamination-related package failure artifacts. These package failure artifacts include bond lifting and breaking, wire neckdown, bond cratering, die attach separation, die passivation, and metal breakage.

Because of the importance of the PSMC moisture sensitivity, both device suppliers and device users have ownership and responsibility. The background for present conditions, moisture sensitivity standardized test and handling procedures have been published by two national organizations. Users and suppliers are urged to obtain copies of both documents (listed below) and use them rigorously. Xilinx adheres to both.

- IPC / JEDEC J-STD-020B

  “Moisture / Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.” Available on www.jedec.org website.

- IPC / JEDEC J-STD-033A

  “Standard for Handling, Packing, Shipping, and Use of Moisture / Reflow Sensitive Surface Mount Devices.” Available on www.jedec.org website.

  None of the previously stated or following recommendations apply to parts in a socketed application. For board mounted parts careful handling by the supplier and the user is vital. Each of the above publications has addressed the sensitivity issue and has established eight levels of sensitivity (based on the variables identified). A replication of those listings, including the preconditioning and test requirements, and the factory floor life conditions for each level are outlined in Table 4-1. Xilinx devices

are characterized to their proper level as listed. This information is conveyed to the user via special labeling on the Moisture Barrier Bag (MBB).

In Table 4-1, the level number is entered on the MBB prior to shipment. This establishes the user's factory floor life conditions as listed in the time column. The soak requirement is the test limit used by Xilinx to determine the level number. This time includes manufacturer's exposure time or the time it will take for Xilinx to bag the product after baking.

Table 4-1: **Package Moisture Sensitivity Levels**

Level	Floor Life		Soak Requirements			
			Standard		Accelerated Equivalent(1)	
	Time	Conditions	Time (hours)	Conditions	Time (hrs)	Conditions
1	Unlimited	≤30°C / 85% RH	168 +5 / -0	85°C / 85% RH		
2	1 year	≤30°C / 60% RH	168 +5 / -0	85°C / 60% RH		
2a	4 weeks	≤30°C / 60% RH	696(2) +5 / -0	30°C / 60% RH	120 +1 / -0	60°C / 60% RH
3	168 hours	≤30°C / 60% RH	192(2) +5 / -0	30°C / 60% RH	40 +1 / -0	60°C / 60% RH
4	72 hours	≤30°C / 60% RH	96(2) +2 / -0	30°C / 60% RH	20 +0.5 / -0	60°C / 60% RH
5	48 hours	≤30°C / 60% RH	72(2) +2 / -0	30°C / 60% RH	15 +0.5 / -0	60°C / 60% RH
5a	24 hours	≤30°C / 60% RH	48(2) +2 / -0	30°C / 60% RH	10 +0.5 / -0	60°C / 60% RH
6	Time on Label (TOL)	≤30°C / 60% RH	TOL	30°C / 60% RH		

Notes:

1. **CAUTION** - The "accelerated equivalent" soak requirements shall not be used until correlation of damage response, including electrical, after soak and reflow is established with the "standard" soak requirements or if the known activation energy for diffusion is 0.4 - 0.48 eV. Accelerated soak times may vary depending on material properties; for example, mold compound, encapsulant, etc. JEDEC document JESD22-A120 provides a method for determining the diffusion coefficient.
2. The standard soak time includes a default value of 24 hours for the semiconductor manufacturer's exposure time (MET) between bake and bag and includes the maximum time allowed out of the bag at the distributor's facilitiy.

   If the actual MET is less than 24 hours the soak time may be reduced. For soak conditions of 30°C / 60% RH, the soak time is reduced by one hour for each hour the MET is less than 24 hours. For soak conditions of 60°C / 60% RH, the soak time is reduced by one hour for each five hours the MET is less than 24 hours.

   If the actual MET is greater than 24 hours, the soak time must be increased. If soak conditions are 30°C / 60% RH, the soak time is increased one hour for each hour that the actual MET exceeds 24 hours. If soak conditions are 60°C / 60% RH, the soak time is increased one hour for each five hours that the actual MET exceeds 24 hours.
3. Suppliers may extend the soak time at their own risk.

Factory Floor Life

Factory floor life conditions for Xilinx devices are clearly stated on the MBB containing moisture sensitive PSMCs. These conditions have been ascertained by following test methods outlined in IPC / JEDEC J-STD-020B and are replicated in Table 4-1. If factory floor conditions are outside the stated environmental conditions (30°C / 85% RH for Level 1, and 30°C / 60% RH for Levels 2-6) or if time limits have been exceeded, then recovery can be achieved by baking the devices before the reflow step. Identified in the next section are two acceptable bake schedules. Either can be used for recovery to the required factory floor level.

Dry Bake Recommendation and Dry Bag Policy

Xilinx recommends, as do the mentioned publications and other industry studies, that all moisture sensitive PSMCs be baked prior to use in surface mount applications, or comply strictly with requirements as specified on the MBB. Tape and Reeled parts are universally dry packed. Level 1 parts are shipped without the need for, or use of, an MBB. Note that to maintain level-1 status, the parts should be stored under conditions specified in Table 4-1 ($\leq$30ºC / 85% RH).

Two bake schedules have been identified as acceptable and equivalent. The first is 24 hours in air at 125°C, in shipping media capable of handling that temperature. The second bake schedule is for 192 hours in a controlled atmosphere of 40°C, equal to or less than 5% RH. Dry Devices are sealed in special military specification Moisture Barrier Bags (MBB). Enough desiccant pouches are enclosed in the MBB to maintain contents at less than 20% RH for up to 12 months from the date of seal. A reversible Humidity Indicator Card (HIC) is enclosed to monitor the internal humidity level. The loaded bag is then sealed shut under a partial vacuum with an impulse heat sealer.

Artwork on the bags provides storage, handling and use information. There are areas to mark the seal date, quantity, and moisture sensitivity level and other information. The following paragraphs contain additional information on handling PSMCs.

Handling Parts in Sealed Bags

Inspection

Note the seal date and all other printed or hand entered notations. Review the content information against what was ordered. Thoroughly inspect for holes, tears, or punctures that may expose contents. Xilinx strongly recommends that the MBB remain closed until it reaches the actual work station where the parts will be removed from the factory shipping form.

Storage

The sealed MBB should be stored, unopened, in an environment of not more than 90% RH and 40ºC. The enclosed HIC is the only verification to show if the parts have been exposed to moisture. Nothing in the part's appearance can verify moisture levels.

Expiration Date

The seal date is indicated on the MBB. The expiration date for dry packed SMD packages is 12 months from the seal date. If the expiration date has been exceeded or HIC shows exposure beyond 20% upon opening the bag bake the devices per the earlier stated bake schedules. The three following options apply after baking:

Use the devices within time limits stated on the MBB.

Reseal the parts completely under a partial vacuum with an impulse sealer (hot bar sealer) in an approved MBB within 12 hours, using fresh desiccant and HIC, and label accordingly. Partial closures using staples, plastic tape, or cloth tape are unacceptable.

Store the out-of-bag devices in a controlled atmosphere at less than 20% RH. A desiccator cabinet with controlled dry air or dry nitrogen is ideal.

Other Conditions

Open the MBB when parts are to be used. Open the bag by cutting across the top as close to the seal as possible. This provides room for possible resealing and adhering to the reseal conditions outlined above. After opening, strictly adhere to factory floor life conditions to ensure that devices are maintained below critical moisture levels.

Bags opened for less than one hour (strongly dependent on environment) may be resealed with the original desiccant. If the bag is not resealed immediately, new desiccant or the old one that has been dried out may be used to reseal, if the factory floor life has not been exceeded. Note that factory floor life is cumulative. Any period of time when MBB is opened must be added to all other opened periods.

Both the desiccant pouches and the HIC are reversible. Restoration to dry condition is accomplished by baking at 125°C for 10-16 hours, depending on oven loading conditions.

Chapter 5

Reflow Soldering Process Guidelines

Solder Reflow Process

To implement and control the production of surface-mount assemblies, the dynamics of the solder reflow process and how each element of the process is related to the end result must be thoroughly understood.

The primary phases of the reflow process are as follows:

1. Melting the particles in the solder paste
2. Wetting the surfaces to be joined
3. Solidifying the solder into a strong metallurgical bond

The sequence of five actions that occur during this process is shown in Figure 5-1.

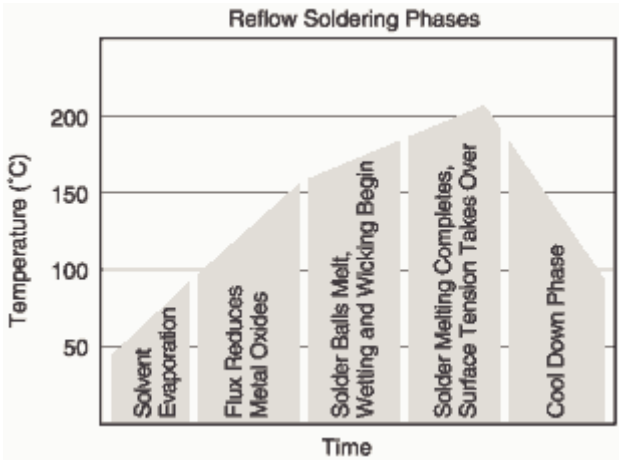


Figure 5-1: **Soldering Sequence**

Soldering Problems Summary

Each phase of a surface mount reflow profile has min / max limits that should be viewed as a process window. The process requires a careful selection and control of the materials, geometries of the mating surfaces (package footprint vs. PCB land pattern geometries) and the time / temperature of the profile. If all of the factors of the process are sufficiently optimized, there will be good solder wetting and fillet formation (between component

leads and the land patterns on the substrate). If factors are not matched and optimized there can be potential problems as summarized in Figure 5-2.

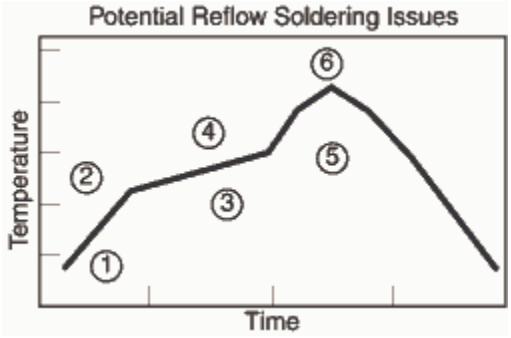


Figure 5-2: **Soldering Problems Summary**

Soldering Problems Summary Notes:

1. Insufficient Temperature to Evaporate Solvent
2. Component Shock and Solder Splatter
3. Insufficient Flux Activation
4. Excessive Flux Activity and Oxidation
5. Trapping of Solvent and Flux, Void Formation
6. Component and/or Board Damage

Typical Conditions for IR Reflow Soldering

Figure 5-3 shows typical conditions for solder reflow processing using IR/Convection. Both IR and Convection furnaces are used for BGA assembly. The moisture sensitivity of Plastic Surface-Mount Components (PSMCs) must be verified prior to surface mount flow. See the preceding sections for a more complete discussion on PSMC moisture sensitivity.

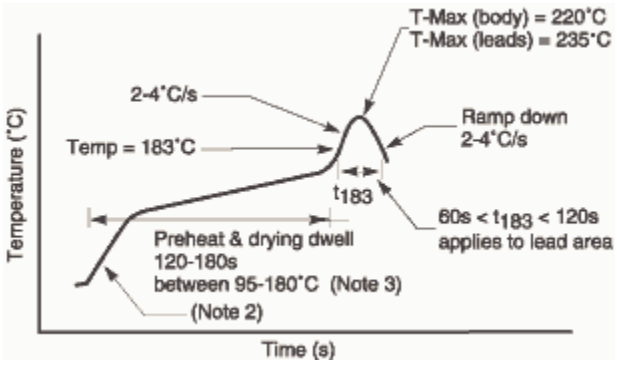


Figure 5-3: **Typical Conditions for IR Reflow Soldering**

Notes:

1. Max temperature range = 220°C (body), 220°C-235°C (leads). Time at temp 30-60 seconds
2. Preheat drying transition rate 2-4°C/s

3. Preheat dwell 95-180°C for 120-180 seconds
4. IR reflow shall be performed on dry packages
5. For MPM BGAs, do not reflow with lid on bottom

Typical Conditions for Vapor Phase Reflow Soldering

The IR process is strongly dependent on equipment and loading differences. Components may overheat due to lack of thermal constraints. Unbalanced loading may lead to significant temperature variation on the board. This guideline is intended to assist users in avoiding damage to the components; the actual profile should be determined by those using these guidelines. For complete information on package moisture / reflow classification and package reflow conditions, refer to the Joint IPC / JEDEC Standard J-STD-020A.

The peak reflow temperature of the PSMC body should not be more than 220°C in order to avoid internal package delamination. For multiple BGAs in a single board, it is recommended to check all BGA sites for varying temperatures because of differences in surrounding components.

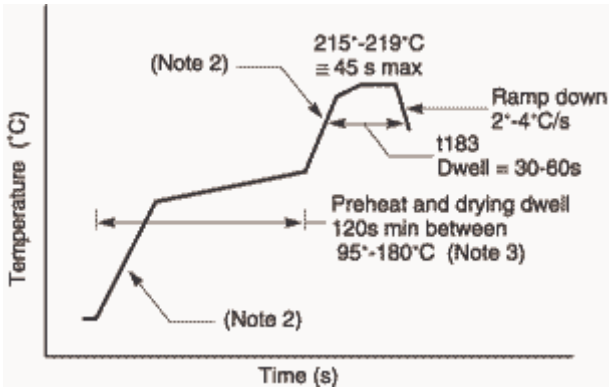


Figure 5-4: **Typical Conditions for Vapor Phase Reflow Soldering**

Notes:

1. Solvent—FC5312 or equivalent—ensures temperature range of leads @ 215-219°C
2. Transition rate 4-5°C / s
3. Dwell is intended for partial dryout and reduces the difference in temperature between leads and PCB land patterns.
4. These guidelines are for reference. They are based on laboratory runs using dry packages. It is recommended that actual packages with known loads be checked with the commercial equipment prior to mass production.

Chapter 6

Tape and Reel

Introduction

Xilinx offers a tape and reel packing for PLCC, BGA, QFP, and SO packages. The packing material is made of black conductive polystyrene and protects the packages from mechanical and electrical damage. The reel material provides a suitable medium for pick and place equipment.

The tape and reel packaging consists of a pocketed carrier tape, sealed with a protective cover. The device sits on pedestals (for PLCC, QFP packages) to protect the leads from mechanical damage. All devices loaded into the tape carriers are baked, lead scanned before the cover tape is attached and sealed to the carrier. In-line mark inspection for mark quality and package orientation is used to ensure shipping quality.

Benefits

- Increased quantity of devices per reel versus tubes improves cycle time and reduces the amount of time to index spent tubes.
- Tape and reel packaging enables automated pick and place board assembly.
- Reels are uniform in size enabling equipment flexibility.
- Transparent cover tape allows device verification and orientation.
- Antistatic reel materials provides ESD protection.
- Carrier design include a pedestal to protect package leads during shipment.
- Bar code labels on each reel facilitate automated inventory control and component traceability.
- All tape and reel shipments include desiccant pouches and humidity indicators to ensure products are safe from moisture.
- Compliant to Electronic Industries Association (EIA) 481. Material and Construction Carrier Tape.
- The pocketed carrier tape is made of conductive polystyrene material, or equivalent, with a surface resistivity level of less than 106 ohms per square inch.
- Devices are loaded “live bug” or leads down, into a device pocket.
- Each carrier pocket has a hole in the center for automated sensing of whether a unit is in the pocket or not.
- Sprocket holes along the edge of the carrier tape enable direct feeding into automated board assembly equipment.

Cover Tape

An anti-static, transparent, polyester cover tape, with heat activated adhesive coating, sealed to the carrier edges to hold the devices in the carrier pockets.

Surface resistivity on both sides is less than 1011 ohms per square inch.

Reel

The reel is made of anti-static polystyrene material. The loaded carrier tape is wound onto this conductive plastic reel.

A protective strip made of conductive polystyrene material is placed on the outer part of the reel to protect the devices from external pressure in shipment.

Surface resistivity is less than 1011 ohms per square inch.

Device loading orientation is in compliance with EIA Standard 481.

Bar Code Label

The bar code label on each reel provides customer identification, device part number, date code of the product and quantity in the reel.

Print quality are in accordance with ANSI X3.182-1990 Bar Code Print Quality Guidelines. Presentation of Data on labels are EIA-556-A compliant.

The label is an alphanumeric, medium density Code 39 labels.

This machine-readable label enhances inventory management and data input accuracy.

Shipping Box

The shipping container for the reels are in a 13" x 13" x 3" C-flute, corrugated, #3 white “pizza box,” rated to 200 lb. test.

Table 6-1: **Tape and Reel Packaging**

Package Code	Qty. Per Reel	Reel Size (inches)	Carrier Width (mm)	Cover Width (mm)	Pitch (mm)
BG225(1)	500	13	44	37.5	32
BG256(1)	500	13	44	37.5	32
BG272(1)	500	13	44	37.5	32
CP56(1)	4000	13	12	9.2	8
CS48(1)	1500	13	16	13.3	12
CS144(1)	2000	13	24	21.0	16
FG256(1)	1000	13	24	21.0	20
FG456(1)	500	13	44	37.5	32
FG676(1)	500	13	44	37.5	32
PC20(1)	750	13	16	13.3	12
PC44(1)	500	12	32	25.5	14
PC68(1)	250	13	44	37.5	32
PC84(1)	250	13	44	37.5	36
PQ100	250	13	44	37.5	32
PQ160	200	13	44	37.5	40
SBGA352(1)	200	13	56	49.5	40
SBGA432(1)	200	13	56	49.5	48
SBGA560(1)	200	13	56	49.5	48
SO8	750	7	12	9.2	8
SO20	1000	13	24	21.0	12
TQ100	1000	13	24	21.0	32
TQ144	750	13	44	37.5	24
VO8	750	7	12	9.2	8
VQ44	2000	13	24	21.0	16
VQ64	2000	13	24	21.0	16
VQ100	1000	13	24	21.0	32

Note:

1. In-house capability.

Standard Bar Code Label Locations

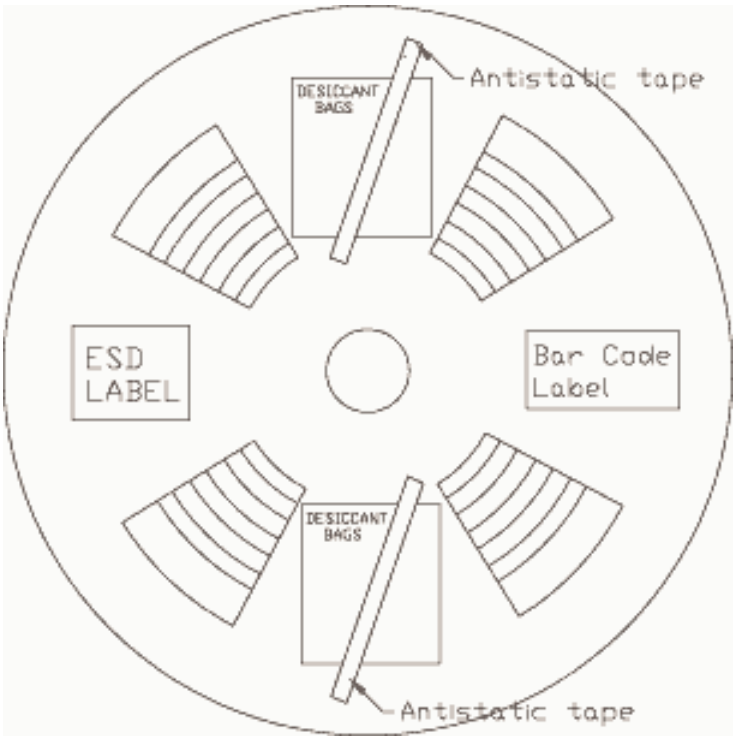


Figure 6-1: **Standard Bar Code Label Locations**

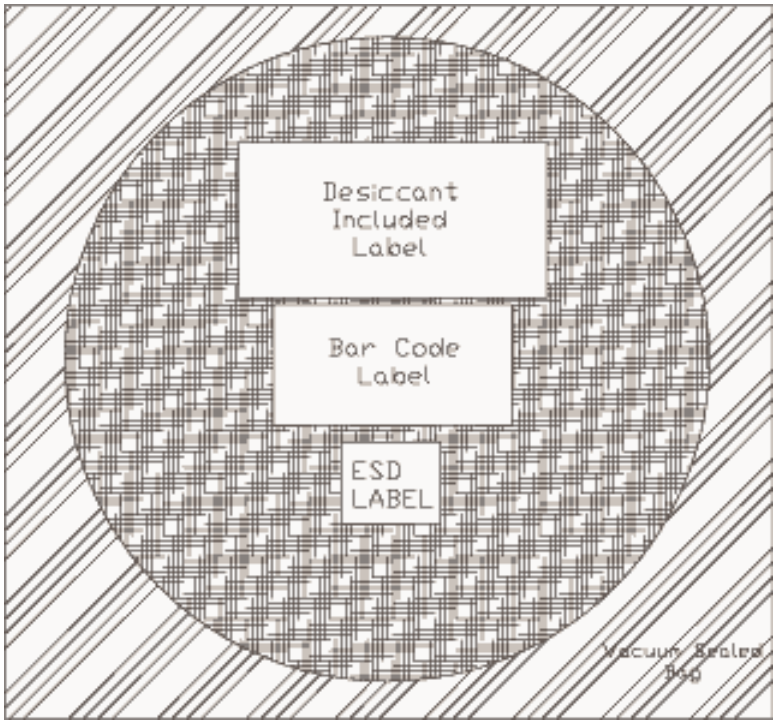


Figure 6-2: **Standard Bar Code Label Locations**

Additional Information

Table of Socket Manufacturers

Table 1 lists manufacturers known to offer sockets for Xilinx Package types. This summary does not imply an endorsement by Xilinx. Each user has the responsibility to evaluate and approve a particular socket manufacturer.

Table-1: **Socket Manufacturers Packages**

Manufacturer	Packages					
	DIP, SO, VO	PC, WC	PQ, HQ, TQ, VQ	PG, PP	CB	BG, CG
Advanced Interconnect 5 Energy Way, P.O. Box 1019 W. Warwick, RI 02893 Toll Free: 1-800-424-9850 www.advintcorp.com	X	X	-	X	-	-
AMP Inc. 470 Friendship Road Harrisburg, PA 17105-3608 (800) 522-6752 www.amp.com	X	X	-	X	-	-
Aries Electronics P.O. Box 130 Frenchtown, NJ 08825 Phone: 908-996-6841 www.arieselec.com	X	X	-	X	-	X
Interconnect Systems, Inc. 708 Via Alondra Camarillo, CA 93012 Phone: 805-482-2870						X
Ironwood Electronics Inc. P.O. Box 21151 St. Paul, MN 55121 Phone: 651-452-8100 www.ironwoodelectronics.com	X	-	-	X	-	X

Table-1: **Socket Manufacturers Packages *(Continued)***

Manufacturer	Packages					
	DIP, SO, VO	PC, WC	PQ, HQ, TQ, VQ	PG, PP	CB	BG, CG
McKenzie Socket Division 910 Page Avenue Fremont, CA 94538 (510) 651-2700	X	X	-	X	-	-
Mill-Max MFG. Corporation 190 Pine Hollow Road P.O. Box 300 Oyster Bay, NY 11771 Phone: 516-922-6000 www.mill-max.com	X	X	-	X	-	X
3M Textool 6801 River Place Blvd. Austin, TX 78726-9000 (800) 328-0411 www.3m.com				X	X	X
Wells Electronics 1701 South Main Street South Bend, IN 46613-2299 (219) 287-5941 www.wellscti.com				X		
Yamaichi Electronics Inc. 2235 Zanker Road San Jose, CA 95131 (408) 456-0797 www.yeu.com		X	X	X	X	

Websites for Heatsink Sources

http://www.wakefield.com

http://www.aavid.com or www.thermalloy.com

http://www.chipcoolers.com

http://www.metalsgroup.com

http://www.malico.com.tw

http://www.pinfin.com

http://www.alphanovatech.com

GlobalWin: http://www.globalwin.com.tw

http://www.avc.com.tw

ALPHA: http://www.micforg.co.jp

COFAN USA http://www.cofan-usa.com

Websites for Interface Material Sources

Power Devices — http://www.powerdevices.com

Chomerics — http://www.chomerics.com

Bergquist Company — http://www.bergquistcompany.com

AOS Thermal Compound — http://www.aosco.com

Xilinx does not endorse these vendors nor their products. They are listed here for reference only. Any materials or services received from the vendors should be evaluated for compatibility with Xilinx components.

Related Xilinx Websites and Links to Xilinx Packaging Application Notes

Implementing Xilinx Flip-Chip BGA Packages,
http://www.xilinx.com/bvdocs/appnotes/xapp426.pdf

Optimizing Solder Reflow Process for Xilinx BGA Packages,
http://www.xilinx.com/bvdocs/appnotes/xapp425.pdf

Packaging Thermal Management,
http://www.xilinx.com/bvdocs/appnotes/xapp415.pdf

Xilinx Lead Free Packages, http://www.xilinx.com/bvdocs/appnotes/xapp427.pdf

Package drawings,
http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Package+Drawings