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Managing Ground Bounce in Large FPGAs

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Summary

Ground bounce must be controlled to ensure proper operation of high performance FPGA devices. Particular attention must be applied to minimizing board-level inductance during PCB layout. This document describes calculations that help to ensure that a design meets input undershoot and logic-low voltage requirements for devices receiving signals from an FPGA.

Introduction

IC manufacturers have traditionally specified simultaneous switching output (SSO) guidelines for each driver type, based on the number of drivers allowed per power/ground pair. For LVTTL-type drivers, ground bounce can be as much as 800 mV before tripping the input-low threshold. Such a level for ground bounce might no longer be acceptable today.

What Changed?

A number of recent developments warrant revisiting published SSO guidelines. While lead inductance has been whittled down to less than 100 pH per ground pin in flip-chip packages, board-level inductance has more than doubled to a 2-3 nH range in recent years, due to miniaturized vias, smaller trace widths, and increased board thickness. As a result, substantially more ground bounce voltage now develops across the PCB, and this is not fully accounted for in published SSO guidelines. Actual ground bounce voltage on PC boards that use 8 mil vias on 125 mil FR4 material could far exceed the Xilinx ground bounce expectation of 600 mV.

For ease of PCB routing and debugging, there is a tendency to cluster wide buses at one edge of the chip. This causes uneven current distribution and ground bounce within the package. As supply voltage decreases, components can tolerate even less noise. Some new devices tolerate as little as 400 mV undershoot at the input. Also, as load capacitance increases, ground bounce deteriorates. Altogether, these design issues now require more critical handling of ground bounce than ever before.

Package-Level SSO

A key point to note is that ground bounce scales linearly. This makes it possible to determine SSO at the package level for entire designs that use drivers of different types, current strengths, and slew rates.

One criterion for package-level SSO ensures that the number of simultaneously switching outputs does not exceed the per-bank limit. Another criterion ensures even distribution of fast/strong drivers across the package. A final criterion ensures that the chip does not generate excessive ground bounce. A quantity called SSO Allowance is used in both of the latter two constraints, which takes into account design-specific parameters, such as board-level inductance, input logic-low threshold, input undershoot voltage, and output load capacitance.

Hence, the following rules apply at the package level:

- WASSO for any bank cannot exceed 100%.
- Average WASSO of two adjacent banks cannot exceed 105% of SSO Allowance.
- Package WASSO cannot exceed SSO Allowance.

Weighted Average SSO (WASSO) is computed first on a per I/O bank basis, then averaged for two adjacent banks, and averaged across all banks to determine the effective WASSO for the entire package.

SSO Allowance

SSO allowance is a number ranging from 0 to 100% and is a product of three scaling factors.

The *first scaling factor* is determined by dividing Xilinx-assumed inductance by the customer's PCB total inductance, which is calculated from board geometries such as via diameter, board thickness, breakout trace width and length, and so forth.

The *second scaling factor* is determined by dividing the lesser of input undershoot voltage and input logic low threshold by the maximum ground bounce voltage (600 mV) Xilinx uses to establish SSO guidelines.

The *third scaling factor* is determined by dividing the Xilinx ground bounce of 600 mV for a 15 pf load by ground bounce that is extrapolated for loads greater than 15 pf. Xilinx output drivers produce an additional 9 mV of ground bounce for each additional 1 pf of load capacitance.

- First Scaling Factor = 1.0 nH / 1.1 nH
= 90.9%
- Second Scaling Factor = 550 mV / 600 mV
= 91.7%
- Third Scaling Factor = 600 mV / (((22 pF – 15 pF) * 9 mV/pF) + 600 mV)
= 600 mV / 663 mV
= 90.5%
- SSO Allowance = 0.909 * 0.917 * 0.905
= 75.4%.

Calculate Package SSO

A sample calculation of package SSO is shown below for a Virtex™-II XC2V6000 device in an FF1152 package.

For the number of SSOs allowed per power/ground pair and the number of power/ground pairs per bank, refer to SSO guidelines provided in the following documents on www.xilinx.com:

- Virtex-E 1.8V FPGA Product Specification (Module 2)
- *Virtex-II Platform FPGA User Guide*
- *Virtex-II Pro Platform FPGA User Guide*

Step 0: **Calculate the package SSO allowance.**

- (1.0 nH / 1.1 nH) * (550 mV / 600 mV) * (600 mV/ (((22 pF – 15 pF) * 9 mV/pF) + 600 mV))
= 75.4%

Step 1: **Calculate the WASSO for each individual bank, starting with bank 0. Assume a design uses 43 Fast 24 mA drivers, 30 Fast 12 mA drivers, and 22 Slow 8 mA drivers.**

- Percent contribution by 24 mA Fast drivers
= 43 drivers used / (5 Fast 24 mA drivers allowed per V_{CC}/GND pair * 13 pairs in I/O bank 0)
= 43 / 65
= 66.2%
- Percent contribution by 12 mA Fast drivers
= 30 drivers used / (10 Fast 12 mA drivers allowed per V_{CC}/GND pair * 13 pairs in I/O bank 0)
= 30 / 130
= 23.1%
- Percent contribution by 8 mA Slow drivers
= 22 drivers used / (22 Slow 8 mA drivers allowed per V_{CC}/GND pair * 13 pairs in I/O bank 0)
= 22 / 286
= 7.7%
- WASSO for bank 0 = 66.2% + 23.1% + 7.7% = 97%

- Calculate WASSO for banks 1 through 7, as done for bank 0 above.
- For this example, assume WASSOs of 45%, 50%, 60%, 60%, 35%, 40%, and 15% are obtained. Ensure that the WASSO for each bank does not exceed 100%.

Step 2: **Calculate the average WASSO for two adjacent banks, and ensure that the averages do not exceed the SSO allowance.**

- Average WASSO between banks 0 and 1
  = (WASSO of bank 0 + WASSO of bank 1) / 2
  = (97% + 45%) / 2
  = 71.0%
  OK!
- If the average WASSO of two adjacent banks exceeds the SSO allowance, apply ground bounce reduction techniques to these two banks.

Step 3: **Calculate the package WASSO and ensure that it does not exceed the SSO allowance.**

- (Sum of WASSO from all banks) / (number of banks available in the package)
  = (97% + 45% + 50% + 60% + 60% + 35% + 40% + 15%) / 8
  = 50.3%
  OK!
- If the package WASSO exceeds the SSO allowance, apply ground bounce reduction techniques to reduce the WASSO.

WASSO Calculator

A Microsoft Excel-based spreadsheet entitled “WASSO Calculator” is provided that automates the calculations shown above. The WASSO Calculator uses PCB geometry, such as board thickness, via diameter, and breakout trace width and length, to determine board inductance. It determines the smallest undershoot and logic-low threshold voltage among all input devices, calculates the average output capacitance, and determines the SSO allowance by taking into account all of the board-level design parameters mentioned in this document. In addition, the WASSO Calculator performs checks to ensure that the overall design does not exceed the SSO allowance.

This calculator can be downloaded from the Xilinx FTP site:

ftp://ftp.xilinx.com/pub/applications/xapp/xapp689.zip

Conclusion

Ground bounce must be controlled to ensure proper operation of high performance devices. Particular attention must be applied to minimizing board-level inductance during PCB layout. A WASSO Calculator (Excel spreadsheet) is provided to help ensure that your design meets input undershoot and logic-low voltage requirements for devices receiving signals from an FPGA. Follow ground bounce reduction techniques to get WASSOs under control.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/16/03	1.0	Initial Xilinx release.