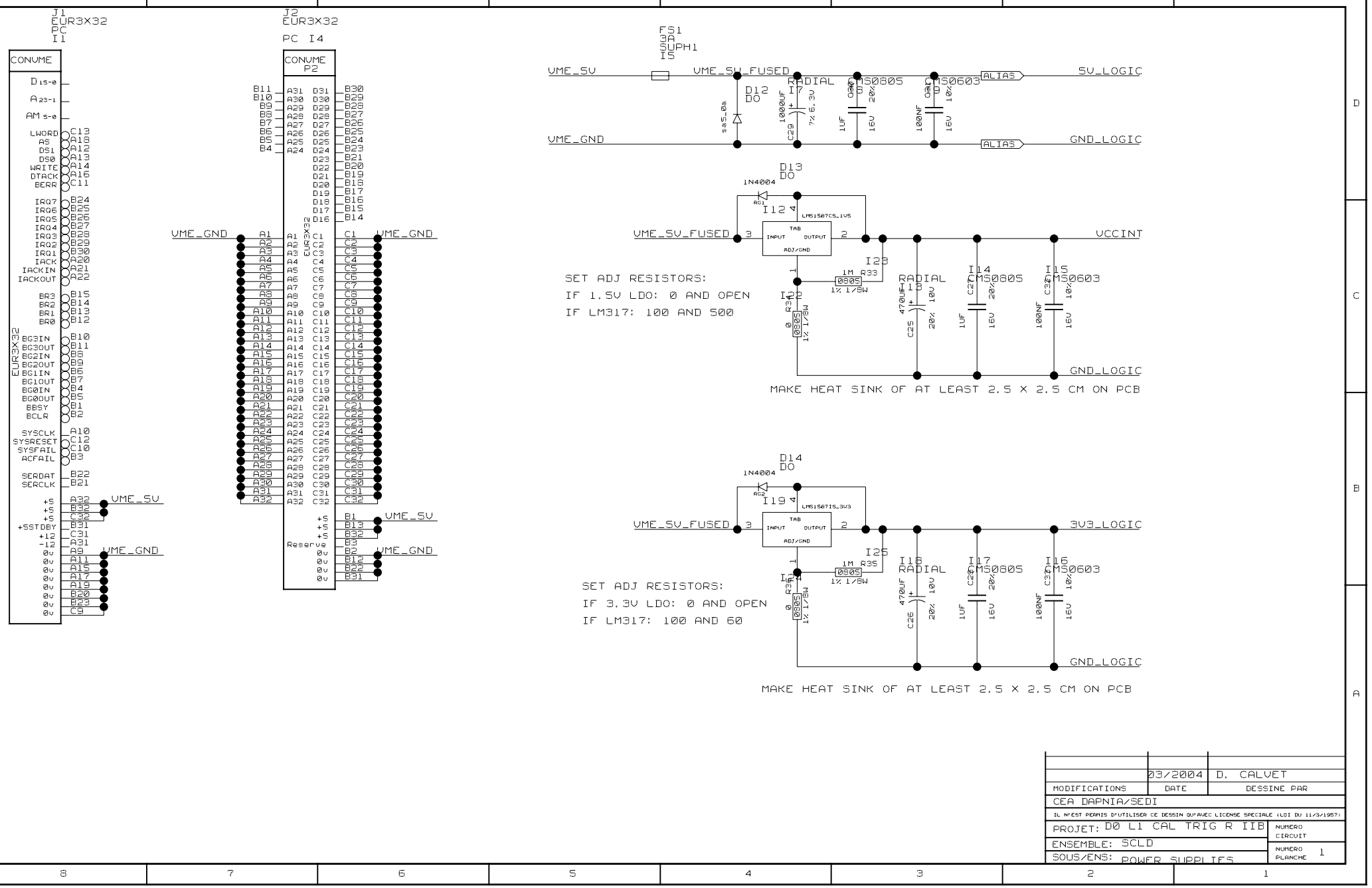
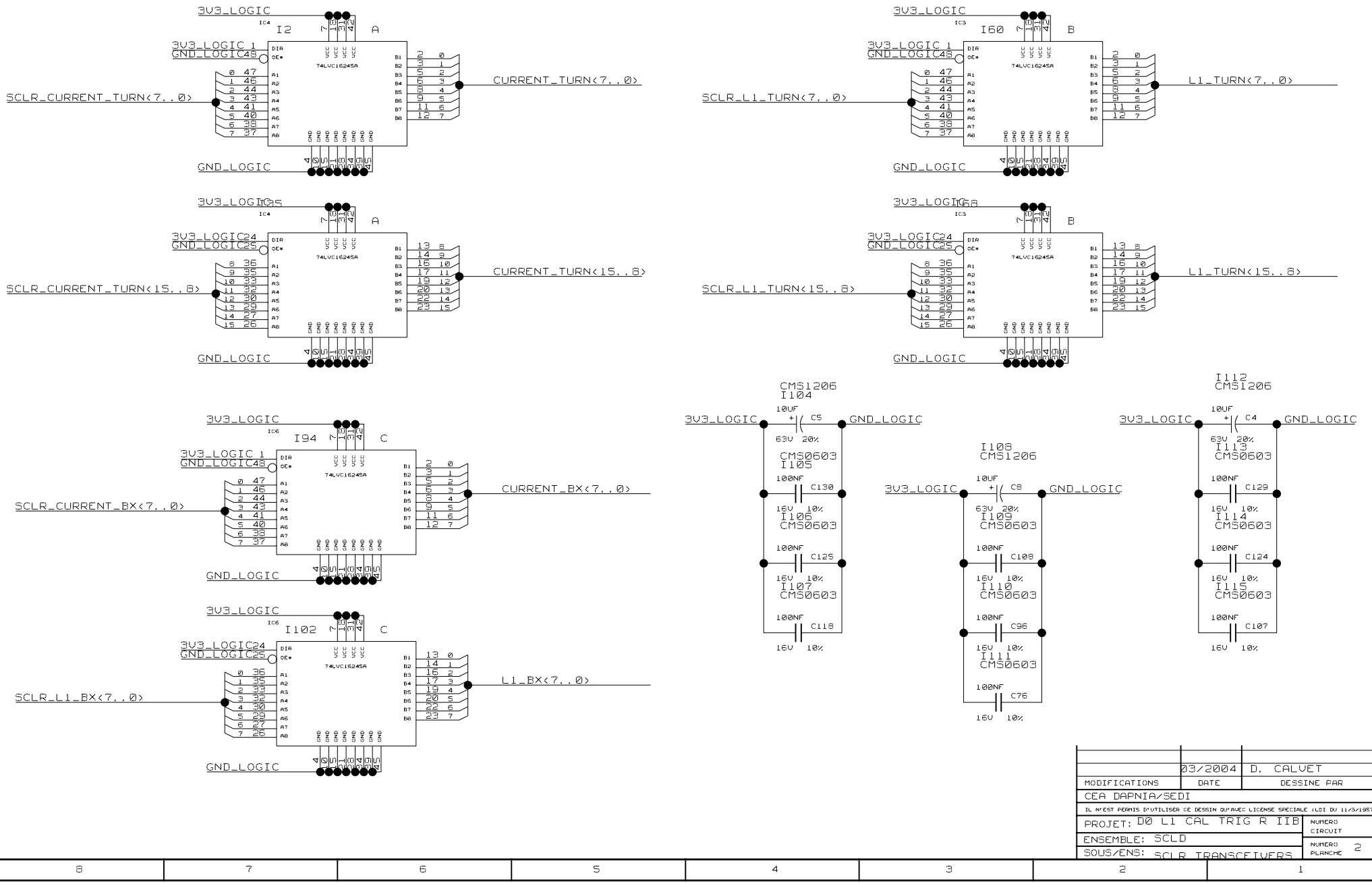
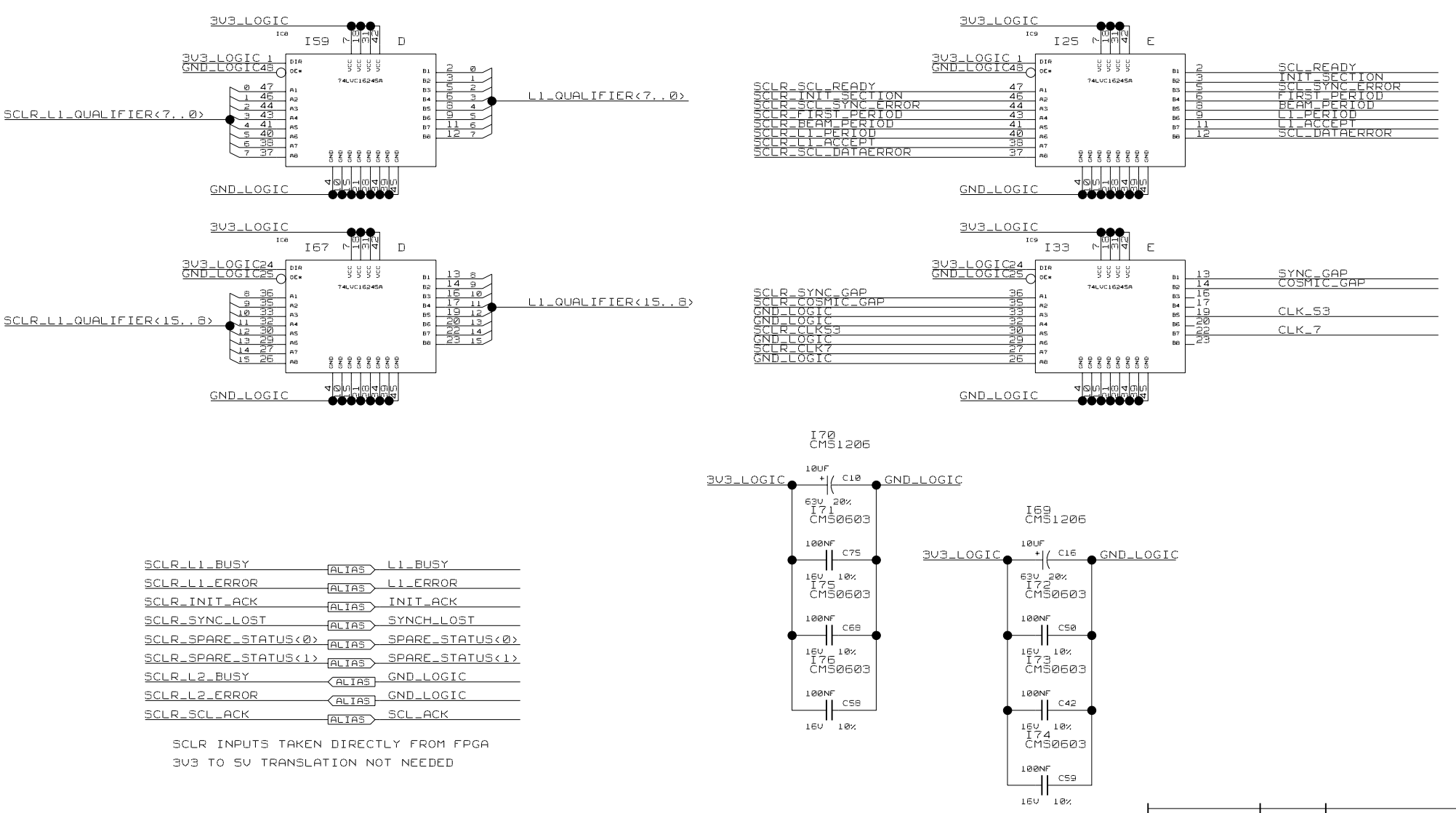


	03/2004	D. CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: D0 L1 CAL TRIG R IIB		NUMERO CIRCUIT
ENSEMBLE: SCLD		
SOUS/ENS: POWER SUPPLIES		NUMERO PLANCHE 1



	03/2004	D. CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: D0 L1 CAL TRIG R IIB		NUMERO CIRCUIT
ENSEMBLE: SCLD		
SOUS/ENS: SCLR TRANSCEIVERS		NUMERO PLANCHE 2



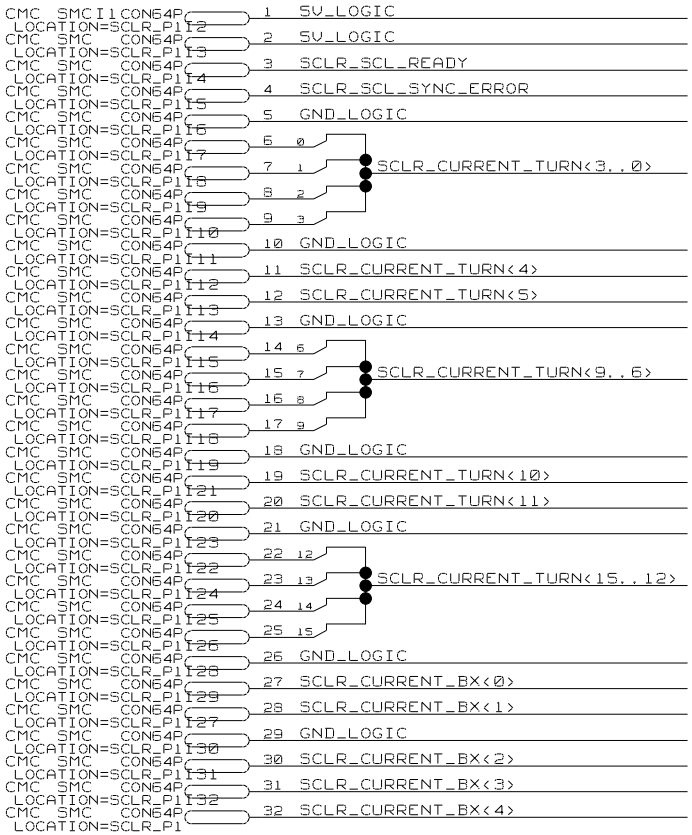
	03/2004	D. CALVET
MODIFICATIONS	DATE	DESSINE PAR

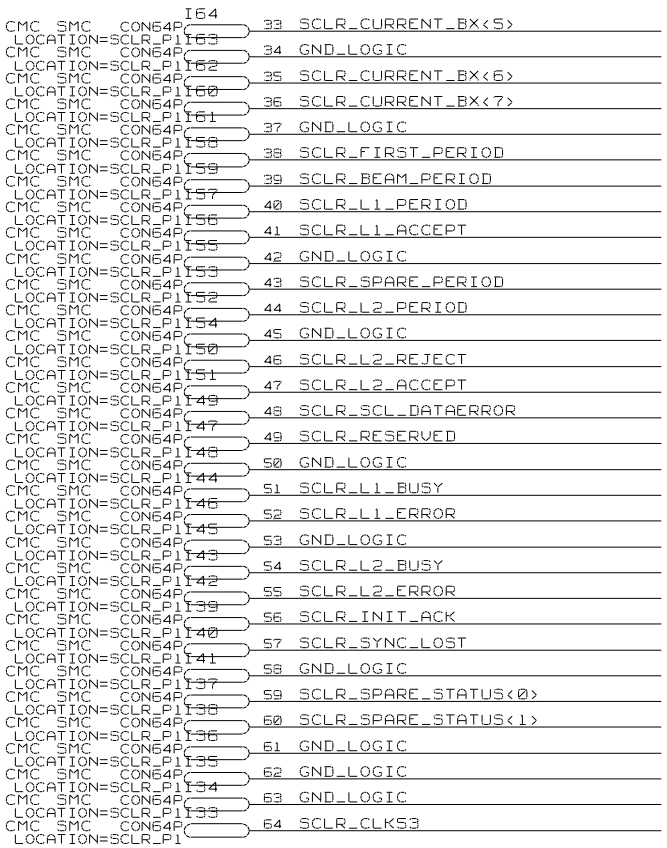
CEA DAPNIA/SEDI

PROJET: D0 L1 CAL TRIG R IIB — NUMERO CIRCUIT

ENSEMBLE: SCLD

SOUS/ENS: SCLR TRANSCEIVERS — NUMERO PLANCHE 3





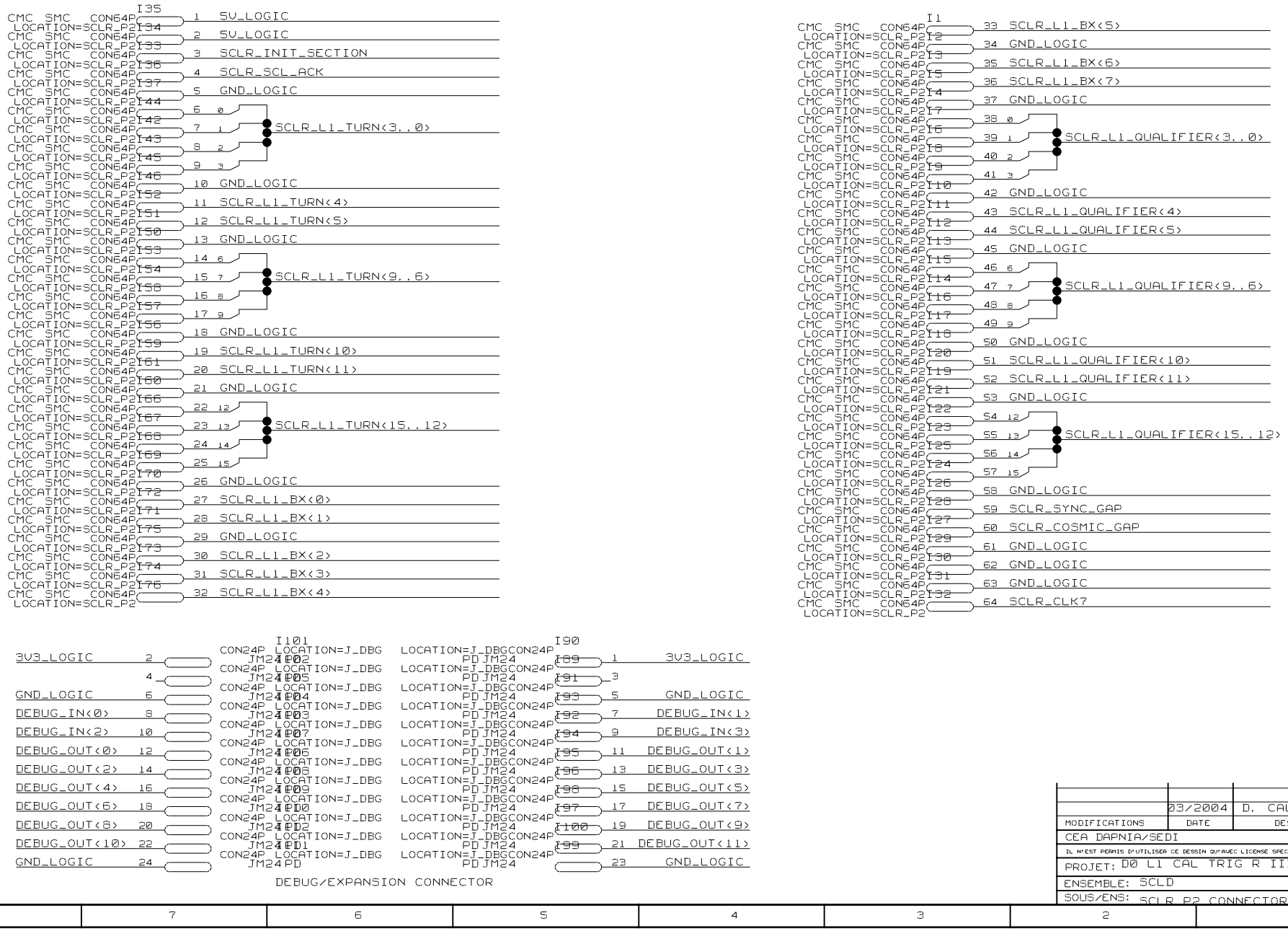
	03/2004	D. CALVET
MODIFICATIONS	DATE	DESSINE PAR

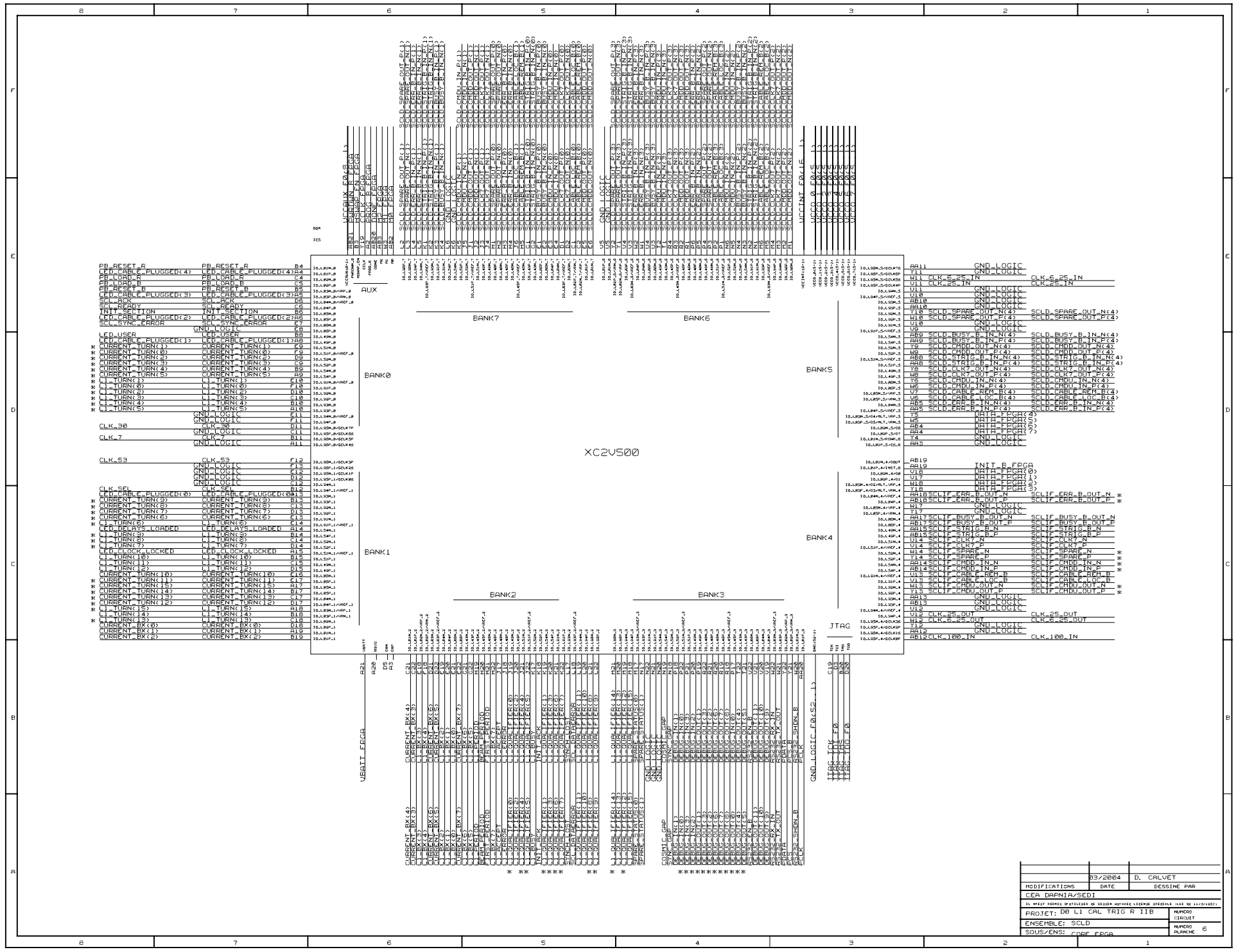
CEA DAPNIA/SEDI

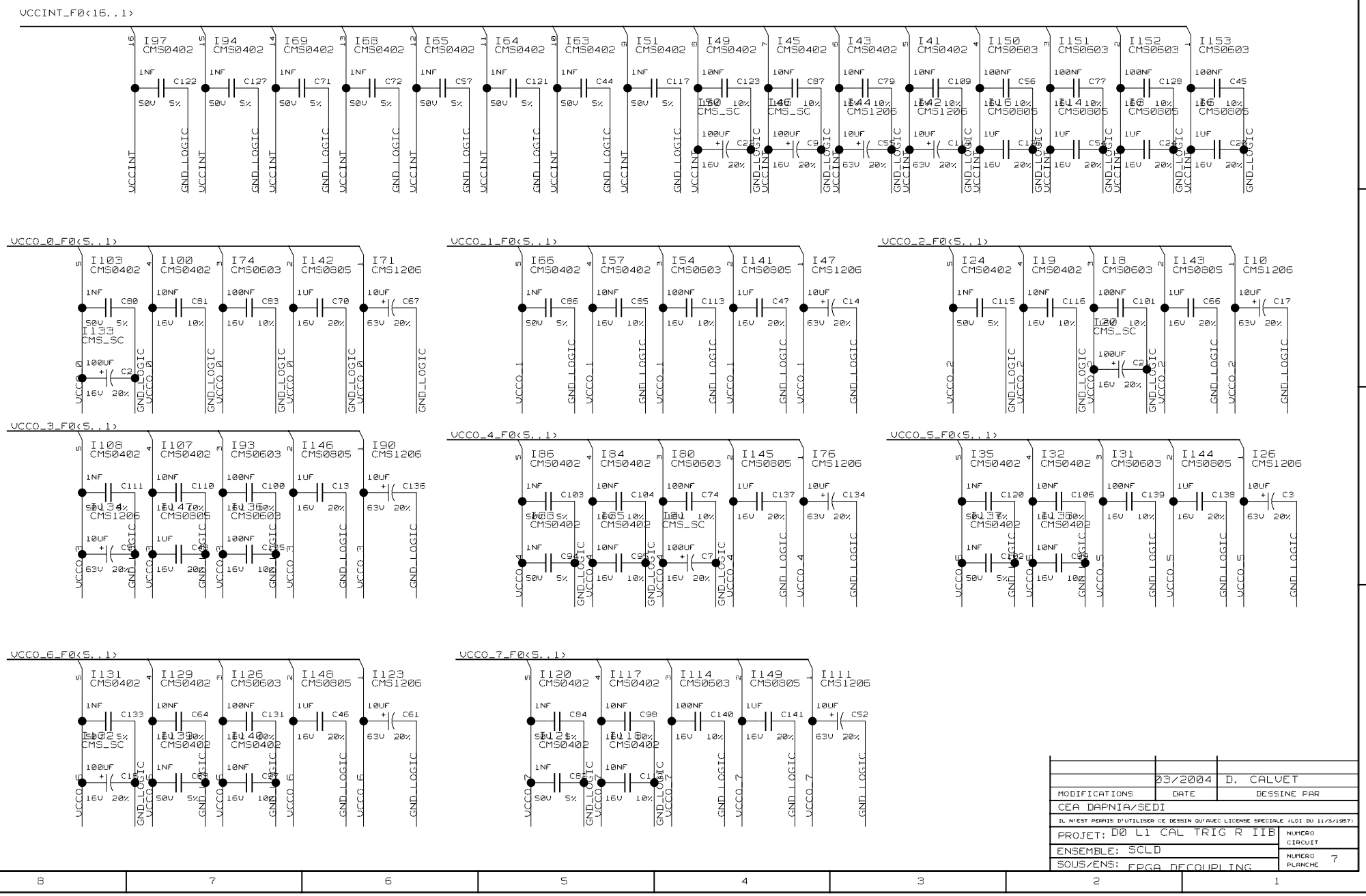
PROJET: D0 L1 CAL TRIG R IIB — NUMERO CIRCUIT

ENSEMBLE: SCLD

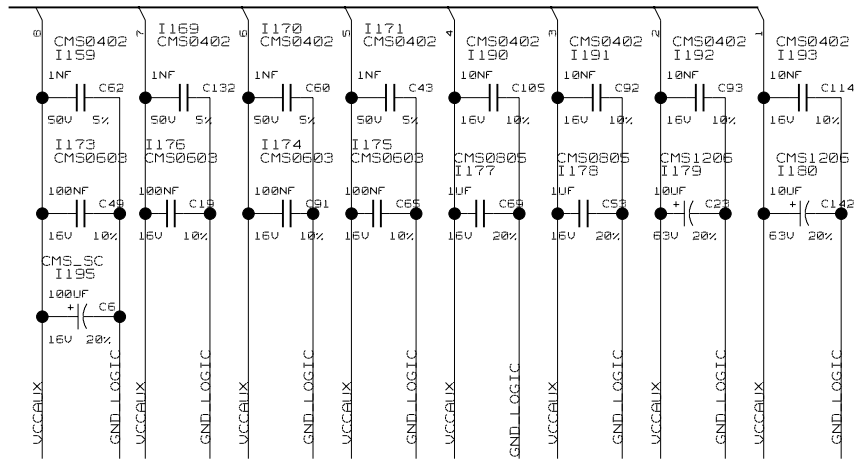
SOUS/ENS: SCLR P1 CONNECTOR — NUMERO PLANCHE 4


I35
CMC SMC CON64P LOCATION=SCLR_P2 I34 1 SV_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I33 2 SV_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I36 3 SCLR_INIT_SECTION
CMC SMC CON64P LOCATION=SCLR_P2 I37 4 SCLR_SCL_ACK
CMC SMC CON64P LOCATION=SCLR_P2 I44 5 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I42 6 0
CMC SMC CON64P LOCATION=SCLR_P2 I43 7 1
CMC SMC CON64P LOCATION=SCLR_P2 I45 8 2
CMC SMC CON64P LOCATION=SCLR_P2 I46 9 3
SCLR_L1_TURN<3..0>
CMC SMC CON64P LOCATION=SCLR_P2 I52 10 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I51 11 SCLR_L1_TURN<4>
CMC SMC CON64P LOCATION=SCLR_P2 I50 12 SCLR_L1_TURN<5>
CMC SMC CON64P LOCATION=SCLR_P2 I53 13 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I54 14 6
CMC SMC CON64P LOCATION=SCLR_P2 I58 15 7
CMC SMC CON64P LOCATION=SCLR_P2 I57 16 8
CMC SMC CON64P LOCATION=SCLR_P2 I56 17 9
SCLR_L1_TURN<9..6>
CMC SMC CON64P LOCATION=SCLR_P2 I59 18 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I61 19 SCLR_L1_TURN<10>
CMC SMC CON64P LOCATION=SCLR_P2 I60 20 SCLR_L1_TURN<11>
CMC SMC CON64P LOCATION=SCLR_P2 I66 21 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I67 22 12
CMC SMC CON64P LOCATION=SCLR_P2 I68 23 13
CMC SMC CON64P LOCATION=SCLR_P2 I69 24 14
CMC SMC CON64P LOCATION=SCLR_P2 I70 25 15
SCLR_L1_TURN<15..12>
CMC SMC CON64P LOCATION=SCLR_P2 I72 26 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I71 27 SCLR_L1_BX<0>
CMC SMC CON64P LOCATION=SCLR_P2 I75 28 SCLR_L1_BX<1>
CMC SMC CON64P LOCATION=SCLR_P2 I73 29 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I74 30 SCLR_L1_BX<2>
CMC SMC CON64P LOCATION=SCLR_P2 I76 31 SCLR_L1_BX<3>
CMC SMC CON64P LOCATION=SCLR_P2 32 SCLR_L1_BX<4>
I1
CMC SMC CON64P LOCATION=SCLR_P2 I2 33 SCLR_L1_BX<5>
CMC SMC CON64P LOCATION=SCLR_P2 I3 34 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I5 35 SCLR_L1_BX<6>
CMC SMC CON64P LOCATION=SCLR_P2 I4 36 SCLR_L1_BX<7>
CMC SMC CON64P LOCATION=SCLR_P2 I7 37 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I6 38 0
CMC SMC CON64P LOCATION=SCLR_P2 I8 39 1
CMC SMC CON64P LOCATION=SCLR_P2 I9 40 2
CMC SMC CON64P LOCATION=SCLR_P2 I10 41 3
SCLR_L1_QUALIFIER<3..0>
CMC SMC CON64P LOCATION=SCLR_P2 I11 42 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I12 43 SCLR_L1_QUALIFIER<4>
CMC SMC CON64P LOCATION=SCLR_P2 I13 44 SCLR_L1_QUALIFIER<5>
CMC SMC CON64P LOCATION=SCLR_P2 I15 45 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I14 46 6
CMC SMC CON64P LOCATION=SCLR_P2 I16 47 7
CMC SMC CON64P LOCATION=SCLR_P2 I17 48 8
CMC SMC CON64P LOCATION=SCLR_P2 I18 49 9
SCLR_L1_QUALIFIER<9..6>
CMC SMC CON64P LOCATION=SCLR_P2 I20 50 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I19 51 SCLR_L1_QUALIFIER<10>
CMC SMC CON64P LOCATION=SCLR_P2 I21 52 SCLR_L1_QUALIFIER<11>
CMC SMC CON64P LOCATION=SCLR_P2 I22 53 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I23 54 12
CMC SMC CON64P LOCATION=SCLR_P2 I25 55 13
CMC SMC CON64P LOCATION=SCLR_P2 I24 56 14
CMC SMC CON64P LOCATION=SCLR_P2 I26 57 15
SCLR_L1_QUALIFIER<15..12>
CMC SMC CON64P LOCATION=SCLR_P2 I28 58 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I27 59 SCLR_SYNC_GAP
CMC SMC CON64P LOCATION=SCLR_P2 I29 60 SCLR_COSMIC_GAP
CMC SMC CON64P LOCATION=SCLR_P2 I30 61 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I31 62 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I32 63 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 64 SCLR_CLK7
3V3_LOGIC 2
4
GND_LOGIC 6
DEBUG_IN<0> 8
DEBUG_IN<2> 10
DEBUG_OUT<0> 12
DEBUG_OUT<2> 14
DEBUG_OUT<4> 16
DEBUG_OUT<6> 18
DEBUG_OUT<8> 20
DEBUG_OUT<10> 22
GND_LOGIC 24
I101
CON24P LOCATION=J_DBG JM24PD 2
CON24P LOCATION=J_DBG JM24PD 5
CON24P LOCATION=J_DBG JM24PD 4
CON24P LOCATION=J_DBG JM24PD 3
CON24P LOCATION=J_DBG JM24PD 7
CON24P LOCATION=J_DBG JM24PD 6
CON24P LOCATION=J_DBG JM24PD 8
CON24P LOCATION=J_DBG JM24PD 9
CON24P LOCATION=J_DBG JM24PD 0
CON24P LOCATION=J_DBG JM24PD 2
CON24P LOCATION=J_DBG JM24PD 1
CON24P LOCATION=J_DBG JM24PD
LOCATION=J_DBGCON24P PDJM24 I89 1 3V3_LOGIC
LOCATION=J_DBGCON24P PDJM24 I91 3
LOCATION=J_DBGCON24P PDJM24 I93 5 GND_LOGIC
LOCATION=J_DBGCON24P PDJM24 I92 7 DEBUG_IN<1>
LOCATION=J_DBGCON24P PDJM24 I94 9 DEBUG_IN<3>
LOCATION=J_DBGCON24P PDJM24 I95 11 DEBUG_OUT<1>
LOCATION=J_DBGCON24P PDJM24 I96 13 DEBUG_OUT<3>
LOCATION=J_DBGCON24P PDJM24 I98 15 DEBUG_OUT<5>
LOCATION=J_DBGCON24P PDJM24 I97 17 DEBUG_OUT<7>
LOCATION=J_DBGCON24P PDJM24 I100 19 DEBUG_OUT<9>
LOCATION=J_DBGCON24P PDJM24 I99 21 DEBUG_OUT<11>
LOCATION=J_DBGCON24P PDJM24 23 GND_LOGIC
I90
DEBUG/EXPANSION CONNECTOR
03/2004
D. CALVET
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: D0 L1 CAL TRIG R IIB
NUMERO CIRCUIT
ENSEMBLE: SCLD
SOUS/ENS: SCLR P2 CONNECTOR
NUMERO PLANCHE
5

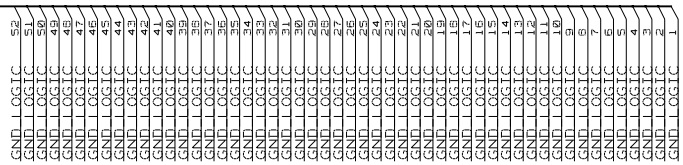

XC2V500
BANK0
BANK1
BANK2
BANK3
BANK4
BANK5
BANK6
BANK7
AUX
JTAG
VBATT_FPGA
GND_LOGIC_FPGA
03/2004
D. CALVET
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
PROJET: D0 L1 CAL TRIG R IIB
ENSEMBLE: SCLD
SOUS/ENS: CORE FPGA
NUMERO CIRCUIT
NUMERO PLANCHE
6


VCCINT_F0<16..1>
I97 CMS0402
I94 CMS0402
I69 CMS0402
I68 CMS0402
I65 CMS0402
I64 CMS0402
I63 CMS0402
I51 CMS0402
I49 CMS0402
I45 CMS0402
I43 CMS0402
I41 CMS0402
I150 CMS0603
I151 CMS0603
I152 CMS0603
I153 CMS0603
C122 C127 C71 C72 C57 C121 C44 C117 C123 C87 C79 C109 C56 C77 C128 C45
1NF 50V 5%
10NF 16V 10%
100NF 16V 10%
C2 C9 C5 C1 C12 C8 C20
100UF 16V 20%
1UF 16V 20%
10UF 63V 20%
GND_LOGIC
VCCINT
VCCO_0_F0<5..1>
I103 CMS0402
I100 CMS0402
I74 CMS0603
I142 CMS0805
I71 CMS1206
C80 C81 C83 C70 C67
I133 CMS_SC
C3
VCCO_0
VCCO_1_F0<5..1>
I66 CMS0402
I57 CMS0402
I54 CMS0603
I141 CMS0805
I47 CMS1206
C86 C85 C113 C47 C14
VCCO_1
VCCO_2_F0<5..1>
I24 CMS0402
I19 CMS0402
I18 CMS0603
I143 CMS0805
I10 CMS1206
C115 C116 C101 C66 C17
I120 CMS_SC
C6
VCCO_2
VCCO_3_F0<5..1>
I108 CMS0402
I107 CMS0402
I93 CMS0603
I146 CMS0805
I90 CMS1206
C111 C110 C100 C13 C136
I134 CMS1206
I147 CMS0805
I136 CMS0603
C4
VCCO_3
VCCO_4_F0<5..1>
I86 CMS0402
I84 CMS0402
I80 CMS0603
I145 CMS0805
I76 CMS1206
C103 C104 C74 C137 C134
I135 CMS0402
I65 CMS0402
I122 CMS_SC
C7
VCCO_4
VCCO_5_F0<5..1>
I35 CMS0402
I32 CMS0402
I31 CMS0603
I144 CMS0805
I26 CMS1206
C120 C106 C139 C138 C3
I37 CMS0402
I36 CMS0402
C2
VCCO_5
VCCO_6_F0<5..1>
I131 CMS0402
I129 CMS0402
I126 CMS0603
I148 CMS0805
I123 CMS1206
C133 C64 C131 C46 C61
I132 CMS_SC
I39 CMS0402
I40 CMS0402
C10
VCCO_6
VCCO_7_F0<5..1>
I120 CMS0402
I117 CMS0402
I114 CMS0603
I149 CMS0805
I111 CMS1206
C84 C98 C140 C141 C52
I25 CMS0402
I16 CMS0402
C8
VCCO_7
03/2004
D. CALVET
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: D0 L1 CAL TRIG R IIB
NUMERO CIRCUIT
ENSEMBLE: SCLD
SOUS/ENS: FPGA DECOUPLING
NUMERO PLANCHE
7

VCCAUX_F0<8..1>



GND_LOGIC_F0<52..1>

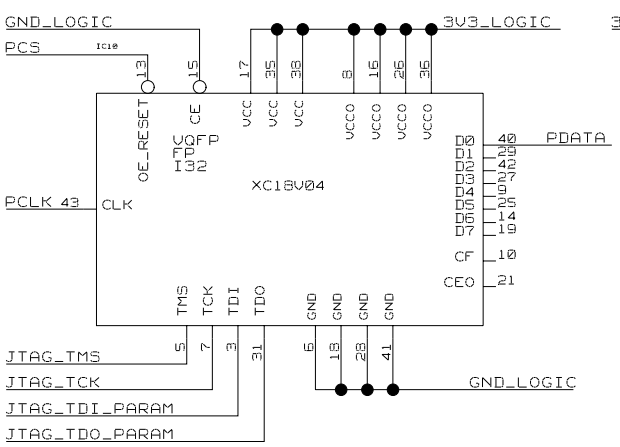


HSWAP_EN_FPGA — ALIAS — GND_LOGIC

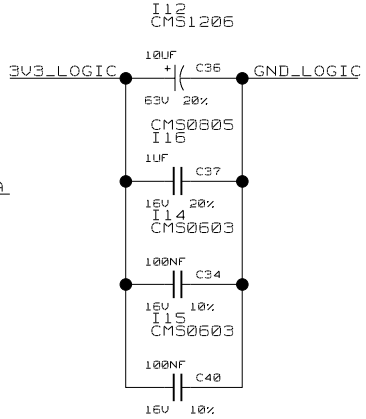
I/OS PULLUP ON FPGA CONFIGURATION

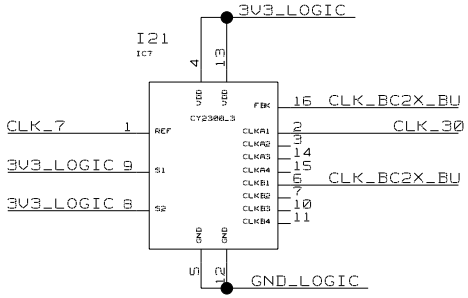
PWRDWN_B_FPGA	ALIAS	3V3_LOGIC
VBATT_FPGA	ALIAS	3V3_LOGIC
VCCO_0	ALIAS	3V3_LOGIC
VCCO_1	ALIAS	3V3_LOGIC
VCCO_2	ALIAS	3V3_LOGIC
VCCO_3	ALIAS	3V3_LOGIC
VCCO_4	ALIAS	3V3_LOGIC
VCCO_5	ALIAS	3V3_LOGIC
VCCO_6	ALIAS	3V3_LOGIC
VCCO_7	ALIAS	3V3_LOGIC
VCCAUX	ALIAS	3V3_LOGIC

	03/2004	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: SCLD		
SOUS/ENS: FPGA DECOUPLING & GND		NUMERO PLANCHE 8

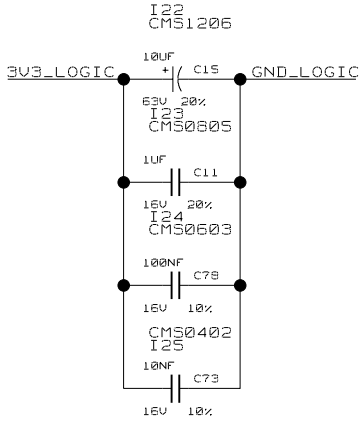


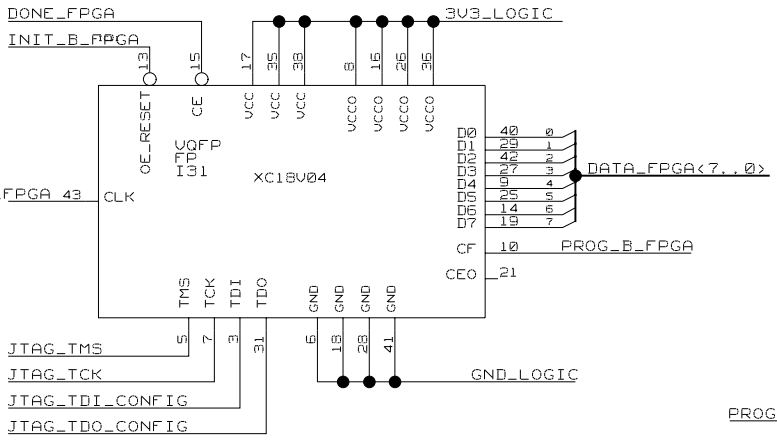
USER PARAMETER SERIAL PROM



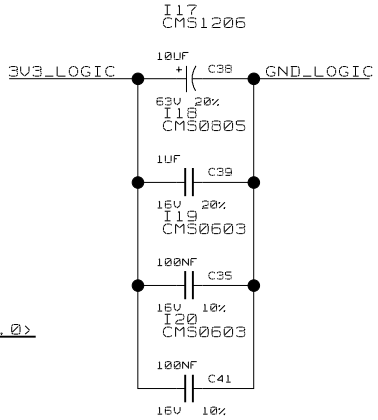


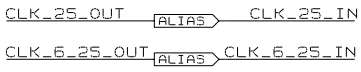
PLL FOR BC CLOCK MULTIPLICATION



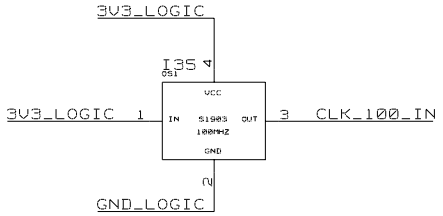


FPGA CONFIGURATION SERIAL PROM

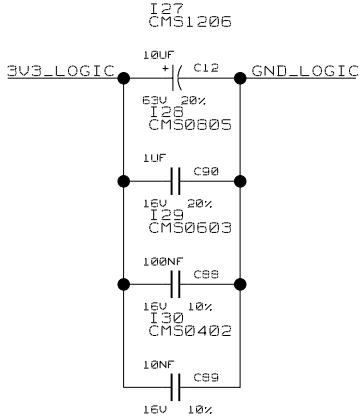


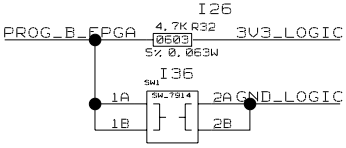


LOCAL CLOCK CONNECTIONS



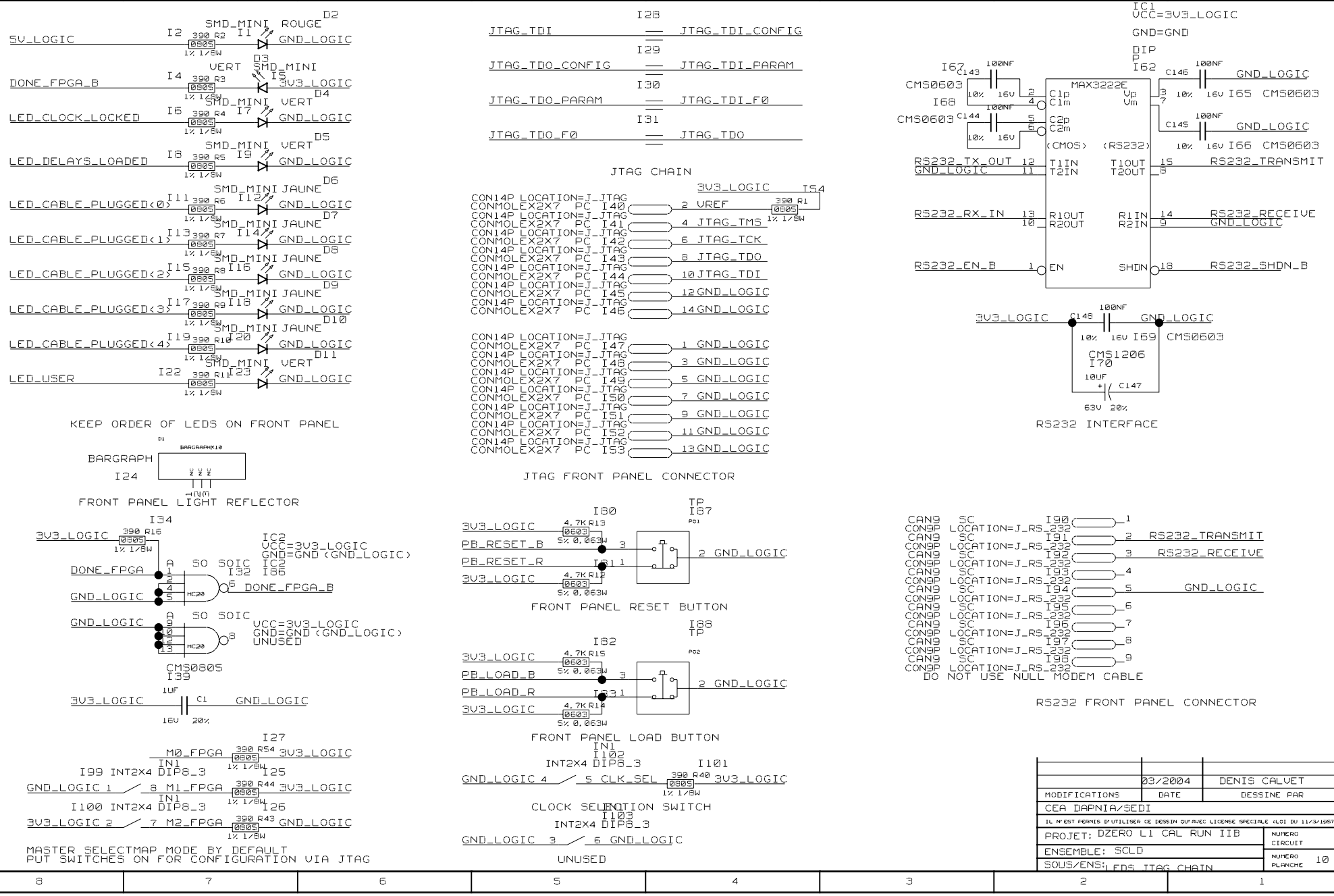
ON BOARD OSCILLATOR





FPGA CONFIGURATION PUSH BUTTON

	03/2004	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: DZERO L1 CAL RUN IIB		NUMERO CIRCUIT
ENSEMBLE: SCLD		
SOUS/ENS: ITAG PROMS		NUMERO PLANCHE 9


D2
SMD_MINI ROUGE
5V_LOGIC
I2 390 R2 I1
GND_LOGIC
D3
VERT SMD_MINI
DONE_FPGA_B
I4 390 R3 I5
3V3_LOGIC
D4
SMD_MINI VERT
LED_CLOCK_LOCKED
I6 390 R4 I7
GND_LOGIC
D5
SMD_MINI VERT
LED_DELAYS_LOADED
I8 390 R5 I9
GND_LOGIC
D6
SMD_MINI JAUNE
LED_CABLE_PLUGGED<0>
I11 390 R6 I12
GND_LOGIC
D7
SMD_MINI JAUNE
LED_CABLE_PLUGGED<1>
I13 390 R7 I14
GND_LOGIC
D8
SMD_MINI JAUNE
LED_CABLE_PLUGGED<2>
I15 390 R8 I16
GND_LOGIC
D9
SMD_MINI JAUNE
LED_CABLE_PLUGGED<3>
I17 390 R9 I18
GND_LOGIC
D10
SMD_MINI JAUNE
LED_CABLE_PLUGGED<4>
I19 390 R10 I20
GND_LOGIC
D11
SMD_MINI VERT
LED_USER
I22 390 R11 I23
GND_LOGIC
0805
1% 1/8W
KEEP ORDER OF LEDS ON FRONT PANEL
D1
BARGRAPHX10
BARGRAPH
I24
FRONT PANEL LIGHT REFLECTOR
I34
3V3_LOGIC
390 R16
DONE_FPGA
GND_LOGIC
A SO SOIC
I32
HC20
IC2
VCC=3V3_LOGIC
GND=GND (GND_LOGIC)
IC2
I86
5 DONE_FPGA_B
GND_LOGIC
SO SOIC
VCC=3V3_LOGIC
GND=GND (GND_LOGIC)
UNUSED
CMS0805
I39
1UF
3V3_LOGIC
C1
GND_LOGIC
16V 20%
I27
M0_FPGA
390 R54
3V3_LOGIC
IN1
I99 INT2X4 DIP8_3
I25
GND_LOGIC 1
8 M1_FPGA
390 R44
3V3_LOGIC
I100 INT2X4 DIP8_3
I26
3V3_LOGIC 2
7 M2_FPGA
390 R43
GND_LOGIC
MASTER SELECTMAP MODE BY DEFAULT
PUT SWITCHES ON FOR CONFIGURATION VIA JTAG
I28
JTAG_TDI
JTAG_TDI_CONFIG
I29
JTAG_TDO_CONFIG
JTAG_TDI_PARAM
I30
JTAG_TDO_PARAM
JTAG_TDI_F0
I31
JTAG_TDO_F0
JTAG_TDO
JTAG CHAIN
3V3_LOGIC
IS4
390 R1
CON14P LOCATION=J_JTAG
CONMOLEX2X7 PC I40
2 VREF
CONMOLEX2X7 PC I41
4 JTAG_TMS
CONMOLEX2X7 PC I42
6 JTAG_TCK
CONMOLEX2X7 PC I43
8 JTAG_TDO
CONMOLEX2X7 PC I44
10 JTAG_TDI
CONMOLEX2X7 PC I45
12 GND_LOGIC
CONMOLEX2X7 PC I46
14 GND_LOGIC
CONMOLEX2X7 PC I47
1 GND_LOGIC
CONMOLEX2X7 PC I48
3 GND_LOGIC
CONMOLEX2X7 PC I49
5 GND_LOGIC
CONMOLEX2X7 PC I50
7 GND_LOGIC
CONMOLEX2X7 PC I51
9 GND_LOGIC
CONMOLEX2X7 PC I52
11 GND_LOGIC
CONMOLEX2X7 PC I53
13 GND_LOGIC
JTAG FRONT PANEL CONNECTOR
I80
TP
I87
P01
3V3_LOGIC
4.7K R13
0603
5% 0.063W
PB_RESET_B
3
PB_RESET_R
I81
1
2 GND_LOGIC
3V3_LOGIC
4.7K R12
FRONT PANEL RESET BUTTON
I88
TP
I82
P02
3V3_LOGIC
4.7K R15
PB_LOAD_B
3
PB_LOAD_R
I83
1
2 GND_LOGIC
3V3_LOGIC
4.7K R14
FRONT PANEL LOAD BUTTON
IN1
I102
INT2X4 DIP8_3
I101
GND_LOGIC 4
5 CLK_SEL
390 R40
3V3_LOGIC
0805
1% 1/8W
CLOCK SELECTION SWITCH
I103
INT2X4 DIP8_3
GND_LOGIC 3
6 GND_LOGIC
UNUSED
IC1
VCC=3V3_LOGIC
GND=GND
DIP
P
I62
I67
C143 100NF
CMS0603
10% 16V
I68
C144 100NF
CMS0603
10% 16V
MAX3222E
C1p
C1m
C2p
C2m
(CMOS)
Vp
Vm
(RS232)
C146 100NF
GND_LOGIC
10% 16V I65 CMS0603
C145 100NF
GND_LOGIC
10% 16V I66 CMS0603
RS232_TX_OUT 12
GND_LOGIC 11
T1IN
T2IN
T1OUT 15
T2OUT 8
RS232_TRANSMIT
RS232_RX_IN 13
10
R1OUT
R2OUT
R1IN 14
R2IN 9
RS232_RECEIVE
GND_LOGIC
RS232_EN_B 1
EN
SHDN 18
RS232_SHDN_B
3V3_LOGIC
C148 100NF
GND_LOGIC
10% 16V I69 CMS0603
CMS1206
I70
10UF
C147
63V 20%
RS232 INTERFACE
CAN9 SC I90 1
CON9P LOCATION=J_RS_232
CAN9 SC I91 2 RS232_TRANSMIT
CON9P LOCATION=J_RS_232
CAN9 SC I92 3 RS232_RECEIVE
CON9P LOCATION=J_RS_232
CAN9 SC I93 4
CON9P LOCATION=J_RS_232
CAN9 SC I94 5 GND_LOGIC
CON9P LOCATION=J_RS_232
CAN9 SC I95 6
CON9P LOCATION=J_RS_232
CAN9 SC I96 7
CON9P LOCATION=J_RS_232
CAN9 SC I97 8
CON9P LOCATION=J_RS_232
CAN9 SC I98 9
CON9P LOCATION=J_RS_232
DO NOT USE NULL MODEM CABLE
RS232 FRONT PANEL CONNECTOR
03/2004
DENIS CALVET
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN SUR AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: DZERO L1 CAL RUN IIB
NUMERO CIRCUIT
ENSEMBLE: SCLD
SOUS/ENS: LFDS JTAG CHAIN
NUMERO PLANCHE 10


CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I1 A1 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I2 A2 SCLD_CLK7_OUT_N<0>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I3 A3 SCLD_CMDU_IN_N<0>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I4 A4 SCLD_STRIG_B_IN_N<0>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I5 A5 SCLD_SPARE_OUT_N<0>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I6 A6 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I7 A7 SCLD_CLK7_OUT_N<1>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I8 A8 SCLD_CMDU_IN_N<1>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I9 A9 SCLD_STRIG_B_IN_N<1>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I10 A10 SCLD_SPARE_OUT_N<1>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I11 A11 GND_LOGIC
I14
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I13 B1 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I12 B2 SCLD_CLK7_OUT_P<0>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I16 B3 SCLD_CMDU_IN_P<0>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I15 B4 SCLD_STRIG_B_IN_P<0>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I19 B5 SCLD_SPARE_OUT_P<0>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I18 B6 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I17 B7 SCLD_CLK7_OUT_P<1>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I20 B8 SCLD_CMDU_IN_P<1>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I21 B9 SCLD_STRIG_B_IN_P<1>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I22 B10 SCLD_SPARE_OUT_P<1>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC B11 GND_LOGIC
I24
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I23 C1 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I25 C2 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I27 C3 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I26 C4 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I28 C5 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I30 C6 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I29 C7 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I31 C8 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I32 C9 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I33 C10 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC C11 GND_LOGIC
I42
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I44 D1 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I43 D2 SCLD_CABLE_REM_B<0>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I46 D3 SCLD_CMDD_OUT_N<0>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I47 D4 SCLD_BUSY_B_IN_N<0>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I45 D5 SCLD_ERR_B_IN_N<0>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I48 D6 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I49 D7 SCLD_CABLE_REM_B<1>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I54 D8 SCLD_CMDD_OUT_N<1>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I55 D9 SCLD_BUSY_B_IN_N<1>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I53 D10 SCLD_ERR_B_IN_N<1>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC D11 GND_LOGIC
I56
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I57 E1 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I58 E2 SCLD_CABLE_LOC_B<0>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I59 E3 SCLD_CMDD_OUT_P<0>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I60 E4 SCLD_BUSY_B_IN_P<0>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I61 E5 SCLD_ERR_B_IN_P<0>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I62 E6 GND_LOGIC
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I63 E7 SCLD_CABLE_LOC_B<1>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I64 E8 SCLD_CMDD_OUT_P<1>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I65 E9 SCLD_BUSY_B_IN_P<1>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC I66 E10 SCLD_ERR_B_IN_P<1>
CONN5P LOCATION=ADF_0_1
ZPACK5X11C PC E11 GND_LOGIC
TIE ROW F TO GND_LOGIC
I122
I123 GND_LOGIC
I86
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I88 A1 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I87 A2 SCLD_CLK7_OUT_N<2>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I90 A3 SCLD_CMDU_IN_N<2>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I91 A4 SCLD_STRIG_B_IN_N<2>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I89 A5 SCLD_SPARE_OUT_N<2>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I92 A6 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I93 A7 SCLD_CLK7_OUT_N<3>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I108 A8 SCLD_CMDU_IN_N<3>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I109 A9 SCLD_STRIG_B_IN_N<3>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I110 A10 SCLD_SPARE_OUT_N<3>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC A11 GND_LOGIC
I78
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I79 B1 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I80 B2 SCLD_CLK7_OUT_P<2>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I82 B3 SCLD_CMDU_IN_P<2>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I81 B4 SCLD_STRIG_B_IN_P<2>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I83 B5 SCLD_SPARE_OUT_P<2>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I85 B6 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I84 B7 SCLD_CLK7_OUT_P<3>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I96 B8 SCLD_CMDU_IN_P<3>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I95 B9 SCLD_STRIG_B_IN_P<3>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I94 B10 SCLD_SPARE_OUT_P<3>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC B11 GND_LOGIC
I68
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I67 C1 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I69 C2 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I71 C3 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I70 C4 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I72 C5 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I74 C6 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I73 C7 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I75 C8 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I76 C9 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I77 C10 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC C11 GND_LOGIC
I111
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I112 D1 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I113 D2 SCLD_CABLE_REM_B<2>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I114 D3 SCLD_CMDD_OUT_N<2>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I115 D4 SCLD_BUSY_B_IN_N<2>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I116 D5 SCLD_ERR_B_IN_N<2>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I117 D6 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I118 D7 SCLD_CABLE_REM_B<3>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I119 D8 SCLD_CMDD_OUT_N<3>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I120 D9 SCLD_BUSY_B_IN_N<3>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I121 D10 SCLD_ERR_B_IN_N<3>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC D11 GND_LOGIC
I97
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I98 E1 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I99 E2 SCLD_CABLE_LOC_B<2>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I100 E3 SCLD_CMDD_OUT_P<2>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I101 E4 SCLD_BUSY_B_IN_P<2>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I102 E5 SCLD_ERR_B_IN_P<2>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I103 E6 GND_LOGIC
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I104 E7 SCLD_CABLE_LOC_B<3>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I105 E8 SCLD_CMDD_OUT_P<3>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I106 E9 SCLD_BUSY_B_IN_P<3>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC I107 E10 SCLD_ERR_B_IN_P<3>
CONN5P LOCATION=ADF_2_3
ZPACK5X11C PC E11 GND_LOGIC
TIE ROW F TO GND_LOGIC
03/2004 D. CALVET
MODIFICATIONS DATE DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: D0 L1 CAL TRIG R IIB
NUMERO CIRCUIT
ENSEMBLE: SCLD
SOUS/ENS: SCLD <-> ADF 0 3
NUMERO PLANCHE 11


I31
CON55P LOCATION=ADF_4_LL
ZPACK5X11C PC
I32 A1 GND_LOGIC
I33 A2 SCLD_CLK7_OUT_N<4>
I34 A3 SCLD_CMDU_IN_N<4>
I35 A4 SCLD_STRIG_B_IN_N<4>
I36 A5 SCLD_SPARE_OUT_N<4>
I38 A6 GND_LOGIC
I37 A7 SCLIF_CLK7_N
I77 A8 SCLIF_CMDU_OUT_N
I75 A9 SCLIF_STRIG_B_N
I76 A10 SCLIF_SPARE_N
A11 GND_LOGIC
I23
I24 B1 GND_LOGIC
I25 B2 SCLD_CLK7_OUT_P<4>
I27 B3 SCLD_CMDU_IN_P<4>
I28 B4 SCLD_STRIG_B_IN_P<4>
I26 B5 SCLD_SPARE_OUT_P<4>
I29 B6 GND_LOGIC
I30 B7 SCLIF_CLK7_P
I39 B8 SCLIF_CMDU_OUT_P
I41 B9 SCLIF_STRIG_B_P
I40 B10 SCLIF_SPARE_P
B11 GND_LOGIC
I2
I1 C1 GND_LOGIC
I3 C2 GND_LOGIC
I5 C3 GND_LOGIC
I4 C4 GND_LOGIC
I6 C5 GND_LOGIC
I8 C6 GND_LOGIC
I7 C7 GND_LOGIC
I9 C8 GND_LOGIC
I10 C9 GND_LOGIC
I11 C10 GND_LOGIC
C11 GND_LOGIC
I78
I80 D1 GND_LOGIC
I79 D2 SCLD_CABLE_REM_B<4>
I81 D3 SCLD_CMDD_OUT_N<4>
I82 D4 SCLD_BUSY_B_IN_N<4>
I83 D5 SCLD_ERR_B_IN_N<4>
I84 D6 GND_LOGIC
I85 D7 SCLIF_CABLE_LOC_B
I86 D8 SCLIF_CMDD_IN_N
I88 D9 SCLIF_BUSY_B_OUT_N
I87 D10 SCLIF_ERR_B_OUT_N
D11 GND_LOGIC
I42
I44 E1 GND_LOGIC
I43 E2 SCLD_CABLE_LOC_B<4>
I45 E3 SCLD_CMDD_OUT_P<4>
I47 E4 SCLD_BUSY_B_IN_P<4>
I46 E5 SCLD_ERR_B_IN_P<4>
I48 E6 GND_LOGIC
I50 E7 SCLIF_CABLE_REM_B
I49 E8 SCLIF_CMDD_IN_P
I52 E9 SCLIF_BUSY_B_OUT_P
I51 E10 SCLIF_ERR_B_OUT_P
E11 GND_LOGIC
TIE ROW F TO GND_LOGIC
I90
SCLD_CMDU_IN_N<0> R45 100 0603 5% 0.063W SCLD_CMDU_IN_P<0>
SCLD_STRIG_B_IN_N<0> R20 100 0603 5% 0.063W SCLD_STRIG_B_IN_P<0>
SCLD_BUSY_B_IN_N<0> R19 100 0603 5% 0.063W SCLD_BUSY_B_IN_P<0>
SCLD_ERR_B_IN_N<0> R21 100 0603 5% 0.063W SCLD_ERR_B_IN_P<0>
3V3_LOGIC R18 4.7K 0603 5% 0.063W SCLD_CABLE_REM_B<0>
I99
SCLD_CMDU_IN_N<2> R24 100 0603 5% 0.063W SCLD_CMDU_IN_P<2>
SCLD_STRIG_B_IN_N<2> R25 100 0603 5% 0.063W SCLD_STRIG_B_IN_P<2>
SCLD_BUSY_B_IN_N<2> R50 100 0603 5% 0.063W SCLD_BUSY_B_IN_P<2>
SCLD_ERR_B_IN_N<2> R51 100 0603 5% 0.063W SCLD_ERR_B_IN_P<2>
3V3_LOGIC R49 4.7K 0603 5% 0.063W SCLD_CABLE_REM_B<2>
I109
SCLD_CMDU_IN_N<4> R29 100 0603 5% 0.063W SCLD_CMDU_IN_P<4>
SCLD_STRIG_B_IN_N<4> R42 100 0603 5% 0.063W SCLD_STRIG_B_IN_P<4>
SCLD_BUSY_B_IN_N<4> R41 100 0603 5% 0.063W SCLD_BUSY_B_IN_P<4>
SCLD_ERR_B_IN_N<4> R30 100 0603 5% 0.063W SCLD_ERR_B_IN_P<4>
3V3_LOGIC R28 4.7K 0603 5% 0.063W SCLD_CABLE_REM_B<4>
I94
SCLD_CMDU_IN_N<1> R47 100 0603 5% 0.063W SCLD_CMDU_IN_P<1>
SCLD_STRIG_B_IN_N<1> R22 100 0603 5% 0.063W SCLD_STRIG_B_IN_P<1>
SCLD_BUSY_B_IN_N<1> R48 100 0603 5% 0.063W SCLD_BUSY_B_IN_P<1>
SCLD_ERR_B_IN_N<1> R23 100 0603 5% 0.063W SCLD_ERR_B_IN_P<1>
3V3_LOGIC R46 4.7K 0603 5% 0.063W SCLD_CABLE_REM_B<1>
I104
SCLD_CMDU_IN_N<3> R52 100 0603 5% 0.063W SCLD_CMDU_IN_P<3>
SCLD_STRIG_B_IN_N<3> R53 100 0603 5% 0.063W SCLD_STRIG_B_IN_P<3>
SCLD_BUSY_B_IN_N<3> R26 100 0603 5% 0.063W SCLD_BUSY_B_IN_P<3>
SCLD_ERR_B_IN_N<3> R27 100 0603 5% 0.063W SCLD_ERR_B_IN_P<3>
3V3_LOGIC R17 4.7K 0603 5% 0.063W SCLD_CABLE_REM_B<3>
I114
SCLIF_CLK7_N R39 100 0603 5% 0.063W SCLIF_CLK7_P
SCLIF_SPARE_N R37 100 0603 5% 0.063W SCLIF_SPARE_P
SCLIF_CMDD_IN_N R38 100 0603 5% 0.063W SCLIF_CMDD_IN_P
3V3_LOGIC R31 4.7K 0603 5% 0.063W SCLIF_CABLE_REM_B
100 OHMS DIFFERENTIAL IMPEDANCE TRACES TO ALL 100 OHMS RESISTORS
PLACE 100 OHMS RESISTORS CLOSEST TO FPGA
MATCH LENGTH OF DIFFERENTIAL PAIRS BETTER THAN 5 MM WITHIN EACH GROUP
MATCH LENGTH OF DIFFERENTIAL PAIRS BETTER THAN 2 CM WITHIN ALL GROUPS
03/2004 D. CALVET
MODIFICATIONS DATE DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: D0 L1 CAL TRIG R IIB
NUMERO CIRCUIT
ENSEMBLE: SCLD
SOUS/ENS: SCLD (-) ADF4 + LB
NUMERO PLANCHE 12