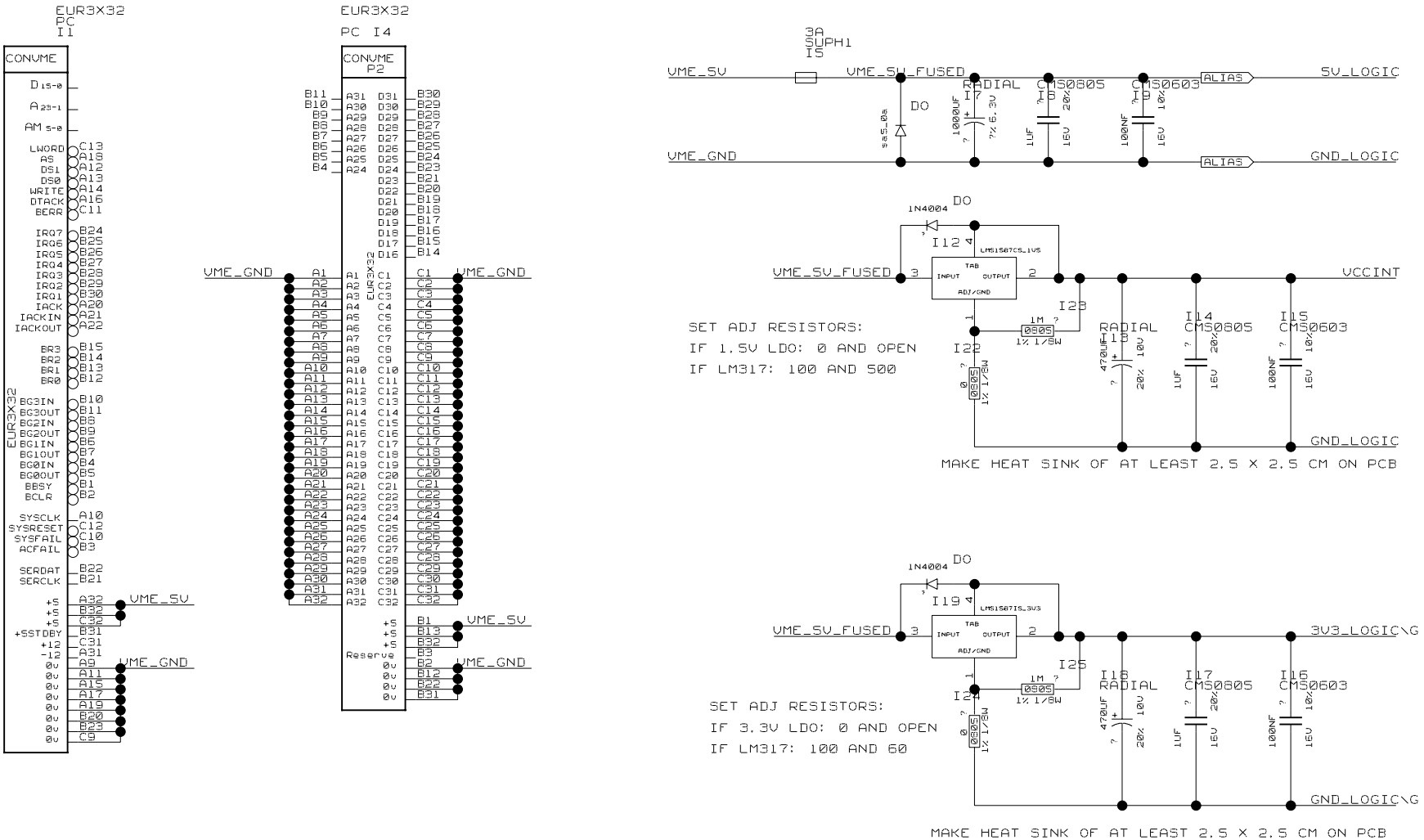


	03/2004	D. CALVET
MODIFICATIONS	DATE	DESSINE PAR

CEA DAPNIA/SEDI

IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)

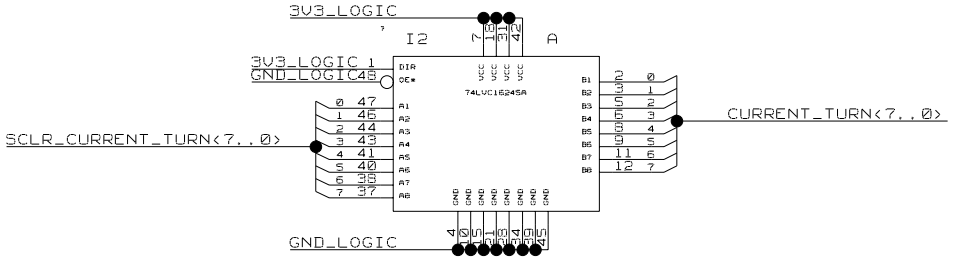
PROJET: D0 L1 CAL TRIG R IIB

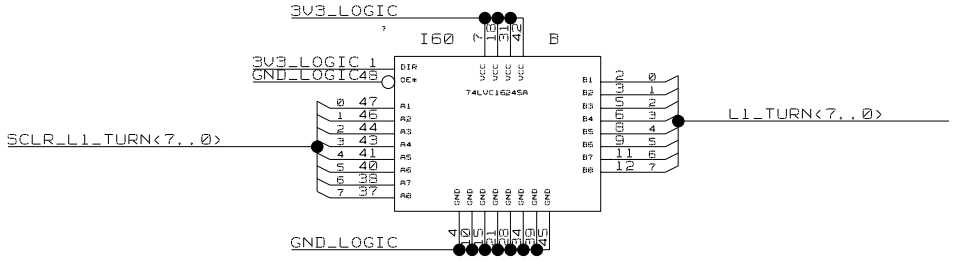
ENSEMBLE: SCLD

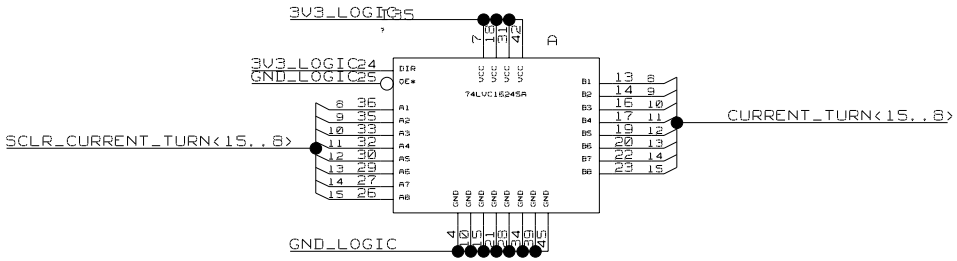
SOUS/ENS: POWER SUPPLIES

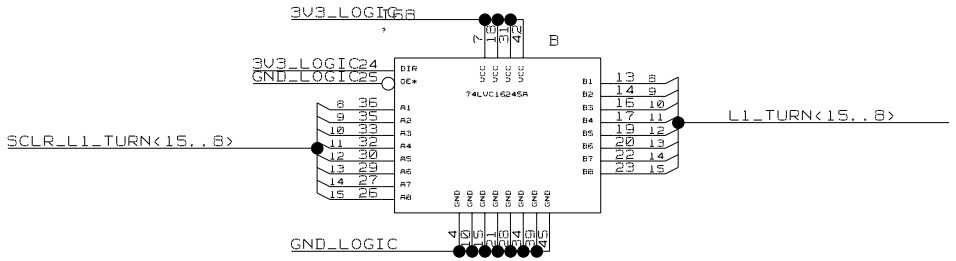
NUMERO CIRCUIT

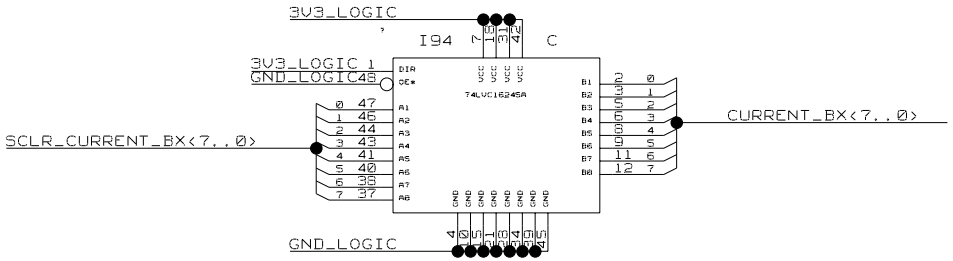
NUMERO PLANCHE 1

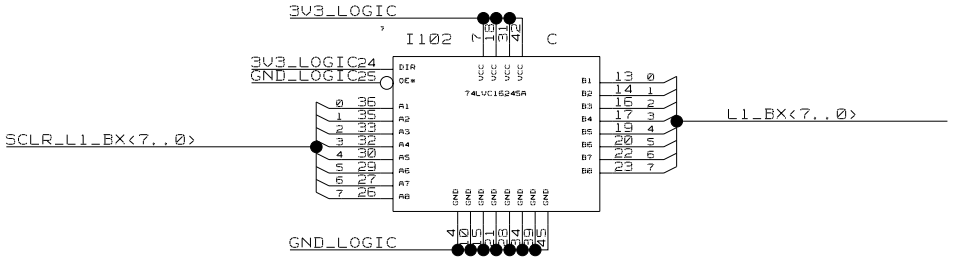


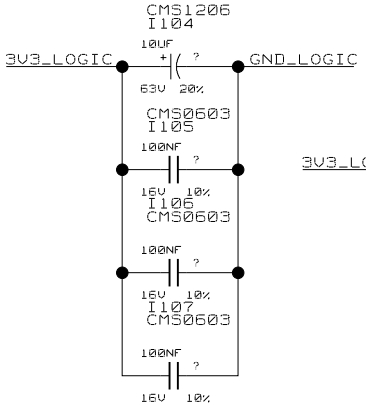


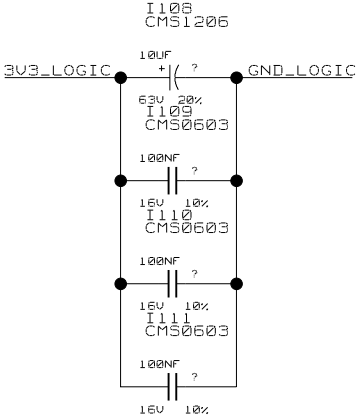


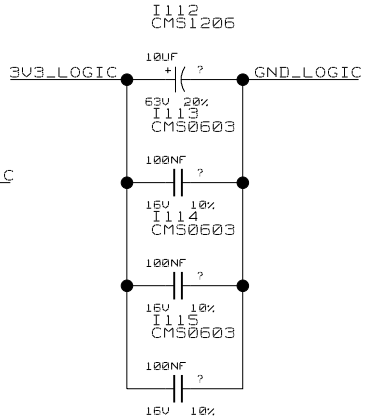












	03/2004	D. CALVET
MODIFICATIONS	DATE	DESSINE PAR

CEA DAPNIA/SEDI

IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)

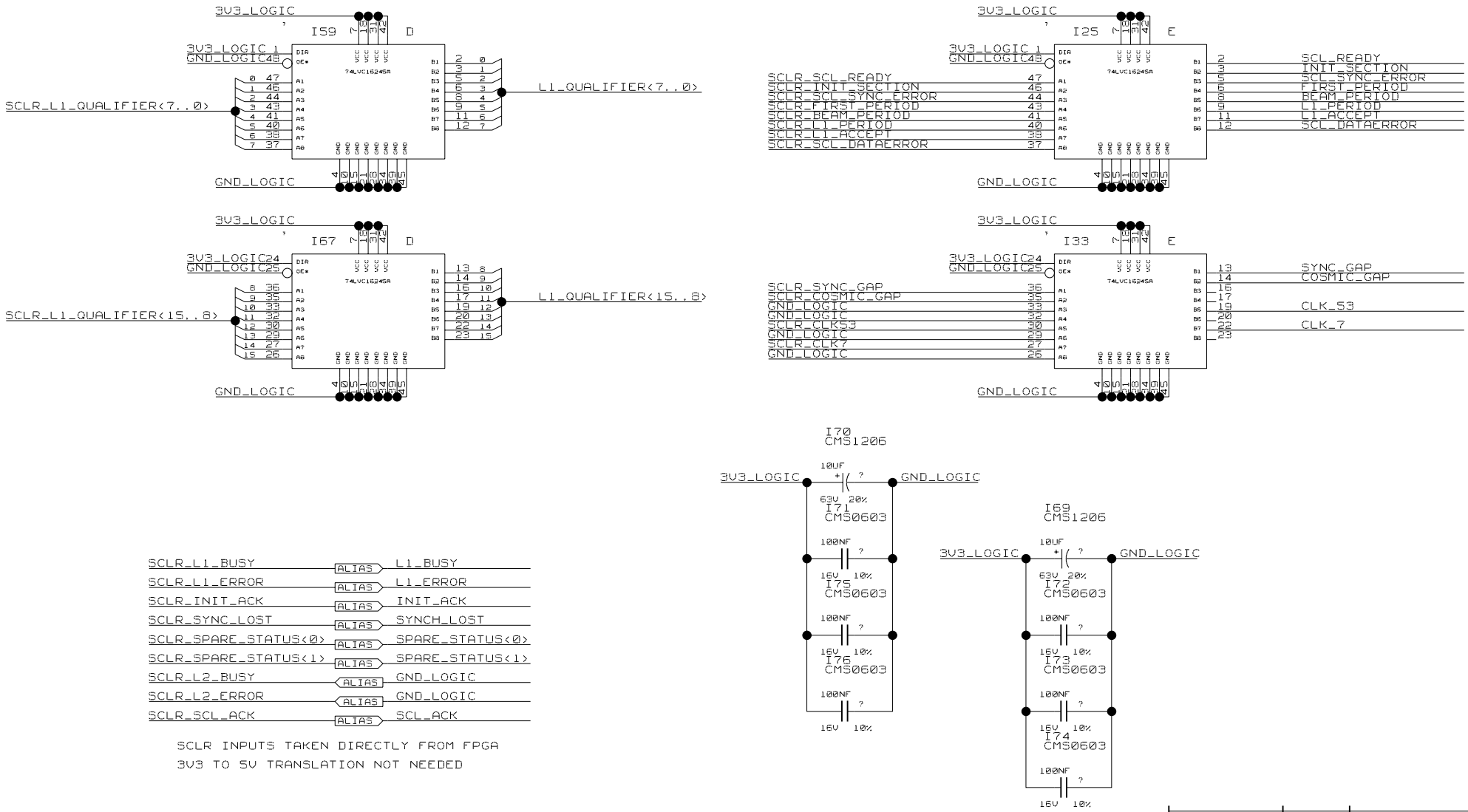
PROJET: D0 L1 CAL TRIG R IIB

ENSEMBLE: SCLD

SOUS/ENS: SCLR TRANSCEIVERS

NUMERO CIRCUIT

NUMERO PLANCHE 2



	03/2004	D. CALVET
MODIFICATIONS	DATE	DESSINE PAR

CEA DAPNIA/SEDI

IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)

PROJET: D0 L1 CAL TRIG R IIB

ENSEMBLE: SCLD

SOUS/ENS: SCLR TRANSCEIVERS

NUMERO CIRCUIT

NUMERO PLANCHE 3

	03/2004	D. CALVET
MODIFICATIONS	DATE	DESSINE PAR

CEA DAPNIA/SEDI

IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)

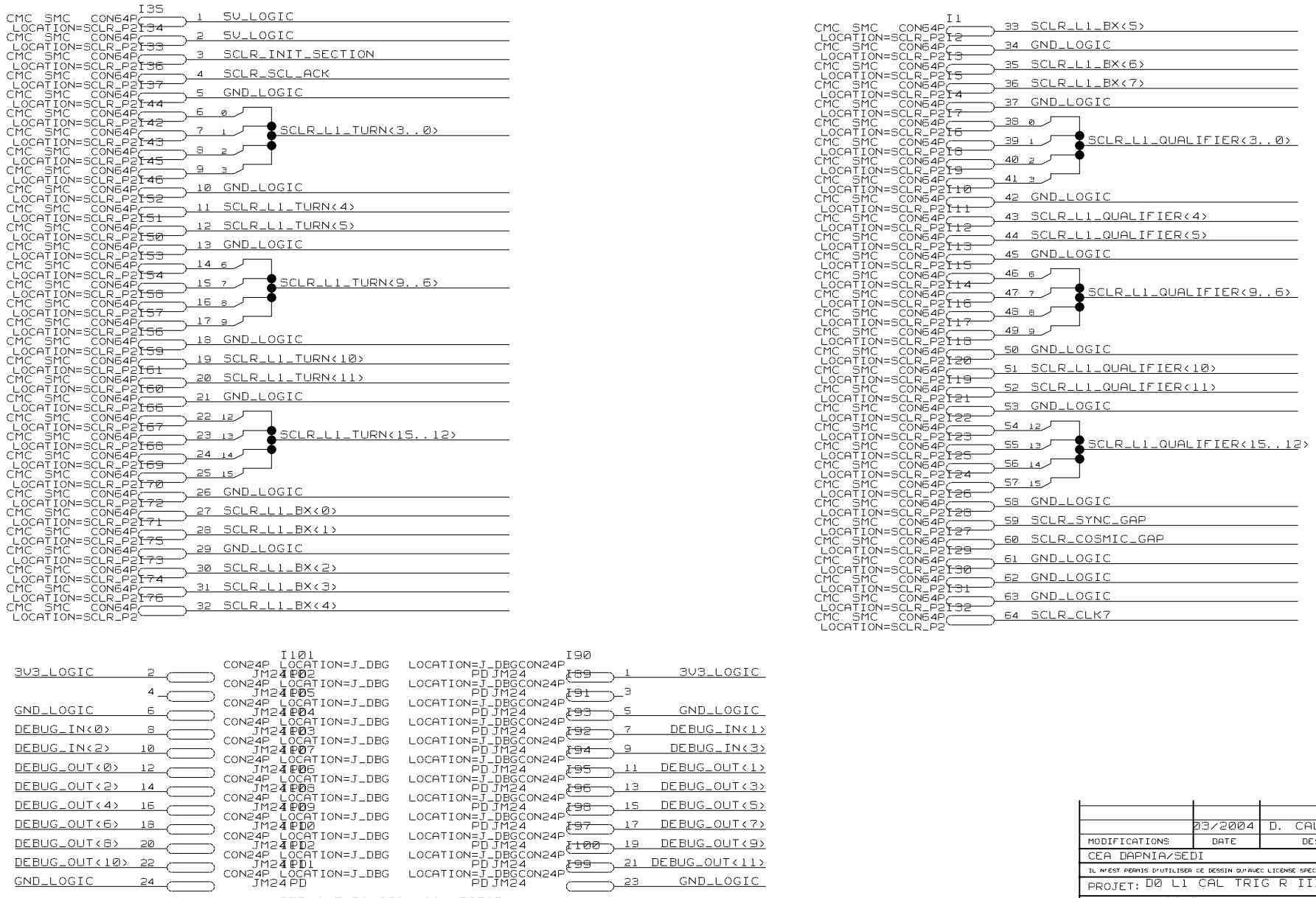
PROJET: D0 L1 CAL TRIG R IIB

ENSEMBLE: SCLD

SOUS/ENS: SCLR P1 CONNECTOR

NUMERO CIRCUIT

NUMERO PLANCHE 4


I35
CMC SMC CON64P LOCATION=SCLR_P2 I34 1 SV_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I33 2 SV_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I36 3 SCLR_INIT_SECTION
CMC SMC CON64P LOCATION=SCLR_P2 I37 4 SCLR_SCL_ACK
CMC SMC CON64P LOCATION=SCLR_P2 I44 5 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I42 6 0
CMC SMC CON64P LOCATION=SCLR_P2 I43 7 1 SCLR_L1_TURN<3..0>
CMC SMC CON64P LOCATION=SCLR_P2 I45 8 2
CMC SMC CON64P LOCATION=SCLR_P2 I46 9 3
CMC SMC CON64P LOCATION=SCLR_P2 I52 10 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I51 11 SCLR_L1_TURN<4>
CMC SMC CON64P LOCATION=SCLR_P2 I50 12 SCLR_L1_TURN<5>
CMC SMC CON64P LOCATION=SCLR_P2 I53 13 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I54 14 6
CMC SMC CON64P LOCATION=SCLR_P2 I58 15 7 SCLR_L1_TURN<9..6>
CMC SMC CON64P LOCATION=SCLR_P2 I57 16 8
CMC SMC CON64P LOCATION=SCLR_P2 I56 17 9
CMC SMC CON64P LOCATION=SCLR_P2 I59 18 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I61 19 SCLR_L1_TURN<10>
CMC SMC CON64P LOCATION=SCLR_P2 I60 20 SCLR_L1_TURN<11>
CMC SMC CON64P LOCATION=SCLR_P2 I66 21 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I67 22 12
CMC SMC CON64P LOCATION=SCLR_P2 I68 23 13 SCLR_L1_TURN<15..12>
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CMC SMC CON64P LOCATION=SCLR_P2 I70 25 15
CMC SMC CON64P LOCATION=SCLR_P2 I72 26 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I71 27 SCLR_L1_BX<0>
CMC SMC CON64P LOCATION=SCLR_P2 I75 28 SCLR_L1_BX<1>
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CMC SMC CON64P LOCATION=SCLR_P2 I74 30 SCLR_L1_BX<2>
CMC SMC CON64P LOCATION=SCLR_P2 I76 31 SCLR_L1_BX<3>
CMC SMC CON64P LOCATION=SCLR_P2 32 SCLR_L1_BX<4>
I1
CMC SMC CON64P LOCATION=SCLR_P2 I2 33 SCLR_L1_BX<5>
CMC SMC CON64P LOCATION=SCLR_P2 I3 34 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I5 35 SCLR_L1_BX<6>
CMC SMC CON64P LOCATION=SCLR_P2 I4 36 SCLR_L1_BX<7>
CMC SMC CON64P LOCATION=SCLR_P2 I7 37 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I6 38 0
CMC SMC CON64P LOCATION=SCLR_P2 I8 39 1 SCLR_L1_QUALIFIER<3..0>
CMC SMC CON64P LOCATION=SCLR_P2 I9 40 2
CMC SMC CON64P LOCATION=SCLR_P2 I10 41 3
CMC SMC CON64P LOCATION=SCLR_P2 I11 42 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I12 43 SCLR_L1_QUALIFIER<4>
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CMC SMC CON64P LOCATION=SCLR_P2 I14 46 6
CMC SMC CON64P LOCATION=SCLR_P2 I16 47 7 SCLR_L1_QUALIFIER<9..6>
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CMC SMC CON64P LOCATION=SCLR_P2 I25 55 13 SCLR_L1_QUALIFIER<15..12>
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CMC SMC CON64P LOCATION=SCLR_P2 I27 59 SCLR_SYNC_GAP
CMC SMC CON64P LOCATION=SCLR_P2 I29 60 SCLR_COSMIC_GAP
CMC SMC CON64P LOCATION=SCLR_P2 I30 61 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I31 62 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 I32 63 GND_LOGIC
CMC SMC CON64P LOCATION=SCLR_P2 64 SCLR_CLK7
3V3_LOGIC 2
4
GND_LOGIC 6
DEBUG_IN<0> 8
DEBUG_IN<2> 10
DEBUG_OUT<0> 12
DEBUG_OUT<2> 14
DEBUG_OUT<4> 16
DEBUG_OUT<6> 18
DEBUG_OUT<8> 20
DEBUG_OUT<10> 22
GND_LOGIC 24
I101
CON24P LOCATION=J_DBG JM24 P02
CON24P LOCATION=J_DBG JM24 P05
CON24P LOCATION=J_DBG JM24 P04
CON24P LOCATION=J_DBG JM24 P03
CON24P LOCATION=J_DBG JM24 P07
CON24P LOCATION=J_DBG JM24 P06
CON24P LOCATION=J_DBG JM24 P08
CON24P LOCATION=J_DBG JM24 P09
CON24P LOCATION=J_DBG JM24 P10
CON24P LOCATION=J_DBG JM24 P12
CON24P LOCATION=J_DBG JM24 P11
CON24P LOCATION=J_DBG JM24 P
LOCATION=J_DBG CON24P PD JM24
LOCATION=J_DBG CON24P PD JM24
LOCATION=J_DBG CON24P PD JM24
LOCATION=J_DBG CON24P PD JM24
LOCATION=J_DBG CON24P PD JM24
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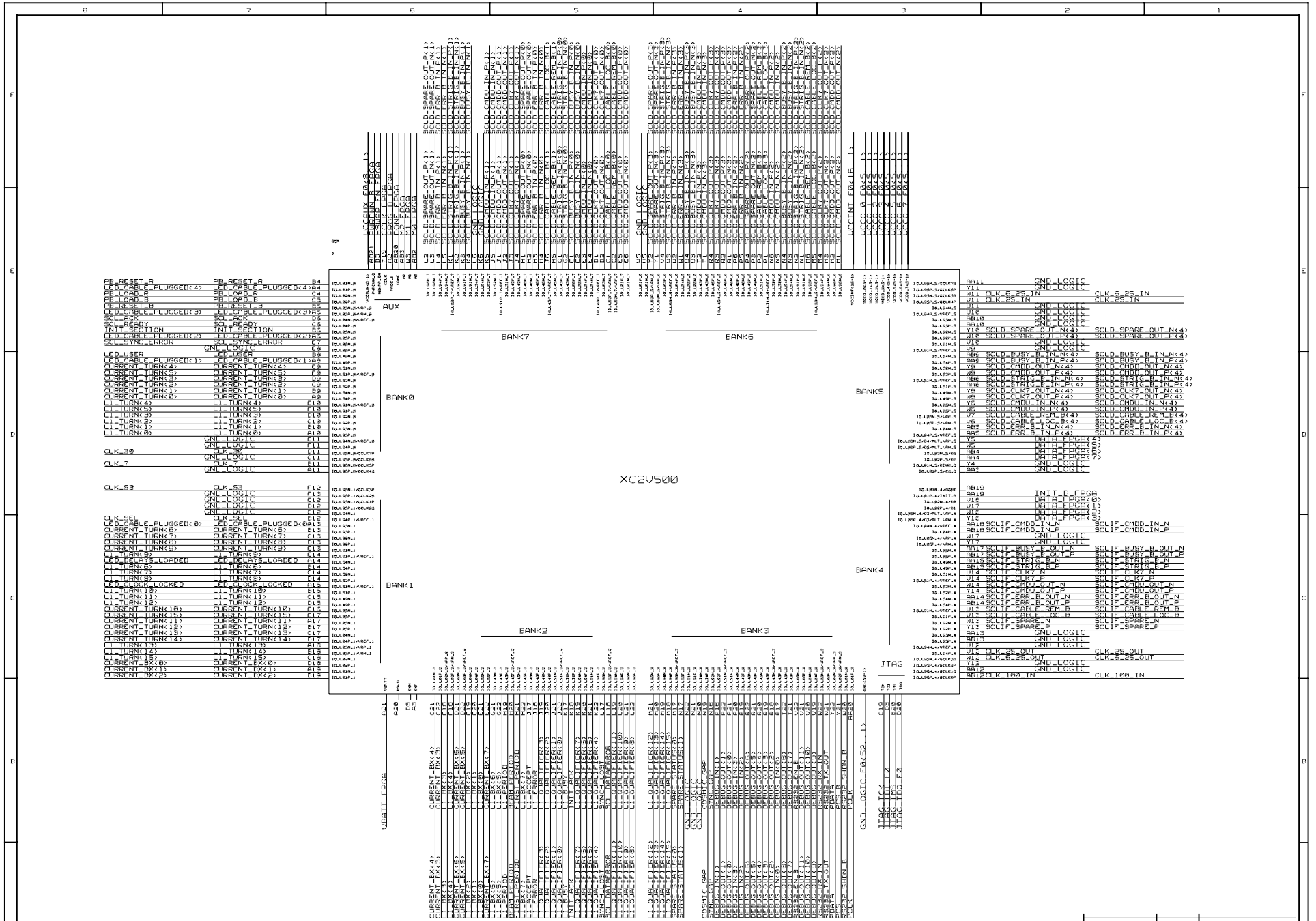
LOCATION=J_DBG CON24P PD JM24
LOCATION=J_DBG CON24P PD JM24
LOCATION=J_DBG CON24P PD JM24
LOCATION=J_DBG CON24P PD JM24
LOCATION=J_DBG CON24P PD JM24
LOCATION=J_DBG CON24P PD JM24
I90
I89 1 3V3_LOGIC
I91 3
I93 5 GND_LOGIC
I92 7 DEBUG_IN<1>
I94 9 DEBUG_IN<3>
I95 11 DEBUG_OUT<1>
I96 13 DEBUG_OUT<3>
I98 15 DEBUG_OUT<5>
I97 17 DEBUG_OUT<7>
I100 19 DEBUG_OUT<9>
I99 21 DEBUG_OUT<11>
23 GND_LOGIC
DEBUG/EXPANSION CONNECTOR
03/2004 D. CALVET
MODIFICATIONS DATE DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: D0 L1 CAL TRIG R IIB
NUMERO CIRCUIT
ENSEMBLE: SCLD
SOUS/ENS: SCLR P2 CONNECTOR
NUMERO PLANCHE 5



	03/2004	D. CALVET
MODIFICATIONS	DATE	DESSINE PAR

CEA DAPNIA/SEDI

EL MEST PERMES D'UTILISER OU DESSIN SUPERE LEGENDE SPECIALE (LIE DU LIZ/SEDI)

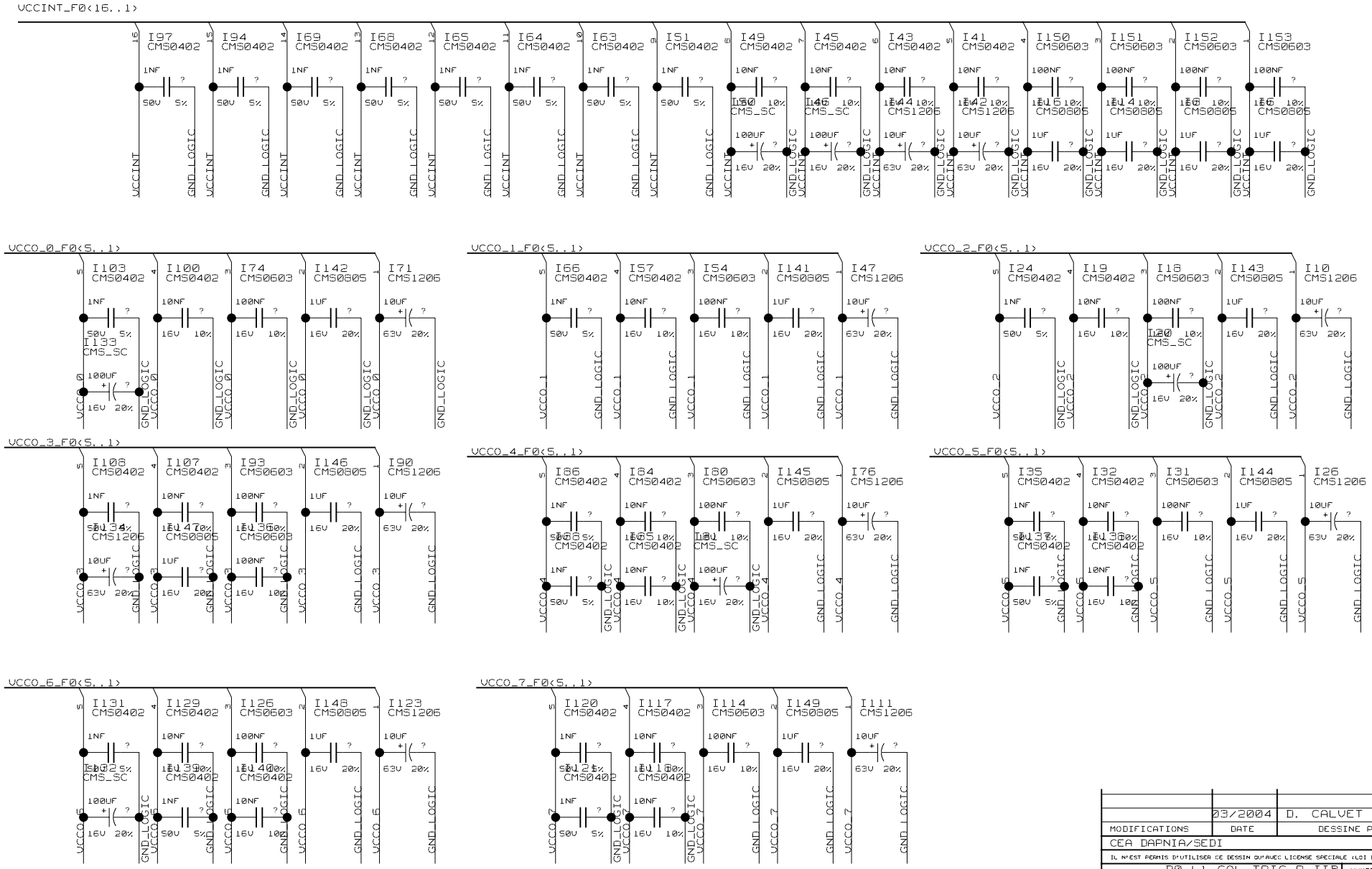
PROJET: D0 L1 CAL TRIG R IIB

ENSEMBLE: SCLD

SOUS/ENS: CORE FPGA

NUMERO CIRCUIT

NUMERO PLANCHE 6



	03/2004	D. CALVET
MODIFICATIONS	DATE	DESSINE PAR

CEA DAPNIA/SEDI

IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)

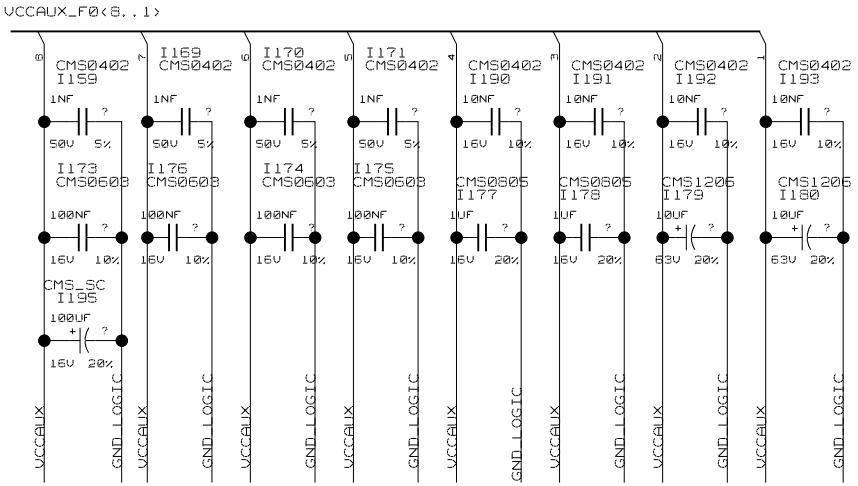
PROJET: D0 L1 CAL TRIG R IIB

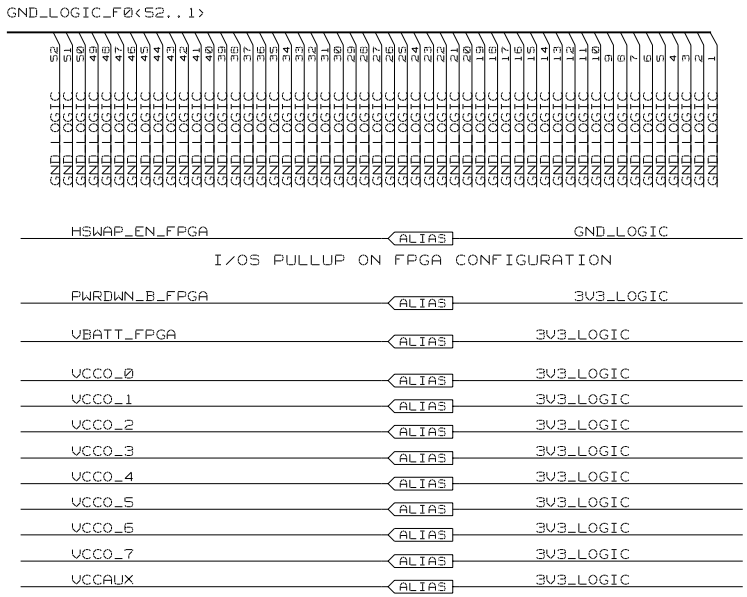
ENSEMBLE: SCLD

SOUS/ENS: FPGA DECOUPLING

NUMERO CIRCUIT

NUMERO PLANCHE 7





	03/2004	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR

CEA DAPNIA/SEDI

IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)

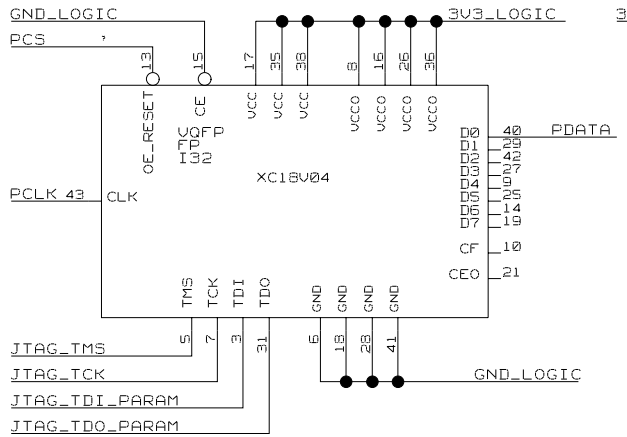
PROJET: DZERO L1 CAL RUN IIB

ENSEMBLE: SCLD

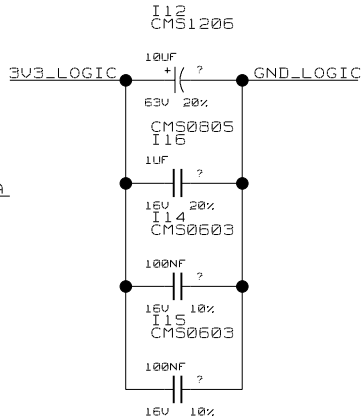
SOUS/ENS: FPGA DECOUPLING & GND

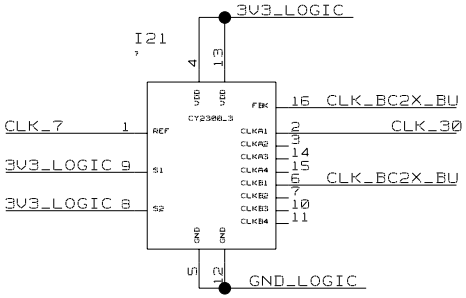
NUMERO CIRCUIT

NUMERO PLANCHE 8

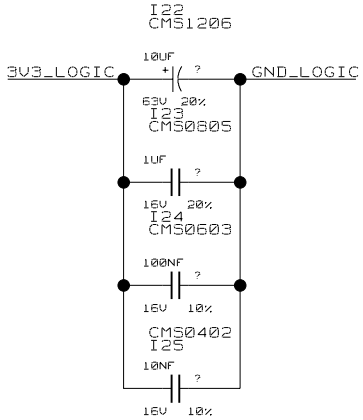


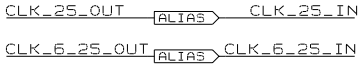
USER PARAMETER SERIAL PROM



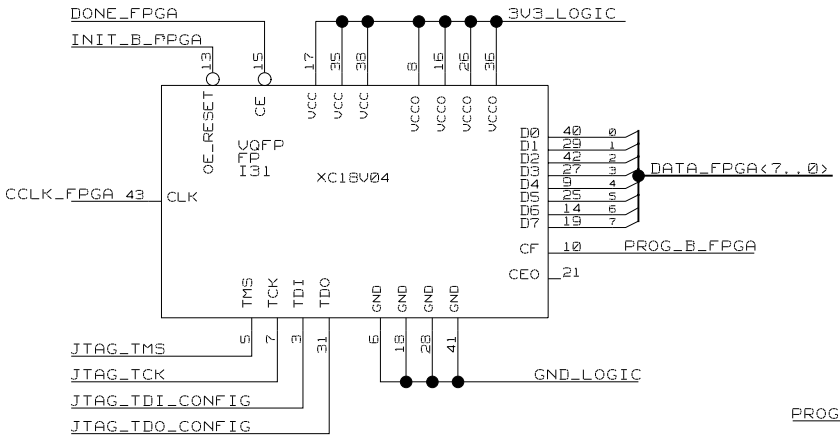


PLL FOR BC CLOCK MULTIPLICATION

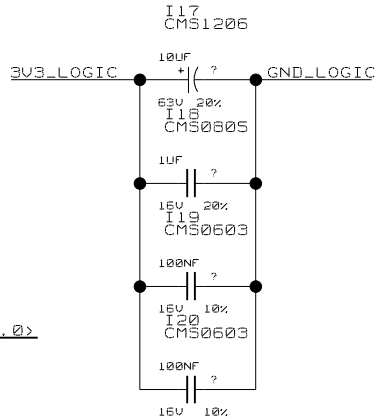


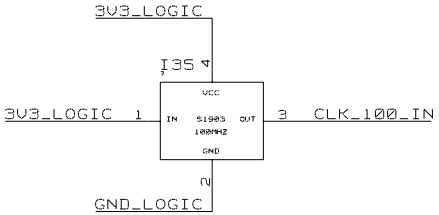


LOCAL CLOCK CONNECTIONS

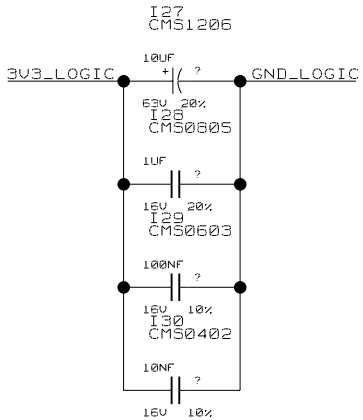


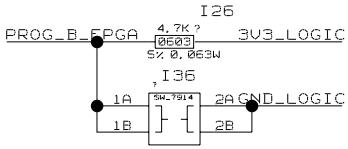
FPGA CONFIGURATION SERIAL PROM





ON BOARD OSCILLATOR





FPGA CONFIGURATION PUSH BUTTON

	03/2004	DENIS CALVET
MODIFICATIONS	DATE	DESSINE PAR

CEA DAPNIA/SEDI

IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)

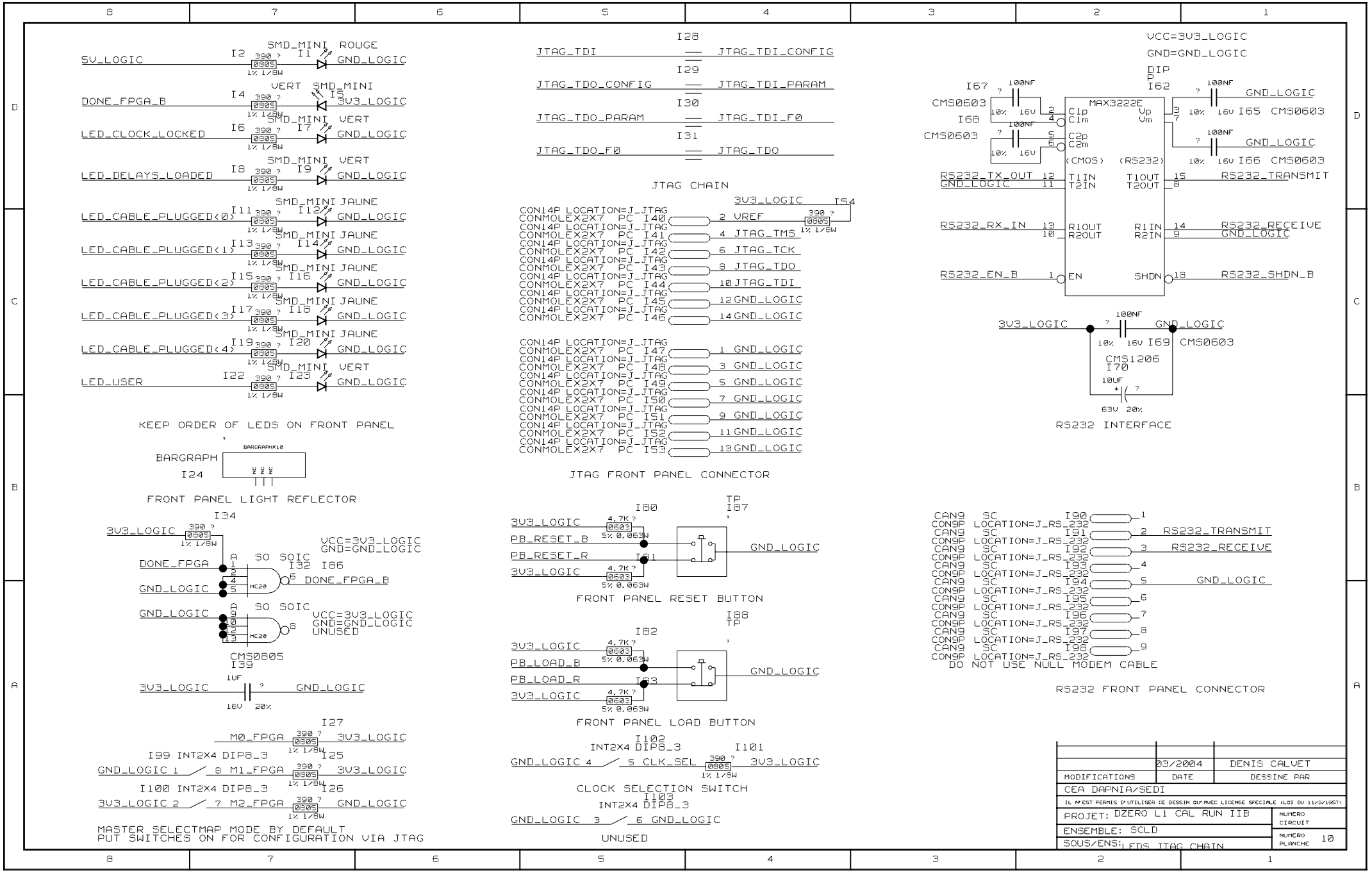
PROJET: DZERO L1 CAL RUN IIB

ENSEMBLE: SCLD

SOUS/ENS: ITAG PROMS

NUMERO CIRCUIT

NUMERO PLANCHE 9


5V_LOGIC
I2 390 ? 0805 1% 1/8W
SMD_MINI ROUGE I1
GND_LOGIC
DONE_FPGA_B
I4 390 ? 0805 1% 1/8W
VERT SMD_MINI I5
3V3_LOGIC
LED_CLOCK_LOCKED
I6 390 ? 0805 1% 1/8W
SMD_MINI VERT I7
GND_LOGIC
LED_DELAYS_LOADED
I8 390 ? 0805 1% 1/8W
SMD_MINI VERT I9
GND_LOGIC
LED_CABLE_PLUGGED<0>
I11 390 ? 0805 1% 1/8W
SMD_MINI JAUNE I12
GND_LOGIC
LED_CABLE_PLUGGED<1>
I13 390 ? 0805 1% 1/8W
SMD_MINI JAUNE I14
GND_LOGIC
LED_CABLE_PLUGGED<2>
I15 390 ? 0805 1% 1/8W
SMD_MINI JAUNE I16
GND_LOGIC
LED_CABLE_PLUGGED<3>
I17 390 ? 0805 1% 1/8W
SMD_MINI JAUNE I18
GND_LOGIC
LED_CABLE_PLUGGED<4>
I19 390 ? 0805 1% 1/8W
SMD_MINI JAUNE I20
GND_LOGIC
LED_USER
I22 390 ? 0805 1% 1/8W
SMD_MINI VERT I23
GND_LOGIC
KEEP ORDER OF LEDS ON FRONT PANEL
BARGRAPH
I24
BARGRAPHX10
FRONT PANEL LIGHT REFLECTOR
I34
3V3_LOGIC
390 ? 0805 1% 1/8W
VCC=3V3_LOGIC
GND=GND_LOGIC
DONE_FPGA
GND_LOGIC
A SO SOIC I32 I86
HC20
DONE_FPGA_B
GND_LOGIC
A SO SOIC
HC20
VCC=3V3_LOGIC
GND=GND_LOGIC
UNUSED
CMS0805
I39
1UF
3V3_LOGIC
? 16V 20%
GND_LOGIC
I27
M0_FPGA
390 ? 0805 1% 1/8W
3V3_LOGIC
I99 INT2X4 DIP8_3
I25
GND_LOGIC 1
8 M1_FPGA
390 ? 0805 1% 1/8W
3V3_LOGIC
I100 INT2X4 DIP8_3
I26
3V3_LOGIC 2
7 M2_FPGA
390 ? 0805 1% 1/8W
GND_LOGIC
MASTER SELECTMAP MODE BY DEFAULT
PUT SWITCHES ON FOR CONFIGURATION VIA JTAG
I28
JTAG_TDI
JTAG_TDI_CONFIG
I29
JTAG_TDO_CONFIG
JTAG_TDI_PARAM
I30
JTAG_TDO_PARAM
JTAG_TDI_F0
I31
JTAG_TDO_F0
JTAG_TDO
JTAG CHAIN
3V3_LOGIC
I54
390 ? 0805 1% 1/8W
CON14P LOCATION=J_JTAG
CONMOLEX2X7 PC I40
2 VREF
CON14P LOCATION=J_JTAG
CONMOLEX2X7 PC I41
4 JTAG_TMS
CON14P LOCATION=J_JTAG
CONMOLEX2X7 PC I42
6 JTAG_TCK
CON14P LOCATION=J_JTAG
CONMOLEX2X7 PC I43
8 JTAG_TDO
CON14P LOCATION=J_JTAG
CONMOLEX2X7 PC I44
10 JTAG_TDI
CON14P LOCATION=J_JTAG
CONMOLEX2X7 PC I45
12 GND_LOGIC
CON14P LOCATION=J_JTAG
CONMOLEX2X7 PC I46
14 GND_LOGIC
CON14P LOCATION=J_JTAG
CONMOLEX2X7 PC I47
1 GND_LOGIC
CON14P LOCATION=J_JTAG
CONMOLEX2X7 PC I48
3 GND_LOGIC
CON14P LOCATION=J_JTAG
CONMOLEX2X7 PC I49
5 GND_LOGIC
CON14P LOCATION=J_JTAG
CONMOLEX2X7 PC I50
7 GND_LOGIC
CON14P LOCATION=J_JTAG
CONMOLEX2X7 PC I51
9 GND_LOGIC
CON14P LOCATION=J_JTAG
CONMOLEX2X7 PC I52
11 GND_LOGIC
CON14P LOCATION=J_JTAG
CONMOLEX2X7 PC I53
13 GND_LOGIC
JTAG FRONT PANEL CONNECTOR
I80
TP
I87
3V3_LOGIC
4.7K ? 0603 5% 0.063W
PB_RESET_B
PB_RESET_R
I81
3V3_LOGIC
4.7K ? 0603 5% 0.063W
GND_LOGIC
FRONT PANEL RESET BUTTON
I88
TP
I82
3V3_LOGIC
4.7K ? 0603 5% 0.063W
PB_LOAD_B
PB_LOAD_R
I83
3V3_LOGIC
4.7K ? 0603 5% 0.063W
GND_LOGIC
FRONT PANEL LOAD BUTTON
I102
INT2X4 DIP8_3
I101
GND_LOGIC 4
5 CLK_SEL
390 ? 0805 1% 1/8W
3V3_LOGIC
CLOCK SELECTION SWITCH
I103
INT2X4 DIP8_3
GND_LOGIC 3
6 GND_LOGIC
UNUSED
VCC=3V3_LOGIC
GND=GND_LOGIC
DIP
P
I62
I67
100NF ? 10% 16V
CMS0603
I68
100NF ? 10% 16V
CMS0603
MAX3222E
C1p
C1m
C2p
C2m
Vp
Vm
(CMOS)
(RS232)
T1IN
T2IN
T1OUT
T2OUT
R1OUT
R2OUT
R1IN
R2IN
EN
SHDN
100NF ? 10% 16V I65 CMS0603
GND_LOGIC
100NF ? 10% 16V I66 CMS0603
GND_LOGIC
RS232_TX_OUT
GND_LOGIC
RS232_TRANSMIT
RS232_RX_IN
RS232_RECEIVE
GND_LOGIC
RS232_EN_B
RS232_SHDN_B
3V3_LOGIC
100NF ? 10% 16V I69 CMS0603
GND_LOGIC
CMS1206
I70
10UF ? 63V 20%
RS232 INTERFACE
CAN9 SC I90 1
CON9P LOCATION=J_RS_232
CAN9 SC I91 2 RS232_TRANSMIT
CON9P LOCATION=J_RS_232
CAN9 SC I92 3 RS232_RECEIVE
CON9P LOCATION=J_RS_232
CAN9 SC I93 4
CON9P LOCATION=J_RS_232
CAN9 SC I94 5 GND_LOGIC
CON9P LOCATION=J_RS_232
CAN9 SC I95 6
CON9P LOCATION=J_RS_232
CAN9 SC I96 7
CON9P LOCATION=J_RS_232
CAN9 SC I97 8
CON9P LOCATION=J_RS_232
CAN9 SC I98 9
CON9P LOCATION=J_RS_232
DO NOT USE NULL MODEM CABLE
RS232 FRONT PANEL CONNECTOR
03/2004
DENIS CALVET
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN SUR AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: DZERO L1 CAL RUN IIB
NUMERO CIRCUIT
ENSEMBLE: SCLD
SOUS/ENS: LEDS JTAG CHAIN
NUMERO PLANCHE
10

CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I1	A1	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I2	A2	SCLD_CLK7_OUT_N<0>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I3	A3	SCLD_CMDU_IN_N<0>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I4	A4	SCLD_STRIG_B_IN_N<0>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I5	A5	SCLD_SPARE_OUT_N<0>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I6	A6	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I7	A7	SCLD_CLK7_OUT_N<1>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I8	A8	SCLD_CMDU_IN_N<1>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I9	A9	SCLD_STRIG_B_IN_N<1>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I10	A10	SCLD_SPARE_OUT_N<1>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I11	A11	GND_LOGIC

I14

CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I13	B1	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I12	B2	SCLD_CLK7_OUT_P<0>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I16	B3	SCLD_CMDU_IN_P<0>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I15	B4	SCLD_STRIG_B_IN_P<0>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I19	B5	SCLD_SPARE_OUT_P<0>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I18	B6	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I17	B7	SCLD_CLK7_OUT_P<1>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I20	B8	SCLD_CMDU_IN_P<1>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I21	B9	SCLD_STRIG_B_IN_P<1>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I22	B10	SCLD_SPARE_OUT_P<1>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC	B11	GND_LOGIC

I24

CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I23	C1	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I25	C2	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I27	C3	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I26	C4	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I28	C5	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I30	C6	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I29	C7	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I31	C8	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I32	C9	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I33	C10	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC	C11	GND_LOGIC

I42

CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I44	D1	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I43	D2	SCLD_CABLE_REM_B<0>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I46	D3	SCLD_CMDD_OUT_N<0>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I47	D4	SCLD_BUSY_B_IN_N<0>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I45	D5	SCLD_ERR_B_IN_N<0>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I48	D6	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I49	D7	SCLD_CABLE_REM_B<1>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I54	D8	SCLD_CMDD_OUT_N<1>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I55	D9	SCLD_BUSY_B_IN_N<1>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I53	D10	SCLD_ERR_B_IN_N<1>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC	D11	GND_LOGIC

I56

CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I57	E1	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I58	E2	SCLD_CABLE_LOC_B<0>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I59	E3	SCLD_CMDD_OUT_P<0>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I60	E4	SCLD_BUSY_B_IN_P<0>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I61	E5	SCLD_ERR_B_IN_P<0>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I62	E6	GND_LOGIC
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I63	E7	SCLD_CABLE_LOC_B<1>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I64	E8	SCLD_CMDD_OUT_P<1>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I65	E9	SCLD_BUSY_B_IN_P<1>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC I66	E10	SCLD_ERR_B_IN_P<1>
CON55P LOCATION=ADF_0_1	ZPACK5X11C PC	E11	GND_LOGIC

TIE ROW F TO GND_LOGIC

I86

CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I88	A1	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I87	A2	SCLD_CLK7_OUT_N<2>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I90	A3	SCLD_CMDU_IN_N<2>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I91	A4	SCLD_STRIG_B_IN_N<2>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I89	A5	SCLD_SPARE_OUT_N<2>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I92	A6	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I93	A7	SCLD_CLK7_OUT_N<3>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I108	A8	SCLD_CMDU_IN_N<3>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I109	A9	SCLD_STRIG_B_IN_N<3>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I110	A10	SCLD_SPARE_OUT_N<3>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC	A11	GND_LOGIC

I78

CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I79	B1	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I80	B2	SCLD_CLK7_OUT_P<2>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I82	B3	SCLD_CMDU_IN_P<2>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I81	B4	SCLD_STRIG_B_IN_P<2>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I83	B5	SCLD_SPARE_OUT_P<2>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I85	B6	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I84	B7	SCLD_CLK7_OUT_P<3>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I96	B8	SCLD_CMDU_IN_P<3>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I95	B9	SCLD_STRIG_B_IN_P<3>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I94	B10	SCLD_SPARE_OUT_P<3>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC	B11	GND_LOGIC

I68

CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I67	C1	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I69	C2	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I71	C3	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I70	C4	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I72	C5	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I74	C6	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I73	C7	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I75	C8	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I76	C9	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I77	C10	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC	C11	GND_LOGIC

I111

CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I112	D1	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I113	D2	SCLD_CABLE_REM_B<2>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I114	D3	SCLD_CMDD_OUT_N<2>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I115	D4	SCLD_BUSY_B_IN_N<2>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I116	D5	SCLD_ERR_B_IN_N<2>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I117	D6	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I118	D7	SCLD_CABLE_REM_B<3>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I119	D8	SCLD_CMDD_OUT_N<3>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I120	D9	SCLD_BUSY_B_IN_N<3>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I121	D10	SCLD_ERR_B_IN_N<3>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC	D11	GND_LOGIC

I97

CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I98	E1	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I99	E2	SCLD_CABLE_LOC_B<2>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I100	E3	SCLD_CMDD_OUT_P<2>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I101	E4	SCLD_BUSY_B_IN_P<2>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I102	E5	SCLD_ERR_B_IN_P<2>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I103	E6	GND_LOGIC
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I104	E7	SCLD_CABLE_LOC_B<3>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I105	E8	SCLD_CMDD_OUT_P<3>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I106	E9	SCLD_BUSY_B_IN_P<3>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC I107	E10	SCLD_ERR_B_IN_P<3>
CON55P LOCATION=ADF_2_3	ZPACK5X11C PC	E11	GND_LOGIC

TIE ROW F TO GND_LOGIC

	03/2004	D. CALVET
MODIFICATIONS	DATE	DESSINE PAR

CEA DAPNIA/SEDI

IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)

PROJET: D0 L1 CAL TRIG R IIB

ENSEMBLE: SCLD

SOUS/ENS: SCLD <-> ADF_0_3

NUMERO CIRCUIT

NUMERO PLANCHE 11

I31
CON55P LOCATION=ADF_4_L
ZPACK5X11C PC
I32 A1 GND_LOGIC
I33 A2 SCLD_CLK7_OUT_N<4>
I34 A3 SCLD_CMDU_IN_N<4>
I35 A4 SCLD_STRIG_B_IN_N<4>
I36 A5 SCLD_SPARE_OUT_N<4>
I38 A6 GND_LOGIC
I37 A7 SCLIF_CLK7_N
I77 A8 SCLIF_CMDU_OUT_N
I75 A9 SCLIF_STRIG_B_N
I76 A10 SCLIF_SPARE_N
A11 GND_LOGIC
I23
I24 B1 GND_LOGIC
I25 B2 SCLD_CLK7_OUT_P<4>
I27 B3 SCLD_CMDU_IN_P<4>
I28 B4 SCLD_STRIG_B_IN_P<4>
I26 B5 SCLD_SPARE_OUT_P<4>
I29 B6 GND_LOGIC
I30 B7 SCLIF_CLK7_P
I39 B8 SCLIF_CMDU_OUT_P
I41 B9 SCLIF_STRIG_B_P
I40 B10 SCLIF_SPARE_P
B11 GND_LOGIC
I2
I1 C1 GND_LOGIC
I3 C2 GND_LOGIC
I5 C3 GND_LOGIC
I4 C4 GND_LOGIC
I6 C5 GND_LOGIC
I8 C6 GND_LOGIC
I7 C7 GND_LOGIC
I9 C8 GND_LOGIC
I10 C9 GND_LOGIC
I11 C10 GND_LOGIC
C11 GND_LOGIC
I78
I80 D1 GND_LOGIC
I79 D2 SCLD_CABLE_REM_B<4>
I81 D3 SCLD_CMDD_OUT_N<4>
I82 D4 SCLD_BUSY_B_IN_N<4>
I83 D5 SCLD_ERR_B_IN_N<4>
I84 D6 GND_LOGIC
I85 D7 SCLIF_CABLE_LOC_B
I86 D8 SCLIF_CMDD_IN_N
I88 D9 SCLIF_BUSY_B_OUT_N
I87 D10 SCLIF_ERR_B_OUT_N
D11 GND_LOGIC
I42
I44 E1 GND_LOGIC
I43 E2 SCLD_CABLE_LOC_B<4>
I45 E3 SCLD_CMDD_OUT_P<4>
I47 E4 SCLD_BUSY_B_IN_P<4>
I46 E5 SCLD_ERR_B_IN_P<4>
I48 E6 GND_LOGIC
I50 E7 SCLIF_CABLE_REM_B
I49 E8 SCLIF_CMDD_IN_P
I52 E9 SCLIF_BUSY_B_OUT_P
I51 E10 SCLIF_ERR_B_OUT_P
E11 GND_LOGIC
TIE ROW F TO GND_LOGIC
I90
SCLD_CMDU_IN_N<0> 100 ? 0603 I89 SCLD_CMDU_IN_P<0>
5% 0.063W
SCLD_STRIG_B_IN_N<0> 100 ? 0603 I91 SCLD_STRIG_B_IN_P<0>
5% 0.063W
SCLD_BUSY_B_IN_N<0> 100 ? 0603 I93 SCLD_BUSY_B_IN_P<0>
5% 0.063W
SCLD_ERR_B_IN_N<0> 100 ? 0603 I92 SCLD_ERR_B_IN_P<0>
5% 0.063W
3V3_LOGIC 4.7K ? 0603 SCLD_CABLE_REM_B<0>
5% 0.063W
I99
SCLD_CMDU_IN_N<2> 100 ? 0603 I101 SCLD_CMDU_IN_P<2>
5% 0.063W
SCLD_STRIG_B_IN_N<2> 100 ? 0603 I100 SCLD_STRIG_B_IN_P<2>
5% 0.063W
SCLD_BUSY_B_IN_N<2> 100 ? 0603 I103 SCLD_BUSY_B_IN_P<2>
5% 0.063W
SCLD_ERR_B_IN_N<2> 100 ? 0603 I102 SCLD_ERR_B_IN_P<2>
5% 0.063W
3V3_LOGIC 4.7K ? 0603 SCLD_CABLE_REM_B<2>
5% 0.063W
I109
SCLD_CMDU_IN_N<4> 100 ? 0603 I110 SCLD_CMDU_IN_P<4>
5% 0.063W
SCLD_STRIG_B_IN_N<4> 100 ? 0603 I111 SCLD_STRIG_B_IN_P<4>
5% 0.063W
SCLD_BUSY_B_IN_N<4> 100 ? 0603 I112 SCLD_BUSY_B_IN_P<4>
5% 0.063W
SCLD_ERR_B_IN_N<4> 100 ? 0603 I113 SCLD_ERR_B_IN_P<4>
5% 0.063W
3V3_LOGIC 4.7K ? 0603 SCLD_CABLE_REM_B<4>
5% 0.063W
I94
SCLD_CMDU_IN_N<1> 100 ? 0603 I95 SCLD_CMDU_IN_P<1>
5% 0.063W
SCLD_STRIG_B_IN_N<1> 100 ? 0603 I96 SCLD_STRIG_B_IN_P<1>
5% 0.063W
SCLD_BUSY_B_IN_N<1> 100 ? 0603 I98 SCLD_BUSY_B_IN_P<1>
5% 0.063W
SCLD_ERR_B_IN_N<1> 100 ? 0603 I97 SCLD_ERR_B_IN_P<1>
5% 0.063W
3V3_LOGIC 4.7K ? 0603 SCLD_CABLE_REM_B<1>
5% 0.063W
I104
SCLD_CMDU_IN_N<3> 100 ? 0603 I105 SCLD_CMDU_IN_P<3>
5% 0.063W
SCLD_STRIG_B_IN_N<3> 100 ? 0603 I106 SCLD_STRIG_B_IN_P<3>
5% 0.063W
SCLD_BUSY_B_IN_N<3> 100 ? 0603 I107 SCLD_BUSY_B_IN_P<3>
5% 0.063W
SCLD_ERR_B_IN_N<3> 100 ? 0603 I108 SCLD_ERR_B_IN_P<3>
5% 0.063W
3V3_LOGIC 4.7K ? 0603 SCLD_CABLE_REM_B<3>
5% 0.063W
I114
SCLIF_CLK7_N 100 ? 0603 I115 SCLIF_CLK7_P
5% 0.063W
SCLIF_SPARE_N 100 ? 0603 I116 SCLIF_SPARE_P
5% 0.063W
SCLIF_CMDD_IN_N 100 ? 0603 I117 SCLIF_CMDD_IN_P
5% 0.063W
3V3_LOGIC 4.7K ? 0603 SCLIF_CABLE_REM_B
5% 0.063W
100 OHMS DIFFERENTIAL IMPEDANCE TRACES TO ALL 100 OHMS RESISTORS
PLACE 100 OHMS RESISTORS CLOSEST TO FPGA
MATCH LENGTH OF DIFFERENTIAL PAIRS BETTER THAN 5 MM WITHIN EACH GROUP
MATCH LENGTH OF DIFFERENTIAL PAIRS BETTER THAN 2 CM WITHIN ALL GROUPS
03/2004 D. CALVET
MODIFICATIONS DATE DESSINE PAR
CEA DAPNIA/SEDI
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)
PROJET: D0 L1 CAL TRIG R IIB
NUMERO CIRCUIT
ENSEMBLE: SCLD
SOUS/ENS: SCLD (-) ADF4 + LB
NUMERO PLANCHE 12