STANDALONE TESTS OF THE ANALOG SPLITTER CARD
(Prototype)

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TESTBENCH AND ANALOG SPLITTER

Testbench
Input: sinus / square / arbitrary waveform generator Stanford Research DS345
Source: made one differential source with 2 AD 829; one voltage follower, one inverter
Load: assembled adapted loads 470 nF + 79 ohms
Visualization: 800 Msp - 100 MHz digital storage oscilloscope Gould 4084

Analog Splitter
One board assembled and tested
All channels functional and operating as designed
Board powered during 100 hours; stable performance
Power requirement: +5 V 3 A
RESPONSE WITH TRIGGER PICKOFF-LIKE SIGNAL

Channel HD 0
x scale: 100 ns/div
y scale: 2 V/div.
Input BLS+ - BLS-
Output CTFE+ - CTFE-

Channel HD 0
x scale: 100 ns/div
y scale: 200 mV/div.
Input BLS+ - BLS-
Output CTFE+ - CTFE-

Input generated with 40 MHz 12-bit precision DAC arbitrary waveform generator
Output loaded with 470 nF + 79 ohms circuit on positive and negative side

RESPONSE WITH TRIGGER PICKOFF-LIKE SIGNAL (CON’T)

Channel HD 1
x scale: 100 ns/div
y scale: 2 V/div.
Input BLS+ - BLS-
Output CTFE+ - CTFE-

Channel HD 1
x scale: 100 ns/div
y scale: 200 mV/div.
Input BLS+ - BLS-
Output CTFE+ - CTFE-

Signals on other channels look very similar to these
Unity gain when loaded - Over 6V differential voltage swing on outputs
**Frequency Response**

Channel HD 2
x axis: 10 Hz to 10 kHz
y scale: 2 V/div.

Input BLS+ - BLS-

Output CTFE+ - CTFE-

Channel HD 2
x axis: 1 MHz to 25 MHz
y scale: 2 V/div.

Input BLS+ - BLS-

Output CTFE+ - CTFE-

Flat response in 100 kHz - 10 MHz (optional compensation capacitor not connected)
Source not sufficiently performant to measure high frequency response

**Side-Effect of the Splitter on Low Frequency Response**

Existing System

![Existing System Diagram](Diagram1)

Low cutoff frequency: $\frac{1}{2\pi RC}$ slope: +6 dB/oct

System with analog splitter

![System with analog splitter Diagram](Diagram2)

Low cutoff frequency: $\frac{1}{2\pi RC}$ slope: +12 dB/oct

Plugging the splitter in D0 will change the low frequency response for the existing system because one additional RC cell is introduced in the circuit

-> this is not thought to be an issue for the kind of signal dealt with
**SQUARE SIGNAL RESPONSE**

Channel HD 2
x scale: 2 us/div
y scale: 1V/div.

Input BLS+ - BLS-
100 kHz square

Output CTFE+ - CTFE-

Channel HD 2
x scale: 250 ns/div
y scale: 1V/div.

Input BLS+ - BLS-
1 MHz square

Output CTFE+ - CTFE-

Test not relevant to the real usage of the splitter - informative plot only

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**SHORT TERM PLANS**

**2ND VERSION OF PCB: LIST OF MODIFICATIONS**

- Add heat sink below each amplifier
- Correct DC/DC converter CAD information to put device on PCB component side
- Increase width of power supply trace
- Use bigger fonts for labels and move some of them
- Place label for +5V, GND and LEDs (+12 V -12 V)
- Place label with name of board and origin
- Use surface mount tantalum capacitor instead of through hole type

**SCHEDULE FOR TEST, INSTALLATION AND NEW VERSION**

- Ship board to Fermilab (December 2002)
- Tests at Fermilab, yes/no for plugging board in D0
- If yes, plug splitter during January 2003 shutdown; if no, modifications
- Check no perturbation introduced by splitter (January 2003)
- Make all corrections/modifications for 2nd version of PCB (February 2003)
- Produce 3-4 new boards (Spring 2003)