D0 DAQ GEOGRAPHIC SECTION SPECIFICATION

A Geographic Section (GS) is a subsystem responsible for transferring data from a particular portion of a detector to the D0 Data Acquisition System under the control of the D0 Trigger Framework (TFW). There are up to 128 Geographic Sections in the D0 Data Acquisition System. Each GS has its own crate, a Data Acquisition Interface module (VBD) and a D0 host computer interface module within that crate. The host computer interface module could be either a networked VME processor or a custom interface module (e.g. Vertical Interconnect). Each GS communicates with the front-end electronics and the TFW providing the necessary synchronization between the TFW and the detectors. The TFW controls the GS's by means of a Serial Command Link (SCL)[1]. The Serial Command Link consists of one unidirectional high speed serial link from the TFW to each GS and one unidirectional link from each GS to the TFW. The signals on both links are described elsewhere[1]. The SCL provides all the necessary signals for proper GS synchronization.

A GS is responsible for providing all the necessary signals to the front-ends (FE) to guarantee proper timing and event synchronization. These must include but are not limited to:
- 53.104 MHz accelerator RF clock
- FIRST CROSSING signal
- SYNC GAP signal
- INIT signal

A GS is responsible for *the proper delay adjustment of the appropriate signals* in order to achieve synchronization between the detectors and accelerator beam crossings. The synchronization of all the elements of the D0 data acquisition system is predicated on correct timing of the detectors relative to the beam crossings.

A FE may generate beam crossing numbers and beam turn numbers using the RF clock, FIRST CROSSING and INIT signals. The FIRST CROSSING and INIT signals must be used to preset the beam crossing counter and the beam turn counter during the GS initialization process. A FE may generate optional sub-harmonics of the RF clock using frequency dividers synchronized by the FIRST CROSSING and INIT signals[2].

Each GS is required to have a pipeline to store incoming events until a TFW decision is made. The minimum pipeline delay is determined by the Level 1 decision time of 3.56 μs (at the TFW location[11]) and the signal propagation time from the TFW to the GS. Each GS must have the ability to store events accepted by the TFW. Events accepted by L1 and L2 decisions are stored in Level 1 and Level 2 buffers respectively (Figure 1). The control of event storage is achieved by means of the BUSY1, BUSY2, L1 ACCEPT, L2 ACCEPT and L2 REJECT signals. Each stored event should include beam crossing and turn numbers associated with it.

EVENT

L1
ACCEPT

L1
BUFFER

L2   L2
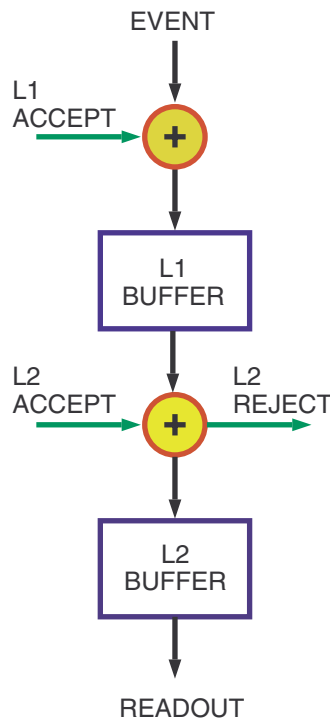ACCEPT   REJECT

L2
BUFFER

READOUT

Figure 1. D0 buffering scheme.

Each GS should maintain a 16 entry deep record of diagnostic messages available for later analysis. The conditions under which a new entry is added is sub-system dependent, however, every GS is required to make an entry for each error reported to the TFW as well as for each transition of INIT that has occurred. These entries must contain status and errors from past events, the turn and crossing numbers associated with the errors, and a time stamp supplied by a local real time clock. Additional system specific information may be stored in the record. Only the 16 most recent entries will be kept. The information from this record should be accessible via standard D0 on-line tools such as EPICS, COMICS software.

Each GS is required to use a Dallas Semiconductor DS1643 Nonvolatile Timekeeping RAM. The chip's memory and registers have to be accessible via VME address space. The access from the host to the Nonvolatile Timekeeping RAM has to be provided via either a networked VME processor or a custom interface module (e.g. Vertical Interconnect). All diagnostic messages are required to be stored in the 8K byte non-volatile memory of the DS1643. The format of diagnostic messages common for all GS's follows: (data words are 16 bits). Sixteen bit VME access is required. We use Big Endian byte ordering that presents the most significant byte in the lower address.

- Time of Event   (8 bytes = 7 bytes of DS1643 data + one spare byte)
- Crossing Number   (2 bytes, upper byte undefined)
- Turn Number   (2 bytes)
- Status   (2 bytes)
- Error Type   (2 bytes)
- User defined   (240 bytes)

The data in the Time of Event part of the entry has to be presented in the following order starting with the lowest address:

- Undefined byte (MSB) and Seconds (LSB)
- Minute (MSB) and Hour (LSB)
- Day (MSB) and Date (LSB)
- Month (MSB) and Year (LSB)

Table 1 is a map of the DS1643 registers. All data is in 24 hour BCD format. It is assumed that one can use the D0 on-line tools EPICS, COMICS to access all the GS's using the Vertical Interconnects or their equivalent and be able to synchronize the DS1643 clocks with the necessary precision.

Table 1.

Address	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	Function
X1FF	D_{80}	D_{40}	D_{20}	D_{10}	D_8	D_4	D_2	D_1	Year (00-99)
X1FE	X	X	X	D_{10}	D_8	D_4	D_2	D_1	Month (01-12)
X1FD	X	X	D_{20}	D_{10}	D_8	D_4	D_2	D_1	Date (01-31)
X1FC	X	FT	X	X	X	D_4	D_2	D_1	Day (01-07)
X1FB	X	X	D_{20}	D_{10}	D_8	D_4	D_2	D_1	Hour (00-23)
X1FA	X	D_{40}	D_{20}	D_{10}	D_8	D_4	D_2	D_1	Minute (00-59)
X1F9	OSC	D_{40}	D_{20}	D_{10}	D_8	D_4	D_2	D_1	Seconds (00-59)
X1F8	W	R	NC	NC	NC	NC	NC	NC	Control A

The memory map is shown in the Table 2. When using Vertical Interconnect the base address of the DS1643 has to be between 0000 and E000 (hex). The suggested base address is 8000 (hex). The contents of the Diagnostic Entries is sub-system dependent.

Table 2.

Starting Address (hex)	Size (bytes)	Comment
Base + 0000	256	Diagnostic Entry 1
Base + 0100	256	Diagnostic Entry 2
Base + 0200	256	Diagnostic Entry 3
Base + 0300	256	Diagnostic Entry 4
Base + 0400	256	Diagnostic Entry 5
Base + 0500	256	Diagnostic Entry 6
Base + 0600	256	Diagnostic Entry 7
Base + 0700	256	Diagnostic Entry 8
Base + 0800	256	Diagnostic Entry 9
Base + 0900	256	Diagnostic Entry 10
Base + 0A00	256	Diagnostic Entry 11
Base + 0B00	256	Diagnostic Entry 12
Base + 0C00	256	Diagnostic Entry 13
Base + 0D00	256	Diagnostic Entry 14
Base + 0E00	256	Diagnostic Entry 15
Base + 0F00	256	Diagnostic Entry 16
Base + 0000	2	Last message address pointer
Base + 0002	206	Reserved
Base + 00D0	2	GS ID
Base + 00D2	2	GS Status
Base + 00D4	3628	User defined NVRAM area
Base + 0F00	248	Reserved
Base + 0FF8	8	DS1643 registers

GS ID is a crate identification number that is specified for every sub-system according to the crate ID map[3]. GS Status word bits are described below.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UD	UD	UD	UD	UD	UD	UD	UD	UD	UD	UD	UD	HB	GE	RM	LM

Where,

        LM   - Local Mode bit; if LM = 1, GS is in a local mode

        RM   - Run Mode bit; if RM = 1, GS is in a run mode

        GE   - Global Error bit; if GE = 1, GS is not running properly

        HB   - HeartBeat bit, has to be set to one every 500 ms by running GS hardware or software

        UD   - User Defined bits; they are sub-system dependent.

Note that LM and RM bits can be each set to one, but not both simultaneously.

There are several modes or states of a GS, which have to be considered separately. The following modes are sufficient to run a GS at the moment:

INITIALIZATION.

1. The Trigger Framework issues the initialization signal (INIT) to every Geographic Section in order to synchronize the preparations for data taking. Both transitions of the INIT have to be detected by each GS. Upon receipt of the first transition, every GS has to assert its INACK signal as soon as possible and start its initialization process. Upon completion, a GS will deassert its INACK to indicate the end of initialization. All error signals have to be cleared during the GS initialization process. When every GS has deasserted its INACK the TFW will remove INIT. No L1 ACCEPTs will be issued while INIT is active and until the next FIRST CROSSING is generated after INIT is deasserted. The minimum duration of the INACK required being not less than one beam rotation interval (i.e., 21 μs).
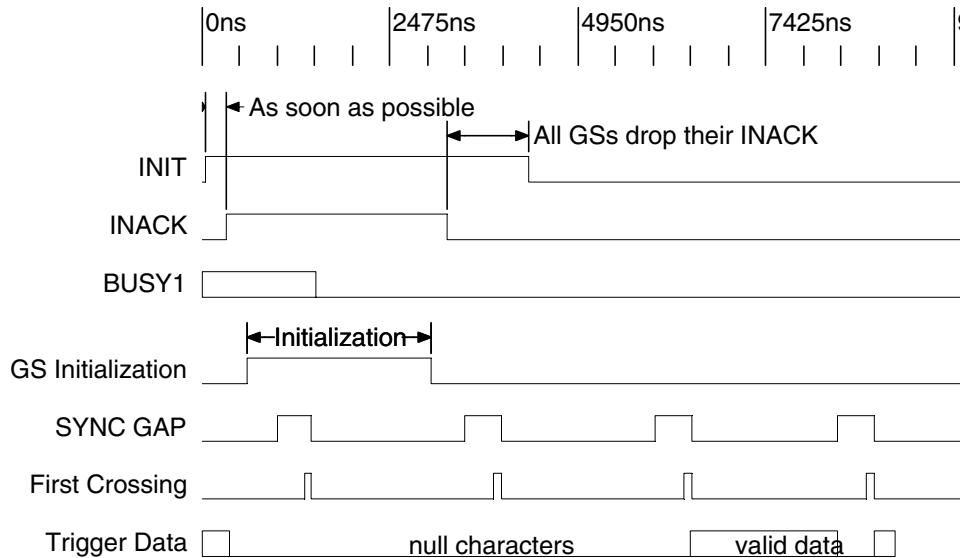

Figure 2. Timing Diagram of the Initialization Procedure.

2. INIT is synchronous to the 7.59 MHz clock (as are the rest of the TFW signals), but otherwise may change state at any time within a turn except beam crossing number $1^{/1/}$. This is the beam crossing within SYNC GAP interval marked by the first transition of the FIRST CROSSING signal. Each GS is required to monitor both FIRST CROSSING and INIT. Any time a GS detects FIRST CROSSING while INIT is true initialization is in progress. The first FIRST

CROSSING after INIT drops indicates the end of initialization and a switch back to normal data taking and marks beam turn number one. Each FIRST CROSSING signal with the INIT at true level should set any frequency dividers, beam crossing counters and turn counters to their initial state thus providing re-synchronization. The beam crossing counter must be preset to 1 and the turn counter must be reset to zero. The turn counter is incremented by the FIRST CROSSING whenever INIT is not present. Turn one would be the first to contain physics data after INIT. When the turn counter reaches 0xFFFF it would roll over to 0x0 on the following orbit. The duration of the INIT should be not less than one beam rotation interval (i.e., 21 μs$^{/1/}$).

3. Upon the receipt of INIT, any FE connected to a L1 trigger system must stop transferring L1 trigger data and switch to transferring 'null' characters while INIT is true. This will serve to clock out any information stored in the Level 1 trigger input FIFOs and re-synchronize them. After INIT is dropped by the TFW, each GS connected to the L1 trigger system must continue the transmission of 'null' characters until the arrival of the next SYNC GAP. The transmission of valid trigger data resumes at the end of the sync gap interval as it does during normal data taking.

4. Any L1, L2 or L3 data transfers in progress at the onset of INIT should not be halted. This avoids the transmission of partial data blocks resulting from initialization. After these transfers are completed, any events remaining in the L1 or L2 data buffers have to be discarded before dropping INACK.

RUN MODE.

1. During data taking (RM bit is set to one) each GS communicates with the TFW by receiving L1 ACCEPT, L2 ACCEPT and REJECT signals and generating BUSY1, BUSY2, ERROR1 and ERROR2 signals. Each GS is required to compare the crossing and beam turn numbers associated with an event at the output of the pipeline with the trigger number received with the L1 or L2 decision. The following table lists those functions that are mandatory for every GS:

Signal	Required action
L1 ACCEPT	Store an event in L1 buffer
ERROR1	Assert this signal in case of L1 trigger number mismatch or other error associated with L1 activities

BUSY1	Assert this signal while a GS cannot execute L1 ACCEPT signals
L2 ACCEPT	Move an event from L1 buffer to L2 buffer
L2 REJECT	Remove an event from L1 buffer
ERROR2	Assert this signal in case of L2 trigger number mismatch or other error associated with L2 activities
BUSY2	Assert this signal while a GS cannot execute L2 ACCEPT signals

2. A GS must report to the TFW any of the error conditions described above by asserting ERROR1 or ERROR2 signals. These signals have to be held active until an INIT is issued by the TFW.

3. The appropriate busy signals have to be asserted for the duration of any busy conditions. The state of both busy signals has to be readable by VME thus allowing the tracing of any stuck busy lines. A GS design must guarantee that the busy signal associated with a L1 or L2 accept will arrive at the TFW location not later than a specified minimum time interval between two accepts of the same type. This interval is defined by the round trip signal propagation time for the GS furthest away from the TFW, in order to have just one trigger decision en route between the TFW and the GS, giving the TFW enough time to inhibit the next accept. This interval could be increased if necessary, but cannot be lesser than described above value. Note that BUSY1 and BUSY2 inhibit only accepts. L2 rejects are not affected by the BUSY2 signal and can be generated at any time after a GS asserts its busy signal. At the moment, the minimum time between L1s is defined as the accelerator gap interval (2.6 μs, twenty 7.59 MHz clock intervals). The L2 minimum interval set by the longest cable delay, presently defined to be 1.58 μs (twelve 7.59 MHz clock intervals). Sub-systems with no direct control of input data stream (e.g. trigger systems) may issue a BUSY1 signal at the 16th event or earlier depending on amount of buffer memory they have.

4. Each GS is required to provide a 16 event deep buffer memory for L1 and 8 deep buffer memory for L2 events. Events in the L1 buffer memory have to be sequentially accepted or rejected by the L2 decisions in the same order they have been stored in the buffer (first-in-first-out sequence). An ERROR 2 will be raised by the GS if the L2

decision trigger number doesn't match the corresponding event crossing and turn numbers in the buffer. This assures a deterministic event flow and simplifies debugging and testing of the data acquisition system. Events stored in the L2 buffers must be sequentially transferred to the VBD module.

5. Each GS connected to the L1 trigger system is required to generate 'null' characters while the SYNC GAP signal is active. This will assure correct event synchronization of the L1 trigger systems.

6. Each GS has to store a sixteen bit transfer number received from the TFW with L2 accept and associate it with the event. Appropriate address has to be programmed in the VBD DMA controller memory in order to append this information to the event. This will be used for event synchronization checks at Level 3 data processing.

LOCAL MODE.

1. When a GS is in local mode, the TFW may stop sending trigger decisions to this particular GS, but continue sending timing signals. This mode may be used for local diagnostics and tests. No data transfers via the VBD data cable are allowed in this mode. LM bit equal to one in the GS status register indicates operation in local mode.

REFERENCES:

1. D.Edmunds. "Serial Command Link Description, D-Zero Run II Trigger DAQ System", http://www.pa.msu.edu/hep/d0/ftp/scl/scl_description.ps.

2. B.Baldin, S.Hansen. "Proposed synchronization scheme for D0 detectors in Run II", D0 Note 2705, 9/8/95.

3. M.Fortner. "D0 crate ID map", d0server4.fnal.gov/users/fortner/crates.pdf