Development of hybrid pixel detectors (ATLAS, CMS, BTeV)

Bottom line: Pixels are almost ready for prime time.

- sensors are now very rad hard (to ~ $10^{15}/cm^2$)
- "deep submicron" CMOS is very rad hard (to > $10^{15}/cm^2$)
- biggest remaining challenge is to make "thin" assemblies (<< 2% of L_{rad} per measurement)

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David Christian

July 9, 2001

Stating the obvious (Pixels vs. Strips)

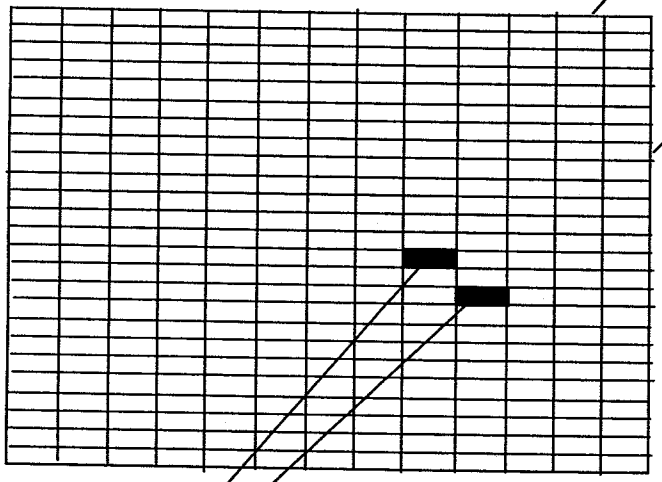
Primary pixel advantage is pattern recognition power, but also:

- much better signal/noise ➔
  - ~100% efficiency
  - slightly better radiation tolerance
  - slightly better position resolution

Fundamental pixel disadvantage is more material per measurement, but also:

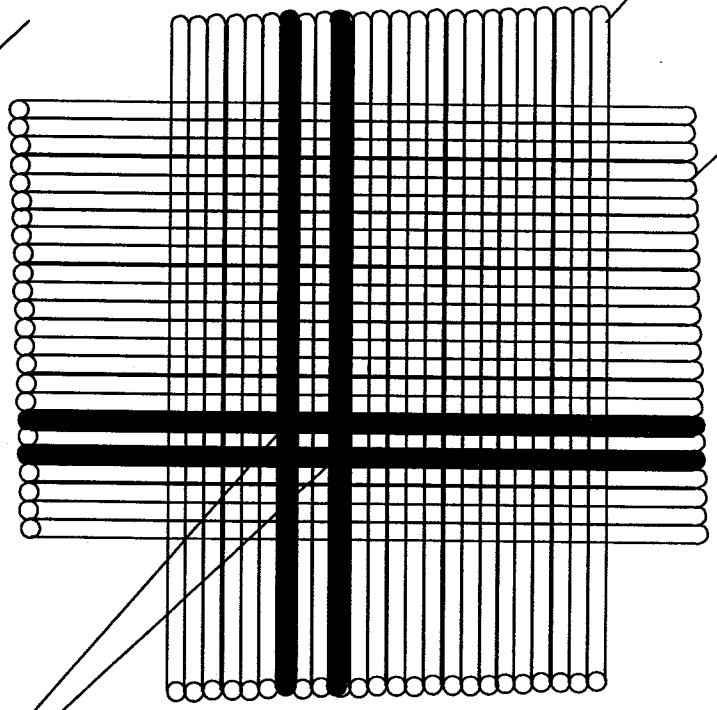
- more complicated system
- new technology

Pixels provide "space point" measurements



Very large number of active elements -electronics must be distributed in the active area of the detectors.

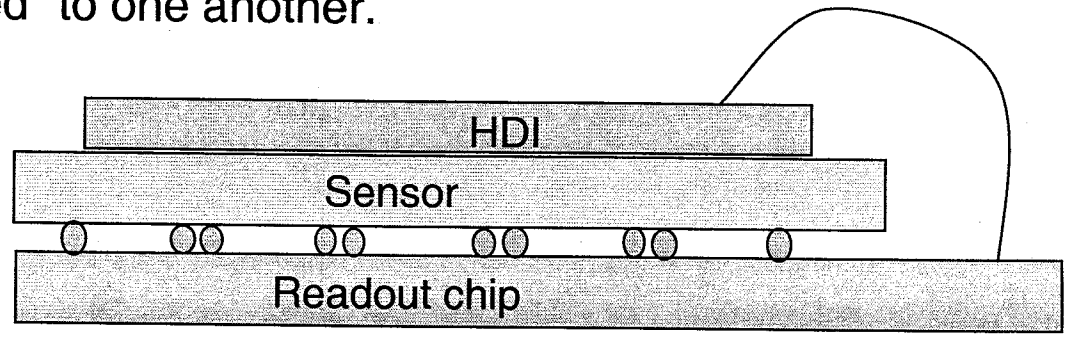
Strip detectors and straw tube chambers provide "projective" measurements



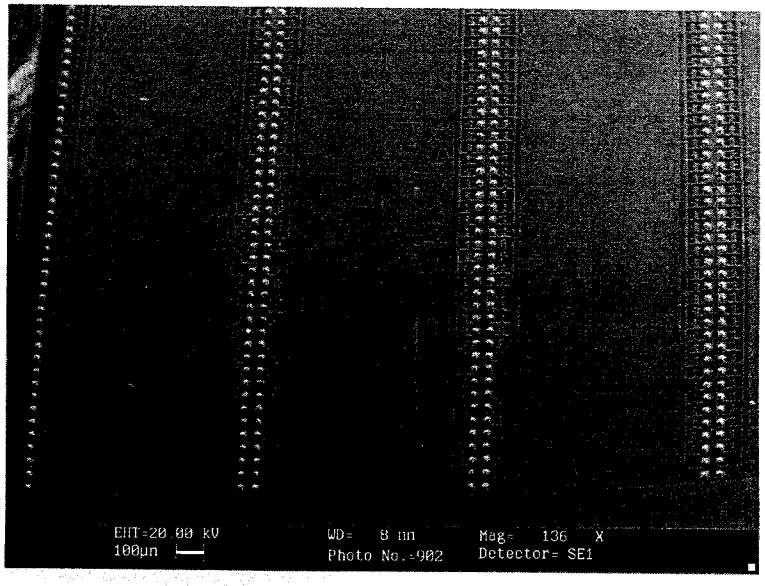
Relatively fewer active elements -electronics may be located at the edges of the detectors.

Hybrid pixel detectors

•Sensors & readout "bump bonded" to one another.
•Readout chip is wire bonded to a "high density interconnect" which carries bias voltages, control signals, and output data.



•Readout chip & HDI in the active area (& need to cool the readout chip) ➔ necessarily more material per measurement than SSD.



Micrograph of FPIX1: bump bonds are visible

Recent results: radiation tolerance of "deep submicron" CMOS circuits.

- Quick review of radiation damage to CMOS circuits
- Basics of design techniques for radiation tolerance in "deep submicron" CMOS
- "Single Event Effects"
- Results of test circuit irradiations

Surprise: special layout techniques make standard "deep submicron" CMOS processes even more radiation hard than the (larger feature size) military processes.

RD-49 established (1997?) to explore radiation tolerance of standard "deep submicron" CMOS.

First thought that standard processes might be usable for devices which would be exposed to <1 MRad.

Recent results look much better than that: simple CERN amplifiers "worked well" after 30 MRad (late 1998)! …preFPIX2 amplifiers are almost unaffected by 33MRad ^{60}Co γ exposure… ditto 26 MRad 200 MeV proton exposure.

FPIX Roadmap

- Pixel size = 50μ x 400μ (matches ATLAS n^+ on n test sensors)

- Target rad-hard technology = Honeywell 0.5μ CMOS (SOI)
  (3 metal, 3.3V) (1 metal layer used for shield between sensor & R/O chip)

- FPIX0 (1997) HP 0.8μ CMOS
  - Close to final analog front end
  - R/O pixel includes a peak sensor – digitized off chip
  - Array size = 12 x 64
  - Bench tests and beam tests

- FPIX1 (1998) HP 0.5μ CMOS
  - Optimized front end
  - 4 comparators per cell (2-bit FADC)
  - New fast R/O architecture, allows both self-triggered and externally-triggered operation
  - Array size = 18 x 160
  - Bench tests and beam tests

- *Then (Dec, 1998), a change of plans*
  - Try to use deep-submicron CMOS
  - All subsequent prototypes should be rad-hard.

FPIX2 Roadmap

- 0.25μ CMOS
  - (5 metal [6 possible], 2.5V)

- Design for 2 vendors ("lowest common denominator" design rules):
  - "CERN" – Very favorable contract, but problems with US Gov. restrictions
  - Taiwan Semiconductor Manufacturing Corp (TSMC) – Available through MOSIS

- PreFPIX2-T (1999) TSMC 0.25μ CMOS
  - New analog front end, with new leakage current compensation strategy
  - 8 comparators per cell (3-bit FADC); no EOC logic included
  - Array size = 2 x 160
  - Bench tests (radiation exposure)

- PreFPIX2-I (2000) "CERN" 0.25μ CMOS
  - Same front end
  - Complete "core" – including new, simplified EOC & R/O (self-triggered only)
  - Array size = 18 x 32

- PreFPIX2-Tb (2000) TSMC 0.25μ CMOS
  - New programming interface
  - Internal DAC's – no external currents required; only external voltages are 2.5V & ground.
  - Array size = 18 x 64

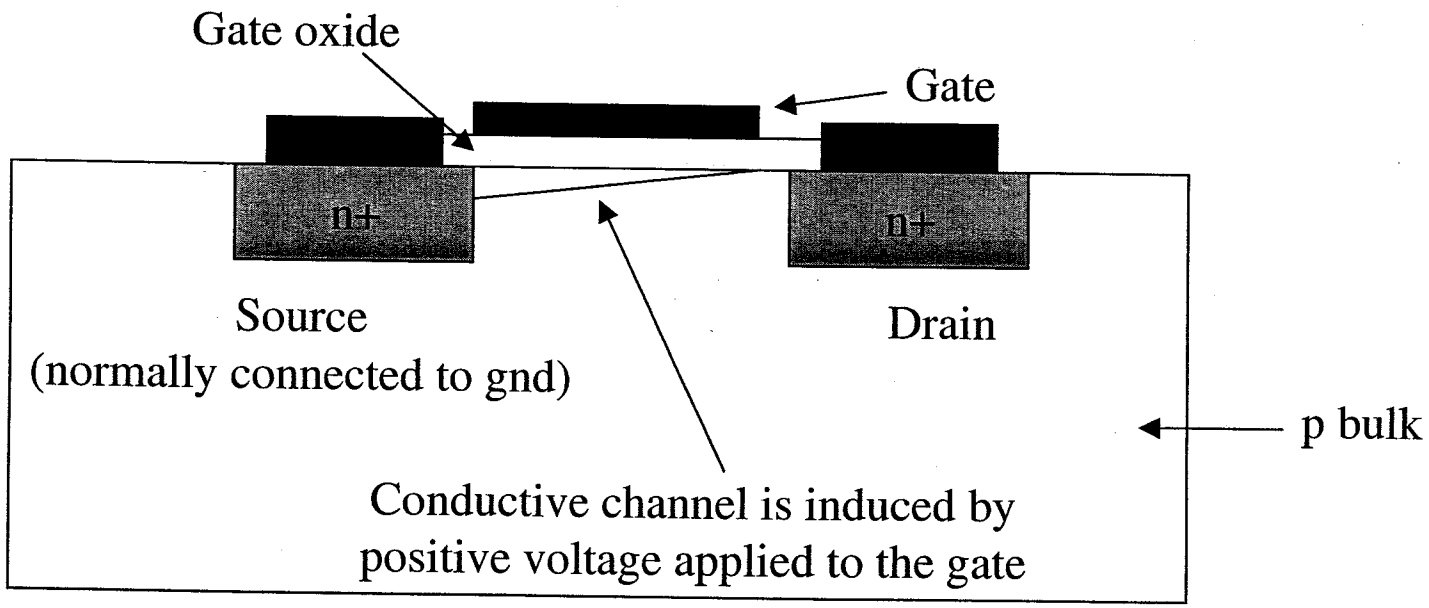
- FPIX2 (2001) 0.25μ CMOS - Final BTeV R/O chip!!??

Approximate CMOS technology roadmap

Year	Min. Feature	Supply Voltage
1995	0.80μ	5V
1996	0.50μ	3.5V
1997	0.35μ	
1999	0.25μ	2.5V
2001	0.18μ	1.8V
2003	0.13μ	1.3V

Radiation Damage to CMOS Circuits

Positive charge trapped in the oxide layer effectively biases the transistors.



"Threshold voltage" shifts with exposure to radiation

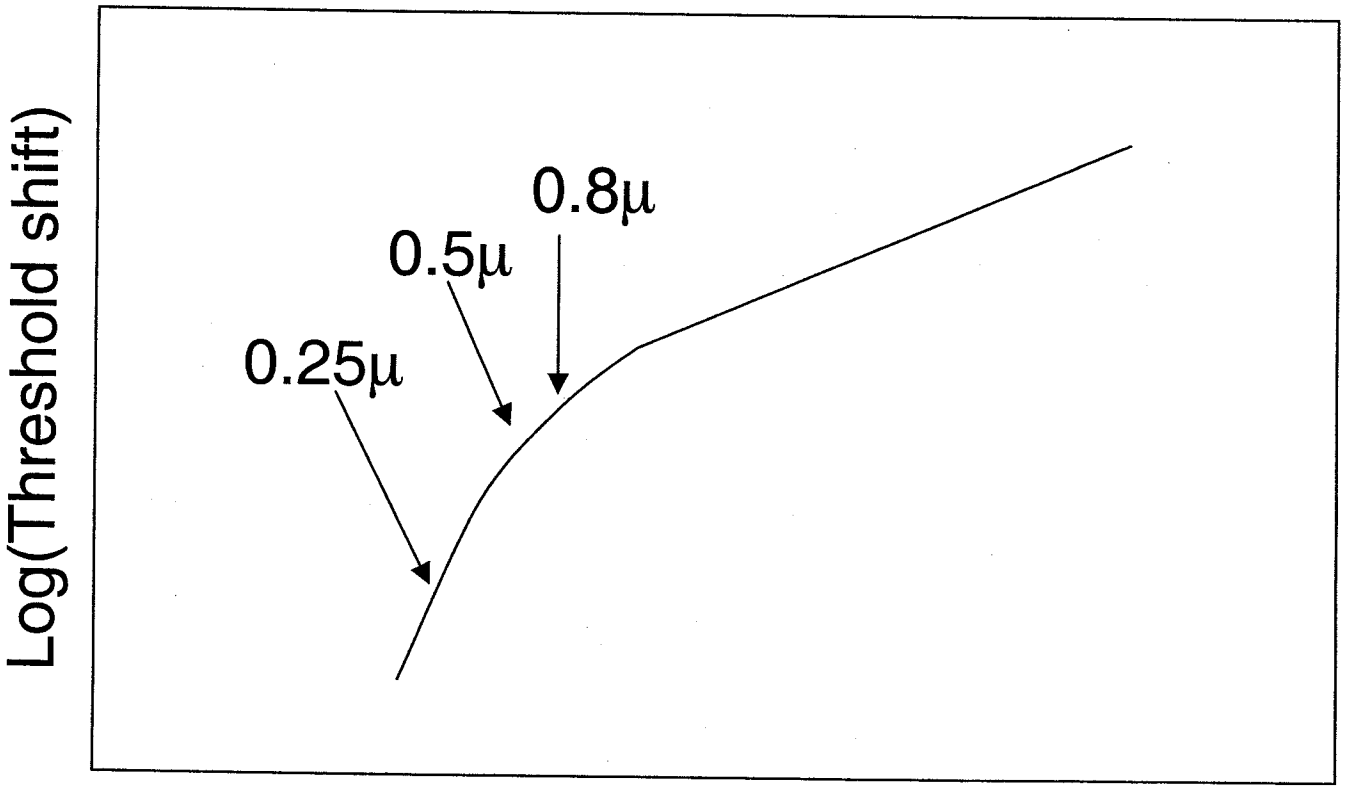
Radiation hard CMOS processes developed for military applications work primarily because they don't allow positive charge to accumulate in the oxide layers.

However, it has been known for some time that the amount of charge trapped in the oxide layers depends dramatically on the oxide thickness.

Since oxide thickness scales with feature size, smaller feature size CMOS processes suffer much less V_{th} shift than larger feature size processes for a given radiation dose.

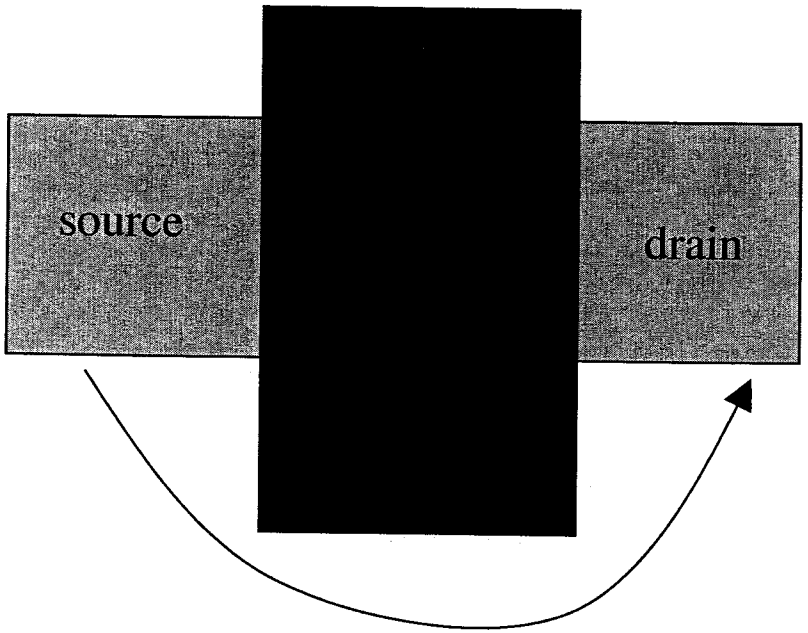
"Deep submicron" CMOS gate oxides are thin enough so that most positive charge tunnels out of oxide.

Threshold shift after a given radiation dose



Minimum feature size (gate oxide
Thickness scales down with feature size)

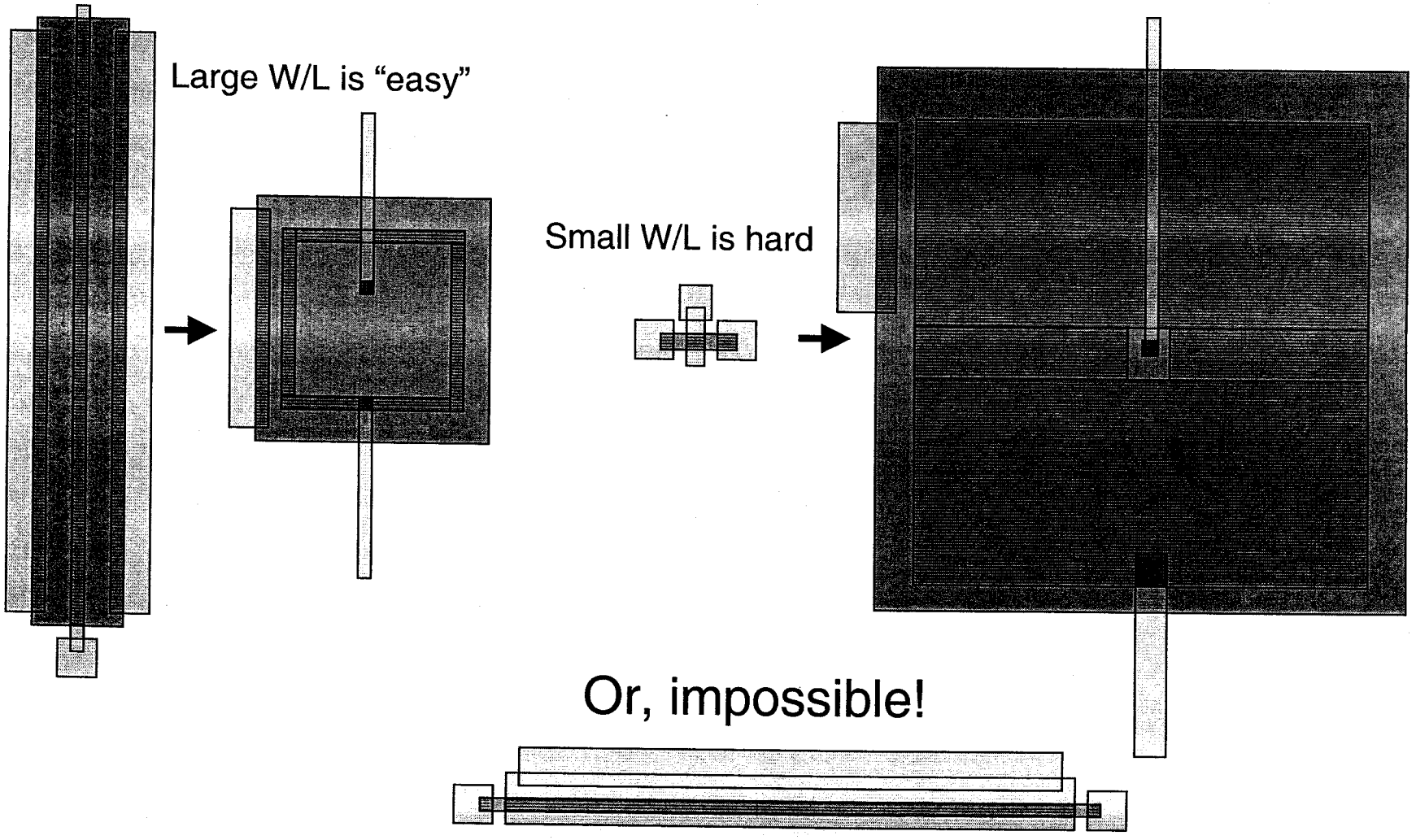
Trapped charge in the field oxide also causes leakage current in nmos devices by inducing an n-channel in the p-bulk.



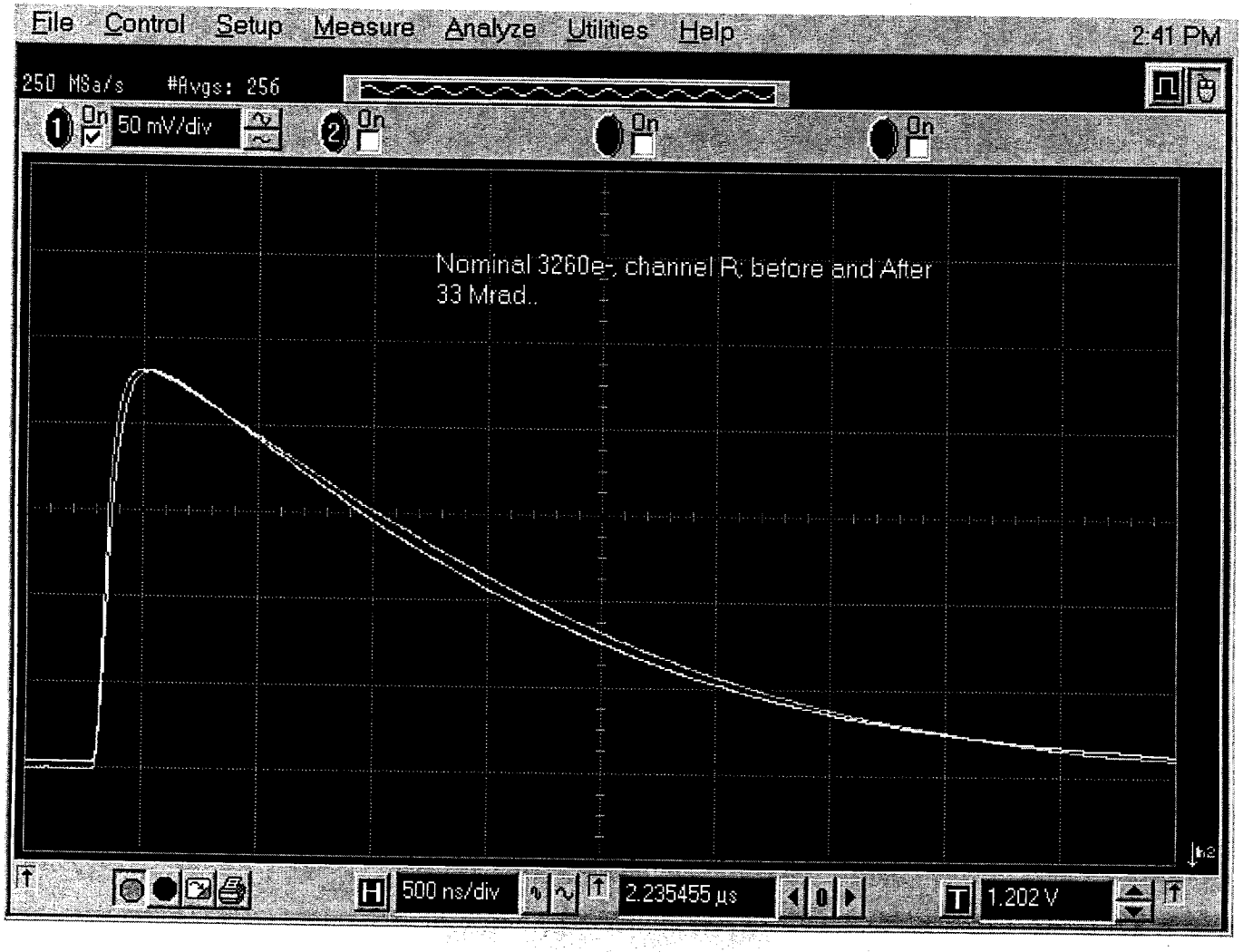
pmos leakage current does not increase (glass charges +; doesn't induce a p-channel).

Rad-hard nfet layout (very schematic!)

"gate all around" layout prevents leakage current
(guard rings to prevent latchup not shown)

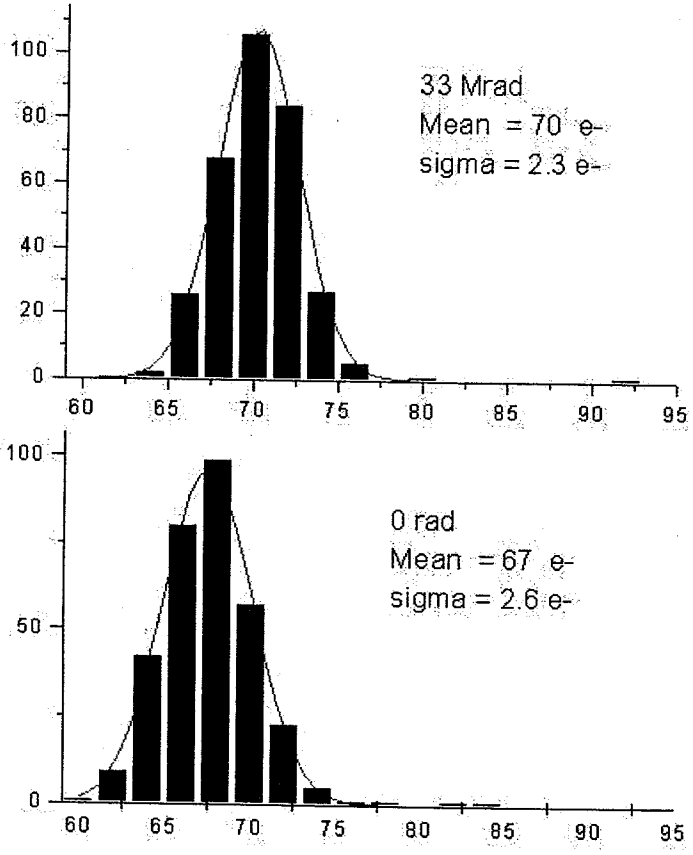


preFPIX2 total dose tolerance – ^{60}Co exposure (33 Mrad ~ 10^{15}/cm^2)



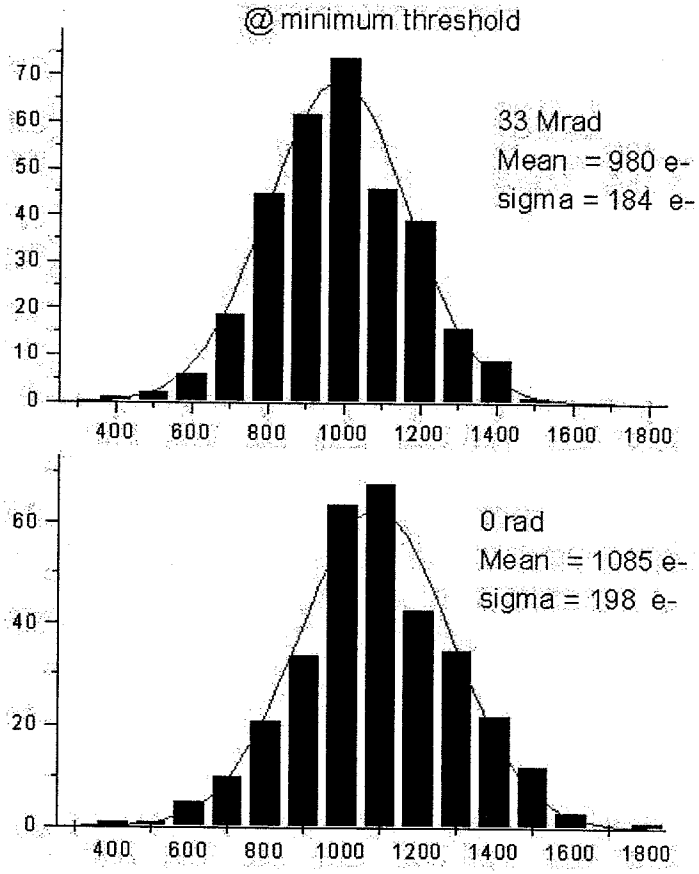
(pre)FPIX2 Noise and discriminator threshold distributions

NOISE DISTRIBUTION vs DOSE



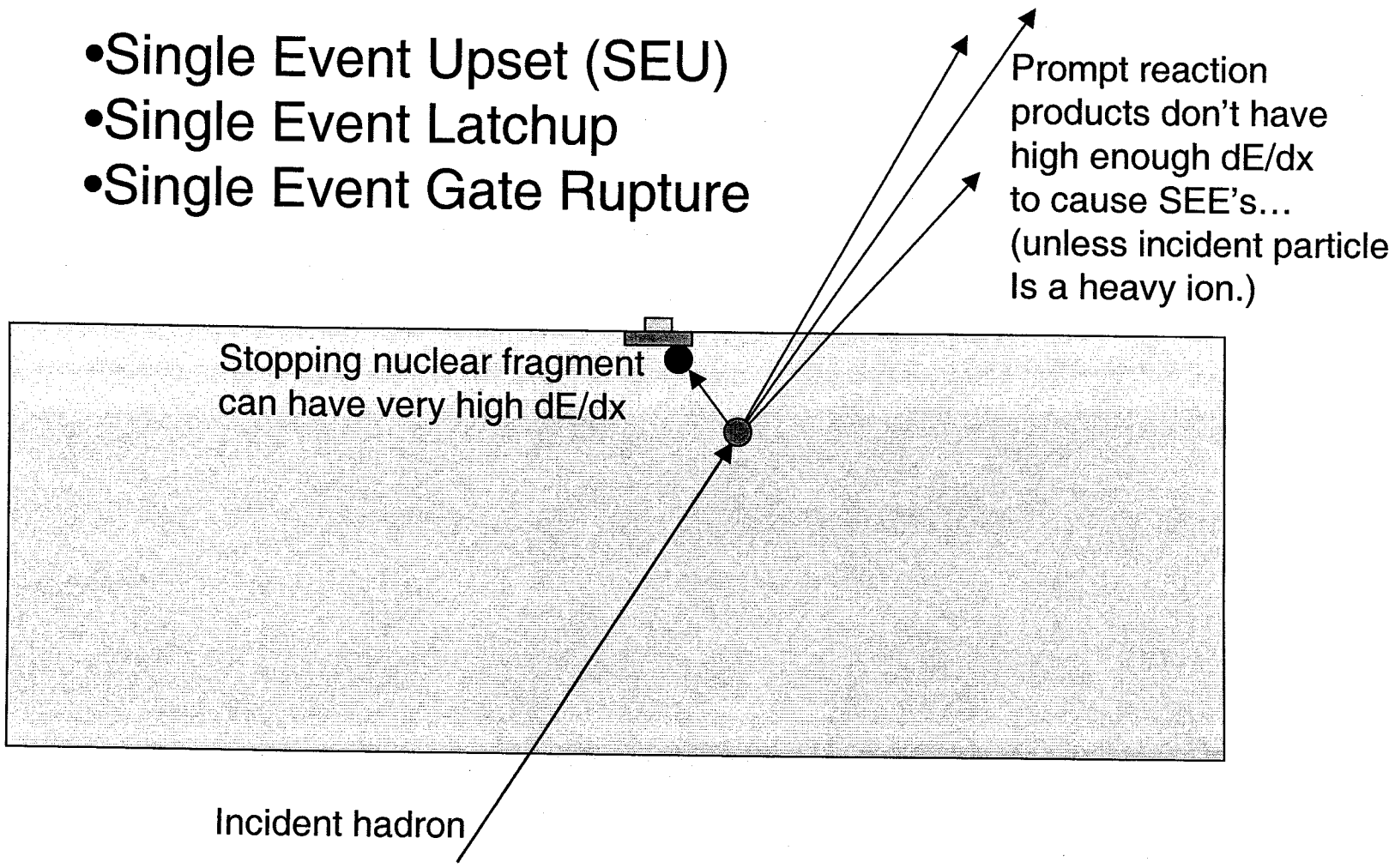
THRESHOLD DISTRIBUTION vs DOSE

@ minimum threshold



Single Event Effects (SEE)

- Single Event Upset (SEU)
- Single Event Latchup
- Single Event Gate Rupture



First CERN proton exposure of a prototype 0.25μ pixel chip demonstrated radiation hardness.

However, a few channels had much higher noise after irradiation than before --- possibly due to gate rupture??? (only measured after ~12 hour annealing period – chips broken)

12/2000 preFPIX2 200 MeV proton irradiation at IUCF
→no noise increase (in a large number of channels) after ~5E14/cm^2 and 6 weeks annealing.
→ No significant rate of gate rupture.

April, 2001 exposure of preFPIX2 to 200 MeV protons:

SEU cross sections measured for two types of flip-flops

Cross sections are small enough that no special circuitry is required for BTeV operation – registers will be monitored & errors corrected as required (~1/hr).

Results: SEU cross sections

$$\sigma_{\text{shift-register}} = \frac{53 \pm \sqrt{53}}{2.33 \cdot 10^{14} \frac{p}{cm^2} \cdot [2 \cdot 18 \cdot 32]} = (1.97 \pm 0.3) \cdot 10^{-16} cm^2$$

$$\sigma_{DAC} = \frac{10 \pm \sqrt{10}}{2.33 \cdot 10^{14} \frac{p}{cm^2} \cdot [14 \cdot 8]} = (3.8 \pm 1.2) \cdot 10^{-16} cm^2$$

N.B. the uncertainty in the integrated fluence is less than 10%