# Errata <br> Title \& Document Type: 2401C Integrating Digital Voltmeter Operating and Service Manual 

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## QUICK REFERENCE INDEX

To locate desired data quickly, bend the handbook back to expose the index marks on the first pages of all the sections. These marks correspond to data identification marks on this page. The detailed contents of Sections 1 through 4 are listed individually just before the first page of each section.


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## SECTION I GENERAL DESCRIPTION

## 1.1 .. BASIC CAPABILITIES

The HP-2401C Integrating Digital Voltmeter is an all solid state electronic instrument which measures de potentials up to $\pm 1000$ volts. The lowest of the instrument's five decade multiple voltage ranges is a $\pm 0.1$ volt range that permits high-resolution miliivolt measurements. In addition to voltage measurements, the HP-2401C is capable of frequency measurements from 5 Hz to 300 kHz . Measurements are indicated on a direct reading 6 digit display that is accompanied by an identification display of the units being measured and input polarity.

The measurements and units are made available in 4-2'-2-1 binary-coded decimal (bcd) for recording by a digital printer or for further digital data processing. Other capabilities may be added to the standard instrument in the form of various accessories and modifications which are discussed briefly in Sections 1.4 and 1.5.

### 1.2 FUNCTIONAL DESCRIPTION

Basically, the Hp-2401C consists of a precise input attenuator, a highlys accurate, highly-linear voltage-to-frequency converter (vfc) and a frequency counter. The vfc has separate outputs, one produced in response to positive input, the other produced in response to negative input. The frequency counter counts the pulses from the vfc for one of three specific sample periods, producing a count that is directly proportional to the average input voltage to the HP-2401C. The sample periods of the HP-2401C, $.01,: 1$, and 1 second, are produced by decade division of the output from a 100 kHz reference oscillator. The counter can be used alone for frequency measurements, as noted previously.
<

### 1.3 DESIGN FEATURES

### 1.3.1 Averaging of Posifive and Negative Excursions

During voltage measurements, the decade counters in the HP-2401C can count either up or down under the control of special logic -- averaging the positive and negative excursions of the input algebraically. Regardless of the polarity of the input; the counters count up initially. Reversal of the input polarity switches the counters to a down count. At the down count of zero, the counters are switched to counting up and the polarity logic is switched. The count at the end of the samplesperiod is the algebraic sum of the voltage-time integrals of the positive andinegative signals tagged with the signal polarity that has the greatest voltage-time integral.

### 1.3.2 Noise Rejection

The HP-2401C design vtrtually eliminates voltage measurement errors caused by extranedis noise. This is accomplished without imposing any restrictions on the grounding of the signal source or the grounding of any interface equipment. The greatest noise rejection is achieved by using a floating and guarded vic that eliminates common mode noise. Further noise rejection is achieved by the input averaging design of the HP-2401C. Combined, these techniques yield an effective nojse rejection greater than 140 db ( 10 million to 1) at all frequencies, including dc,
Induced ac ground currents, usually at power line frequency, can generate a potential of several volts between the signal source ground and the voltmeter chassis ground. If not blocked these currents will cause a voltage larger than the signal to appear at the input, resulting in a completely erroneous reading. To prevent this effect, known as common-mode pickup, the HP-2401C features a shield or 'guard' that completely isolates the mea-. suring circuit from the instrument chassis. The guard breaks the common mode loop. With the HP-2401C operated at the ground potential of the sig-' nal source, common mode rejection (defined as tho'ratio between the common mode signal and the spurious voltage it causes; to te superimposed on the signal to be measured) exceeds 120 db at 60 Hz and 160 db at dc with a 'ground leg' impedance of 1000 ohms between the source ground and the low side of the voltmeter input. The combined effect of guarding and ayeraging is such that a bommon mode potential of 100 volts will not cause a discernible error in the HP-2401C reading.

To reduce superimposed noise, the HP-2401C, by means of active integration, reads the average value of the applied voltage over a fixed sample period. When the average value of superimposed noise is zero over the selected sample period, no error caused by superimposed rioise appears in the measurement. (See Figure 3-6, a graph of noise rejection versus noise frequency for the fixed sample periods that are provided in the HP-2401C.)

### 1.3.3 Overranging

Overranging to $300 \%$ of full scale is permissible on every range except the 1000 volt range. This provides additional resolution and accuracy on readings that are within the overranging capability. If the instrument is accidentally overloaded beyond $300 \%$ of full scale, the input attenuator is switched automatically to the 1000 /yblt range. This occurs at approximately $310 \%$ of full scale. The overload conctition is indicated on the recording output. The instrument resets automatically when it starts taking the next sample. If the overload condition persists, the protective cycle and overload indication are repeated.

### 1.3.4 Manual Coniral of Display Duration and Satmpling Rete

At the end of the sample period, the display-and recording outputs can be held for a period that is adjustable from 200 milliseconds to 7 seconds.

At the end of this period, the HP-2401C will take a new sample. The sam-ple-hold cycle will repeat inderinitely. The repetition rate of this cycle and the duration of the display period are set by the SAMPLING RATE control on the front panel.

## -1.3.5 Adaptability fo Data Acquisition Systems

To facilitate its use in data acquisition systems, the HP-2401C has been designed to be completely programmable. Programming is accomplishȩd simply by means of external contact closures to ground. The following may be programmed:
a. Measurement function (volts, frequency, or other functions added by accessories or modification of the standard instrument).
b. Voltage range.
c. Sample period.

System cabling is simplified because input, programming, and bed output connections are made at the rear of the instrument. Data acquisition system programming of the MP'2401C can bypass the SAMPLING RATE control on the front pahel. The maximum sampling rates then depend upon selection of the sample period. The . 91 second sample period most frequently used for data acquisition systems permits a maximum of 50 readings per second. ${ }^{1}$ Nine readings per second are possible when the .1 sec ond sample period is selected. This sample period provides the optimum combination of speed, resolution, and accuracy for most measurements. The 1 second period, providing about 1 reading per second,is useful where maximum resolution is required.

### 1.3.6 Control of Sample Period

The input signal can be integrated over one of the fixed sample periods, or over an extended period which may be started manually or by programming. In this way analog signals from transducers car be integrated over any desired time interval, 'permitting totalization of flows, pressures, or other quantities.

### 1.3.7 Self Checking ')

A precision intérnal $\pm 1$ volt reference source is provided for checking the calibration of the HP-2401C. The internal standardits obtained from a specially aged, temperature stabilized Zener diode thitgis selected for less than $0: 006 \%$ drift in 6 months. The provision of this internal standard permits inplace calibration; avoiding frequent unracking and transportation of the instrument to the standards laboratory.

The HP-2401C design also provides for a self check of forward counting and decimal point logic.

### 1.4 CAPABILITIES PROVIDED BY ACCESSORIES

### 1.4.1 HP-2410B AC/Ohms Converter

The HP-2410B AC/Ohms Converter adapts the HP-2401C for resistance and ac voltage measurements. This instrument makes possible resistance measurement on six decade-mulitple ranges from 0.1 K ohms to 10 megohms full scale. AC voltage measurement ranges are the same as the dc ranges of the HP-2401C , except that the input cannot be allowed to exceed 750 volts peak. The HP-2401C includes the $\Omega, \mathrm{K} \Omega, \mathrm{M} \Omega$, and AC displays which indicate the units being measured when the HP-2410B is used with the HP-2401C.

### 1.4.2. HP-24ilA Guarded Data Amplifier

The HP-2411A Guarded Data Amplifier adapts the HP 2401C for low-level, high input.impedance measurements. The HP-2411A (at +10 gain) -HP-2401C (at , 1V range) combination affords a $\pm 10$ millivolt full scale range, with overranging to $\pm 30$ millivolts. At +10 or $+1^{-}$gain, the HP-2411A input impedance is 10,000 megohms (effictive at +1 gain and HP-2401C to $\pm 10$ volts). The HP-2411A bypasses its input directly to the HP-2401C when more than 10 volts is applied. During the time required for switchover to bypass mopde, the HP-2411A will'tplerate up to 300 volts foverload. Correct positloning of the decimal point on the HP-2401C is controlled by decimal logic assembly A30 (supplied with the HP-2411A to be plugged into the HP-2401C.

### 1.5 CAPABILITIES*PROVIDED BY OPTIONS

A variety of standard options to the HP-2401C are available.
These are summarized briefly as follows.
18: Fits the HP-2401C with Zero-Trak C-300-S-20 slides. This facilitates calibration and servicing of rack mounted instruments.

21: Provides positive-true 8-4-2-1 bcd recording outputs instead of the $\overline{4-2^{\prime}}-2-1$ bcd recording outputs supplied by the standard instrument.

29: Allows frequency measurements to 1.2 MHz .
30: Adds period measurement capability. Full scalẹ period of 1, 10, and 100 milliseconds may be measured.

31: Adds automatic ranging capability. The HP-2401C automatically selects the appropriate voltage measurement range on receipt of a read command signal. Maximum time from the read command to the start of the meas-
urement, allowing change from lowest to highest range or vice versa, is 34 milliseconds. The autoranger also controls the HP-2410B AC/Olms Converter or the HP-2411A Guarded Data Amplifier when either is used with the HP-2401C.

35: Provides negative-true 8-4-2-1 bcd recording outputs jnstead of the $4-2$ '-2-1 positive-true bed recording outputs. supplied by the standard instrument.

146: Adapts HP-2401C for single-comector program input from HP computers.

### 1.6 PHYSICAL DESCRIPTION

The HP-2401C mounts in a standard 19 -inch rack and requires 7 inches of vertical panel space. It extends to a depth of 18-3/8 inche's (including the externally-mounted cooling fan). The instrument chassis-is made of, alodined aluminum, and the front panel is finished in lightagrey baked enamel with black-filled engraved titles.

### 1.7 SPECIFICATIONS

## DC VOLTAGE MEASUREMENTS

## NOISE REJECTION

Overall Effective Common Mode Rejection: (ratio of commen' mode signal to its effect on digital dtsplay): 140 db at all frequencies, 160 db at dc ( 0.1 second sample period).

Common Mode Rejection: (ratio between common mode signal and voltage it superimposes on source): 120 db at $60 \mathrm{~Hz}, 160 \mathrm{dh}$ at dc, with 1000 ohms between low side of sofrce and low side of voltmeter input (resistances up to 10 K permisalble).

Superimposed-Noise Rejection: (ratio of superimposed noise to its effect on digital display): More than 20 db at 55 Hz for 0.1 second sample period; increases 20 db per decade incr rase in frequency. Infinite rejection at frequencies evenly divisible by 10 . (For 1 second and 0.01 second sample periods see Figure'3-6.) Combined amplitude of signal and superimposed noise can equal $\pm 3$ times full scale, for any signal amplitude.

INPUT CIRCUIT
Type: Floated and guarded signal pair. Signal pair and guard may be operated up to 500 v above chassis ground.
Ranges: 5 ranges from 0.1 to 1000 v full scale (see also 'Resolution' on page 1-6). $\quad 10 \mathrm{mv}$ range , with accessory HP-2411A Amplifier. Range selection by front panel switch or remote circuit closure to ground. See page 1-6 for specifications of optional Autoranger. Signal polarity sensed automatically.
Overranging: Overranging to $300 \%$ of full scale permissible, except on 1000 v range. Attenuator switches automatically (in 3 ms ) to 1000 v range if overload exceeds $310 \%$. Reset automatically by next internal or external read command signal.:
Input Impedance: 10 M on $10,100,1000 \mathrm{v}$ ranges. $\overline{1 M}$ on $1 v$ range. 100 K on 0.1 v range. Impedance is within $\pm .02 \%$ of nominal value, all ranges. $<150$ pf all ranges. '.
Connectors: Front pajuel binding posts ( $3 / 4$ inch centers) for $\mathrm{HI}, \mathrm{LO}$ and GUARD. Alternate input via guarded comector on rear panel.

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## meiculact OUTHIT

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EXTERNAL PROGRAMMINO
HP 2401C may be completcly programmed by external circuit closures to ground (defined as contact closure or equivalent that ralses internal circuit to -Iv or more positive level and that can supply uprto 70 ma ). For maximum sampling speed, pulse input may be used for reset/encode command. Unless otherwise stated, all programming commands are received via rear MS3102A28-218 37-pin connector.

Function: HP 2401C measures voltage unless closure is received on 'frequency' command line.

Range: Separate closure required to select any of the Iive voltage ranges. Range select time $<6 \mathrm{~ms}$.

Sample Period: Separate closure required to select any of the three fixed sample periods or to activate 'manual' control. When 'manual' control is activated, closure (or -1 to +5 v ) on 'start/stop' line starts sample period, open circuit (os -5 to 30 v ) stops sample period. '(Input resigtance 4 K .) sample period starta/stops within $1 \mu \mathrm{~s}$ of command.
*
Reset (Encode): Counter portion of HP 2401C may be reset and new count started by closure on 'Counter Reset' IIne, or counter may be reset by $-15 \mathrm{v}, 25 \mu \mathrm{~s}$ pulse (rise time $<2 \mu \mathrm{~s}$ ) applied to separate rear BNC (not avallable with 146). Fixed delay of 12.7 ms to start of new count with closure reset, 9.7 ms with pulse reset.
Hold: Positive 1 to 12 v ( 4.5 ma , max.) inhlbits start of new count. Negative 1 to 35v permite new count. Received via recorder (bod) output connector.

Accessory Amplifier: When used with HP 2411A Amplifier, decimal point togic card furnished with the $\mathbf{2 4 1 1 A}$ must be Ingtalled in the 2401C.
AC/Ohms Meagurements: Uf used with HP 2410B AC/ Ohms Converter, coupling cards supplied with 2410B must be instatled in the 2401 C . External programming, except pulse'encode command, is accomplished through 2410B.

## OPERATINO CONDITIONS

Ambient temperatures 10 to $50^{\circ} \mathrm{C}$, relative humidity to $95^{\circ} \mathrm{r}$ at $40^{\circ} \mathrm{C}$.

## POWER REOURED

$115 / 230 \mathrm{v} \pm 10^{\sigma} \%, 50$ to $60 \mathrm{Kz}, 150$ watts approx.
WEOMT
Net wt. $48 \mathrm{lb}(22 \mathrm{~kg})$; shipping wt. $87 \mathrm{lb}(25,7 \mathrm{~kg})$. PANEE FINISH
Wght grey baked enamel, black-filled lettering.

OPTIONS
18. Rack-Mounting Slides: HP 2401C fitted with-Zero-Trak C. 300-5-20 slides for eesy withdrawalfrom rack.
21. +8-4.2-1 BCD Output: Supplied instead of standard +4-2-2.1 output (same speciflcations). Required for compatibility with Hewiatt-Pecteard Coppputers.
29. 1 MHz Frequency Range: Extends frequency massurgment range to 1.2 MHz .

30. Period Measurements: Adds memsurement of multiple period sereges of signals to 10 kHz . Specifications on pege 1.7.
31. Autoranging: Specifications on page 1-6.
35. -8-4-2-1.BCD Output: Sppplied inftead of star (dard +4-2-2-1 output (same specificetions exce.t ' 0 ' and/' 1 ' state levels reversed).

146. Programming by HP Computers: Adepts 2401C for singleconnector program input from HP Computess. Provided in place of rear 'Counter Reset' ENC. Option 21 biso required.

## ACCESSORIES AVAlLABLE

(Oirder by accessory orustock number.)

1. H006 5050A Digital Recorder. Check with local Hewlett-Packard sales office for appropriate options, price, and delivery.
2. J66/65 562AR Digital Recorder. Check with local Hewlett-Packard sales office for appropriate options, price, and delivery.
3. 2547A Coupler. Offers a choice of several different serial-entry output recorders, including magnetic tape, punched tape, punched cards, and typed los. Check with local Hewlett-Packard sales office for appropriate options
4. Prógramming Input Connector. MS3106B28-21P, 37-pin (with clamp) stock number 5060-2440
5. Recorder Output Connector: Amphenol 57-30500, stock number 1251-0088
6. Input Connector. Mates with rear guarded Input connector, stock number 1251-0350
(One connector is furnished with instrument.)
7. Cover. Plugs onto front inpat terminals to prevent their use when rear input is in use. Accessory number 12529A

## ACCESSORIES FURNHSHEP

1. Power Cable. Length 7-1/2 feet, plugs into rear connector. stock number 8120-0078.
2. Input Connector. Mates with rear guarded input connector. Slock number 1250-0350.
3. Extender Boards. For servicing plug- In circult boards. Set of five. Stock number 5060-5078.


## INSTALLATION AND OPERATION

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## SECTION II installation and operation

### 2.1 INSTALLATION

The HP-2401C Integrating Digital Voltmeter mounts in a standard 19 -inch rack, requiring 7 inches of vertical panel space, and is also suitable for bench-top use. "Depth required behind the front panel, including recommended cable clearances, is $21-3 / 8$ inches. The HP-2401C contains its own cooling fan. No special ventilation is required unless the temperature of the instrument would otherwise be outside the range of $10-50^{\circ} \mathrm{C}$ or relative humidity would otherwise exceed 95 percent.

### 2.1.1 Line Sef 5 wifh and Power Requirements <br> - A slide switch on the rear panel allows the HP-2401C to be set for operation from either 115 or 230 -volt power, at 50 to 60 Hz , without rewiring the primary connections of the power transformer. The HP-2401C is normally supplied from the factory with the line set switch in the 115 volt position and a 2 ampere slow-blow fuse installed in the fuseholder on the front panel. Power required is approximately 150 watts.

## CAUTION

Before operating the HP-2401C, make certain that the line set switch is positioned correctly. Slide this switch to expose 115 for operation from 115 volts or to expose 230 for operation from 230 volts. For 230 -volt operation. replace the 2 ampere slow-blow fuse with a 1 ampere slow-blow fuse.

### 2.1.2 Input, Output, and Programming Connectors

$\frac{\mathrm{HI}, \mathrm{LO} \text {, and GUARD: Binding post terminals on the front panel. The HI }}{\text { and }} \mathrm{LO}$ termingie rec and LO terminale receive the two-wire dc input voltage; the GUARD terminal (connected internally to the guard chasais) receives the reference potential of the measurement source. The signal pair and guarid may be operated up to 500 volte above chassis ground. See Figure 2.1 for input signal connections.

If guarding is not used, the GUARD terminal must be connected to the Lo terminal. For example, when measuring a floating dc voltage -- such as the output of a floated dc amplifier -- do not connect GUARD to the chassis ground of the amplifier; connect the GUARD terminal to the LO terminal.

## CAUTION

Do not connect voltage to the HI and LO terminals when plug is connected to J31. Voltage thus applied can damage any instrument whose output is connected to the HP2401C via 331.

DC INPUT (J31): A special guarded receptacle on the rear panel. Pins $A$ and $B$ connect to the HI and LO dc input lines. The oval shell connects to guard.

FREQ INPUT: Front and rear panel paralleled BNC receptacles, either of which may receive the input signal whose frequenicy is to be counted when the HP -2401C is used for frequency measurethent.

100 Hz STD OUTPUT/INPUT (J3): Rear panel BNC receptacle that provides an output of the internal 100 kHz time base for external use, or receives a precise external time base input if desired. An associated toggle switch labelled INT-EXT selecte the internal or external time base mode.

COUNTER RESET (J4): Rear panel BNC receptacle which receives an external pulse that is used to reset the counter section of the voltmeter.

PROGRAM CONTROL (J1): Rear panel MS3102A28-218 receptacle that receives the external program commands when the HP-2401C is programmed by external circuit closures to ground, as in data acquisition systems. (See Section 2.6.) Also receives program commands from a HP-2410B AC/Ohms Converter or HP-2411A Guarded Data Amplifier when either of these instruments is used with the HPL2401C. (See Sections 2.5.3 and 2.5.4.)

BCD OUTPUT (J2): Rear panel Amphenol 57-40500 receptacle that provides bed outputs for function, data, and range, + and -bed reference voltages, and + and -print commands. It also accepts holdoff signal and scan signal from recorder or coupler (scan signal is routed to PROGRAM CONTROL connector).

### 2.1. 3 HP-2410B AC/Ohms Converter Coupling Cards

When the HP-2401C is used with á HP-2410B AC/Ohms Converter, the two coupling cards (printed circuit boards) supplied with the HP-2410B must be installed in the voltmeter. (If a HP-2410B/HP-2401C combination is purchased, the coupling cards are installed in the voltmeter at the factory.)

The two printed circuit boards are the HP-2410B Units Coupling (A9) and AC/Ohms Delay Gate (A23). Install HP-2410B Units Coupling Card (A9) in connector XA9; AC and Ohms Delay Gate Card (A23) in connector XA23. These locations are shown in Figures 4-3 and 4-4.

### 2.1.4 HP-2411A Guarded Dafa Amplifier Decimal Point Logic Card

When the HP-2401C is used with a HP-2411A Guarded Data Amplifier, the HP-2411A Dfeimal Point Logic Printed Circuit Card (A30) supplied with the HP-2411A must be installed in the voltmeter. This gasures correct positioning of the decimal point when the HP -2411A is set for +10 gain . (if a HP-2401C/HP-2411A combination is purchased, A30 is ingalled in the voltmeter at the factory -- see Figure 4-4.) When the HP-2401C is purchased
separately, a jumper board is installed in the A30 position. HP-2411A Decimal Point Logic Card A30 replaces this jumper board in receptacle XA30.

### 2.2 PREOPERATIONAL CHECK AND CALIBRATION

To achieve the specified measurement accuracy, perform the following preliminary checkout and calibration procedures daily, or each time the instrument is turned on. Allow in 1-1/2 hour warmup.

### 2.2.1 Counfor Section Chock

a. Set Power switch to ON, other controls as follows:

100 KC STD (rear panel): INT. FUNCTION: $\quad$ FREQ.
ATTENUATION: CHECK.
SAMPLING RATE: CW from STOP.
b. Check reading at each of the three fixed sample periods in turn;readings should be as follows ( $\pm 1$ count):

Sample Period:

$$
\begin{array}{cccc}
.01 & \text { Sec, } & 10.0 & \text { KC Reading } \\
.1 & \text { Sec, } & 10.00 & \text { KC Reading } \\
1.0 & \text { Sec, } & 10.000 & \text { KC Reading }
\end{array}
$$

### 2.2.2 ZERO Adjustment (After 1/2 Hour Warmup)

a. Set Power switch to ON , note time, and set other controls as follows:

100 KC STD (rear panel): INT.
FUNCTION: . VOLT.
RANGE:
SAMPLE PERIOD:
SAMPLE PERIOD: $\quad / \quad 1$ SEC
SAMPLING RATE:
ZERO.
b. After the HP-2401C has been on for at least 1-1/2 hours, set the front panel ZERO adjustment for zero $\pm 1$ count readout on the digital display.

### 2.2.3 Full-Scale Adjustment (After ZERO Adjustment)

a. Set the RANGE switch to $\operatorname{NT}+1 \mathrm{~V}$.
b. Set the front panel CAL+ adjustment for +1000.00 MłLLIVOLTS indication on the digital readout.
c. Set the RANGE switch to INT -1V.
d. Set the front panel CAL- adjustment for 1000.00 MLLIVOLTS indication on the digital readout.

### 2.3 LOCAL OPERATION

Operation of the HP-2401C is straightforward and can be controllod locally at the front panel per Table 2-1 or can be programmed as required for data acquisition systems use. (See Section 2.6 for programmed operation.)

### 2.4 FUNCTIONS OF CONTROLS

### 2.4.1 Froni Panal Controls

FUNCTION switch: Selects the type of measurement to be made, such as VOLT for dc voltage measurements, AUTO RANGE for automatic ranging voltage measurements (with HP-2401C-31), FREQ for frequency measurements, or PERIOD for period measurements (with 4 LP -2401C- 30 ). An EXT SEL position prepares the HP-2401C to respond to function and range programming via PROGRAM CONTROL connector $\mathbf{J} 1$.

RANGE switch: ${ }^{2}$ Selects the full-scale range of . 1, 1, 10, 100 , or 1000 volts. INT +IV, ZERO, and INT -1V positions are also provided for datly calibration of the instrument.

SAMPLE PERIOD switch: Fixed sample periods of $.01, .1$, or 1 second are selected by this switch. In addition, the sample period may be started manually by switching to START position and ended by switching to STOP. An EXT SEL position allows programmed selection of a fixed sample period or programmed starting and stopping of the sample period.

SAMPLING RATE control: Adjusts the length of time that the display and recording outputs are held after the end of the sample period. The time is adjustable from 200 milliseconds to 7 seconds (approximately). When switched to frop position, the reading is held until reset either manually or by progr ming. Programmed control can achieve up to 50 readings -per second, as noted in Section 1.3.5.

RESET pushbutton: Resets the instrument, including the digital'display, and automatically initiates another sample period if one of the three fixed sample periods is selected and the SAMPLING RATE control is in STOP position. With SAMPLE PERIOD switch at STOP, resets the instrument to zero; sample period begins when SAMPLE PERIOD switch is set to . START.
ATTENUATION control: Determines the input signal attenuation when making frequency or period meagirements. A switched CHECK position connects a 10 kHz signal derived from the internar time base oscillator to the counters. This is used for a confidence check of the counter section.

Power switch and Line fuse: Controls ac power to the voltmeter; 2 am-

### 2.4.2 Rear Panel Conirols

STORE/DISPLAY DURING COUNT switch: In the STORE position, the previous visual display is held until the end of the current sample period, at which time the display changes directly to the new reading. However, external encode commands or RESET switch triggering causes transfer of all zeros to the digital display at the start of the triggered sample. In the DISPLAY position, the actual counting is displayed during the sample period
100 KC STD switch: Selects the source of the counter time base reference standard. The INT position of this switch selects the internal 100 kHz time base signal and connects it to the adjacent 100 KC STD INPUT/OUTPUT BNC connector J3. The EXT position selects an external signal, recelved via BNC connector J3, as the time base standard of the instrument.

115/230V switch: Sets the instrument for operation from available line voltage (115 or 230 vac; 2 ampere fuse is used for 115 vac operation, 1 amp ere fuse for 230 vac operation).

Table 2-1. Operation Summary (Std. 30, 31 Instruments)

## TURN-ON AND PRELIMINARY CONTROL SETTINGS

a. Set Power switch to ON (display digits light).
b. Set 100 KC STD switch to INT (EXT if external standard is to be used).
c. Sft SAMPLING RATE for desired display interval or to STOP for measurement triggering by RESET pushbutton or remote command.
d. Select SAMPLE PERIOD that achieves the desired resolution of measurements (see Table 2-2).

## VOLTAGE MEASUREMENT

a. Sét FUNCTION switch to VOLT (VOLT or MILLIVOLT display lights).
b. Select lowest RANGE that can be used without lighting the OVERLOAD display.

AUTORANGING VOLTAGE MEASUREMENT (HP-2401C-31)
a. Set FUNCTION switch to AUTO RANGE.
b. Set RANGE switch to any position except INT +1V, INT -1V, or ZERO.

FREQUENCY MEASUREMENT
a. Set FUNCTION switch to FREQ (KC display lights).
b. Adjust ATTENUATION control clockwise about $30^{\circ}$ past the point where consistent measurements are obtaifed.

PERIOD MEASUREMENT (HP-2401C-30)
a. Set FUNCTION switch to PERIOD (MILLISEC display lights).
b. Adjust ATTENUATION control clockwise about $30^{\circ}$ past the point where consistent measurements are obtained.

CONNECTIONS
a. Connect voltage to bé measured and shield to HI, LO, and GUARD terminals per Figure 2-1.
b. Cpunect signal whose frequency or period is to be measured to FREQ INPUT receptacle per Figure 2-1.
'Pabla 2-2. Jlasalullon of Manauramonta

| Bample Poriod | mangui | Full-Pksulo Reanding | Maximum Ovarrango Neadhes | Premuencey llaudlns | parlode Avoraged* |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 18 BICC | $\begin{array}{r} .1 \mathrm{~V} \\ 1.0 \mathrm{~V} \\ 10.0 \mathrm{~V} \\ 100.0 \mathrm{~V} \\ 1000.0 \mathrm{~V} \end{array}$ | $\begin{aligned} & 100.000 \mathrm{MV} \\ & 1000.00 \mathrm{MV} \\ & 10,0000 \mathrm{~V} \\ & 100.000 \mathrm{~V} \\ & 1000.00 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 900.000 \mathrm{MV} \\ & 3000.00 \mathrm{MV} \\ & 90.0000 \mathrm{~V} \\ & 900.000 \mathrm{~V} \\ & -2-6 .-\ldots- \end{aligned}$ | $000.000 \mathrm{KC}$ | $\begin{aligned} & \quad 100 \\ & \left(i^{\prime} / 1\right. \text { Bos } \\ & \text { Ramolution }) \end{aligned}$ |
| . 1 BIEC | $\begin{array}{r} .1 \mathrm{~V} \\ 1.0 \mathrm{~V} \\ 1.0 .0 \mathrm{~V} \\ 100.0 \mathrm{~V} \\ 1000.9 \mathrm{~V} \end{array}$ | $\begin{aligned} & 100.00 \mathrm{MV} \\ & 1.0000 \mathrm{~V} \\ & 10,000, \mathrm{~V} \\ & 100.00 \mathrm{~V} \\ & 1000.0 \end{aligned}$ | $\begin{aligned} & 900.00 \mathrm{MV} \\ & 3.0000 \mathrm{~V} \\ & 90.000 \mathrm{~V} \\ & 300.00 \mathrm{~V} \\ & \ldots \end{aligned}$ | $0000.00 \cdot K C$ |  |
| . 01 SEC | $\begin{array}{r} .1 \mathrm{~V} \\ 1.0 \mathrm{~V} \\ 10.0 \mathrm{~V} \\ 100.0 \mathrm{~V} \\ 1000.0 \mathrm{~V} \end{array}$ | 100 O MV 1.00 V 10.0 V $1000 . V$ $1000 . V$ | $\begin{array}{r} 300.0 \mathrm{~V} \\ 9.000 \mathrm{~V} \\ 90.00 \mathrm{~V} \\ 900.0 \mathrm{~V} \\ \hdashline \end{array}$ | $00000.0 \mathrm{KC}$ | $\begin{gathered} 1 \\ (100 \mu \mathrm{Boc} \\ \text { Romplution) } \end{gathered}$ |

* HP 2401C-30.


### 2.5 SPICIAL OPEİATINO CAPABILITIES

### 2.5.1 Operallon Wifh ixidrnal Time Base Deference

Aćcurate extermal $10 \mathrm{kHz}, \mathrm{kHz}$, or 100 Hz , redronces can be utad to achleve multiplicrition of the fixed armple poriods of the linatrumont by 10,100 , or 1,000: If sueh sample periodemultiplication is ueod, tho decimal point must be shilfted ono, two, or threo places to the left. Bwitchoper to the extornal atandard algnal is accomplishod by motting the 100 KC ETD awitch to EXT and connocting the alandard algnal to the 100 KC BTD INPUT/OUTPUT rocoptacle at tho rear of the inatrumont. Thin oxtornal algnal must have 2 volt peak-topoak amplitude across a 1.2 K load.

### 2.5.2 Manual Conirol of Sample Perlod

Duratign of the sample perlod (counter gate timo) can be controlled manually, as follows:

- a. Set the SAMPLE PERIOD awitch to STOP and rebet tho counter by actualing the IRESET pushbutton.
b. Set the BAMPLEE PERIOD ' B witoh to START.
c. End the sample pertod by belling the SAMPLE PErfiOD switch to Srop.

When a manually started and atopped sample period ts used, flows, pressures, thrusts, countable ovents, etc., can be totalized over periods that are lonyor than the fixed periods selectable on the SAMPLE PERIOD switch. Avorage voltuge or frequency may be determined bly dividing the reading by tho duration (in seconds) of the extended sample period.
NOTE: The counting process is always displayed while the SAMPLE PERIOD awitch is in START or STOP position, regardless of the STORE/DISPLAY

### 2.5.3 AC Volfage Mogsuromonis and Roslatance Meggurements

TheriP-2410B AC/Ohma Converter makes posalble ac voltage and realatance measuremente with the HP-2401C. Aseemblies A9 and A23, oupplied with the HP-2410B, muat be installed in thip HP-2401C. Specified accuracy of the HP-2410B is achieved after 1 hour warmup; but it can beed 15 seconde after it is turned on.

Infual Preparation
a. Connect the HP-2410B programming cable from receptacle 18 on the rear of the HP-2410B to PROGRAM CONTROL receptacle $J 1$ on the rear of the HP-2401C.
b. Connect the HP-2410B aignal output cable from the HI, LO, and GUARD dc terminals on the terminal strip at the rear of the HP-2410B to correaponding terminale on the HP-2401C.
NOTE: To avoid unnecessary measurement errors, make certain that the guard atheld is connected at only one point, the measurement reference pofnt. If a GUARD terminal is tied to a LO terininal at the front pants of the HP-2410B, make certaln that such connection is not duplicated between GUARD and LO terminals at the rear of the HP-2410B or at the front panel dr the HP-2401C.
c. Turn on both inatrumente and set HP-2401C FUNCTION switch to EXT SEL, SAMPLE PERIOD awitch to desired position, SAM PLING RATE COltrol to STOP, and RANGE awitog to IV.

AC Voltage Meacurement
a. Set HP-2410B FUNCTION swth to AC NORM for frequencies below 400 Hz or AC FAST for frequencles abpve 400 Hz ; set HP-2410B RANGE awitch to loweat range that can be used without lighting OVERLOAD Indicator on HP-2401C.
b. Connect ac voltage to HI, LO, and GUARD AC/DC INPUT of HP-2410B, but do not exceed 750 volt peak input.
c. Initiate meacurements by actuating the RESET pushbutton on the HP2401C or by eetting SAMPLING RATE control clockwise from STOP.

## Realatance Meafurement

a. Perform the HP-2410B ohms zero calibration as specified in the HP2410B handbook.
b. Set ,HP-2410B FUNCTION awtch to OHMS and RANGE switch to the loweat range that can be used without lighting OVERLOAD indicator on HP-2401C.
c. Connect resiatance to be measured to the resistance input of the HP-' 2410B.
d. Initiate measurements by actuating the RESET puahbutton on the HP2401 C or by eetting the SAMPLING RATE contral clockwise from STOP.

Measurements Using the MP-2411A Guarded Defa Amplifier
The HP-2411A Guarded, Data Amplifier makes possible measurement of lowlevel inputs at a full-scale sensitivity of 10 millivolts with the HP-2401C. This instrument may also be used for extremely high input impedapce measurements at +1 gain on the .1 and 1 volt ranges of the HP-2401C Assembly A30, supplied with the HP-2411A, must be installed in the HP-2401C. To achieve specified zefo drift, the HP-2411A requires a 2 hour warmup, at constant temperature, but it can be used 15 seconds after it is turned on. Proceed as follows:
a. Connect the HP-2411A programming output cable from PROGRAM OUTPUT receptacle J2 on the HP-2411A to the PROGRAM CONTROL receptacle $J 1$ on the rear of the HP-2401C.
b. Connect the HP-2411A signal output cable from OUTPUT receptacle $J 5$ on the HP-2411A, to the DC INPUT receptacle, J81, on the rear of the HP-2401C.

NOTE: To avoid unnecessary measurement errors, make certain that the guard shield is connected at only one point, the meamurement reference point. Moize certain that the guard sheld is connected at the measurement cource reference point and that the GUARD and LO terminals on the front panels of the HP-2411A andHP-2401C are not tied together.
c. Turn on both instruments and set the HP-2411A ZERO adjustment as specified in the HP-8411A handbook.
d. Set the HP-2401C FUNCTION switch to EXT SEL, SAMPLE PERIOD switch to desired sample period, and SAMPLING RATE contral to STOP.
e. For maximum resolution of low-level measprements, set the HP-2411A MODE switch to +10 gain and the HP-2401 C RANGE switch to . IV. This achieves a $\pm 10$ millivolt full-scale range ( $\pm 00$ millivolt overrange).
f. For minimum londing of the voltage being measured, et the HP-2411A MODE switch to +1 gain. The input resistance will then be 10,000 mogohme for input voltages to $\pm 10$ volts. Input greater than 10 volts automatically switches the HP-2411A to bypass mode, which reduces input impedance to that of the HP-2401C.
g. Connect the dc voltage to be measured to the HI, LO, and GUARD INPUT terminals of the HP-2411A in accordance with the general principle expressed in Section 2.1.1 and Figure 2-1.
h. Initiate measurements by actuating the RESITT pushbutton on the HP2401 C or by setting the SAMPLING RATE contral clockwise from STOP.

### 2.5.5 Pulse Mecsurements

To measure pulsed at the FREQ INPUT connectors, the input trigger circuit must be adjusted so that the hysteresis limits will be triggered by either a positive pulse or a negative pulse. Refer to Section 4.7.11 for the adjustment procadure. Refer to Section 4.7.12 to readjust for sine wave operation.

### 2.6 PROCRAMMIED OPRAT1ON

The measurements described in Sections 2. 3, and 2.5 may be programmed and initiated by external circuit closures to ground. This feature makes the HP-2401C particularly adaptable for use in automatic data acquisition systems. The remote control lines do not interfere with the guarding properties of the measurement circuits. All programming and input connections can be made at the rear of the instrument, which simplifies cabling.

### 2.6.1 Contrel softings

Set front panel controls of the HP-2401C as follows for fully programmed operation:

FUNCTION:
SAMPLE PERIOD:
SAMPLING RATE: RANGE:

EXT SEL.
EXT SEL.
STOP (switched positioy) or desired rate. Any position except $\mathbb{N} T-1 V$. INT +1V. or ZERO.

### 2.6.2 Programming Requirements

Refer to Table 2-3 for the pins of J1 that must be connécted to program and initiate the various measurements. (An extemnal contact closure to ground is defined as a contact closure or equivalent whigh raises the internal circuit to a potential that is no more negative than 1 volt at a naximum load current of 70 milliamperes.) Complete programming information must be present; for each type of measurement. otherwise the input attenuator switches automatically to the $\mathbf{1 0 0 0}$ volt range and the decimal point blanks. The prorramming required for each type of measurement is as follows:.
DC Voltage Measurements: Only range and sample period must be proyrammed. The HP-2401C automatically measures dc voltage if the frequency measarement function is not programmed.

Autoranging Voltage Measurements (HP-2401C-31 Only): Autoranging function and sample period must be programmed; ranges must not be programhed.
Frequ@gy Measurements: Frequency function and sample period must be programimed.

Period Measurements (HP-2401C-30 Only): Period function and Sample period (number of periods averaged) must be programmed.

### 2.6.3 Application of Pŕogram Commends

The external contact closures are applied between the required pin(s) of $) / 1$ and pin $Z$. For example, to program a frequency measurement over a sample period of 1 second, external contact closures must connect pins $B$ and $R$ of J1 to pin $\mathbf{Z}$.

Table 2-3. Program Control Connector (J1)
Connector Type: MS8102A88-218 Mating Connector: M83106B28-21P


* Pins for HP-2410B use only.
**Overload reset not normally used ance counter resets overload circuit. When counter section is reset, pin d provides overload reset pulse for HP-2410B and HP-2411A overload reset.


### 2.6.4 Inflicting Measurements

Measurement may be initiated by either of two encode command inputs. One of these inputs is a contact closure between pin c of J 1 and pin Z . which grounds the counter reset program line. This triggers a reset pulse after about 3 milliseconds delay, starting a new measurement cycle. The 3 millisecond delay prevents multiple reset commands caused by contact bounce when relay contact closure is used for resetting. The other input which may be used to initiate measurement is a -15 volt, 25 microsecond pulse with rise time less than 2 microseconds. This pulse, applied to COUNTER RESET receptacle J 4 on the rear panel of the HP-2401C resets the digital display to all zeros and starts a new measurement cycle immediately.

### 2.6.5 STandard mocouroment Delays

Measurement (the sample period) actually begins 9 . 7 milliseconds after the reset pulse has reset the time base and counting/ display decades of the HP2401C. AC Normal, AC Fast. or resistance measurements programmed through a HP-2410B AC/Ohms Converter introduce up to 550. 220, or 110 milliseconds additional delay.

### 2.6.6 Programmed Control of Extended Sample Periods

Program periods longer than 1 second as follows:
a. Enable extended sample period programming benconecting pin a of II to pin Z .
b. Start the sample period by connecting pin b of .11 from pin Z .
c. Stop the sample period by disconnecting pin b of Jl from pin Z .
d. Reset the HP-2401C as specified in Section 2.6. 4 before initiating the next measurement.
-Repeat steps a, b, and $c$ of this procedure for each measurement involving angxtended sample period. When extended sample period programming is no longer desired, disconnect pin a of $J 1$ from pin $Z$ and program the cor(rect pin for the desired fixed sample period (.01. .1. or 1 second).
NOTEA: Alternatively, sample periods may be started by a relatively posilive potential ( -1 to +5 volts) and stopped by a negative potential ( -5 to -30 volts) applied through JI pin macros 4 K ת.

NOTE B: The counting process can be displayed during programmed extended sample periods only be setting the STORE' DISPLAY switch to DISPLAY position.

### 2.6.7 Programming Through HP-24108 or MP-2A11A

When using HP-2410B or HP-2411A accessory instrument with the voltmeter. programming must be connected to the accessory instrument. See the applicable handbook for details. This is necessary for correct operation of the HP -2401C logic circuits, particularly the display and decimal point logic. The programming functions applied to the accessory instrument are routed through it to the HP-2401C via the same programming output cable that is used when making manually controlled measurements per Section 2.5.3 or 2.5.4.

Table 2-4. BCD Output Connector (J2)
Connector Type: 57-40500 Mating Connector: 57-30500


* Coding of outputs from HP-2401C-21 or 35; " 0 " and " 1 " state levels from HP-
$2401 \mathrm{C}-35$ are reversed: " 0 " $=-5$ to -1 v and $1 "=-35$ to -24 v .
**Non-hold state is -1 to -35 v .

Table 2-5. Function Codes


### 2.6.8 Overload Resetting

Any overload condition occurring on a previous measurement is reset automatically by resetting the counters per Section 2.6.4. It is also possible to reset an overload condition without resetting the counters. This is accomplished by connecting pin $\mathbf{d}$ of J 1 to pin Z temporarily.

### 2.7 RECORDING OUTPUTS

BCD voltages (ground referenced) are produced for each measured digit and for indication of measurement function (+VDC, -VDC,KC, etc.) and decimal point. These bed outputs are available at the BCD OUTPUT conrector, J2. Pin assignments of J2 are outlined in Tables 2-4 and 2-5.

Also given in Table 2-4 are the bed output weighting and levels, record command output, and bed reference voltages. A hold command may be applied to J 2 pin 22 to inhibit the voltmeter from initiating a new masurement until the recording device has completed $i t s / c y c l e$ or has stored the data. The hold should be used only when the SAMPLING RATE control is used to initiate measurements at an unsynchronized rate. A reset command will reset the DCU's but a new measurement is not initiated until any hold-off command is removed. A voltage to J2 pin 22 that is between +1 and +12 volts (maximum load 4.5 milliamperes) inhibits the counter section of the voltmeter. A voltage to J 2 pin 22 that is between -1 and -35 volts enables the counter section of the voltmeter.

The scan signal and hold command from the recording device are also routed to PROGRAM CONTROL connector J1/tor systems use.

Section III


Figure 3-1. HP 2401C Digital Voltmeter Block Diagram

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# SECTION III <br> THEORY OF OPERATION 

### 3.1 OINIRAL

The functional elemente $\alpha$ the HP-2401C Integrating Digital Voltmeter are illuatrated in Figure 3-1. As indicated, the HP-2401C consists principally of a voltage-to-frequency converter (vfc) and a counter. The vic includea an input attenuator and integrating and-pulse forming circuits. The vic output ta applied to the counter section and an overload detector via a counter control circuit. The counter includea a preciaion time base generator, decade dividers, control logic circuita, and aix reversible counting and display decaden.

### 3.1.1 Volrage Measurement

f Voltage to be measured is applied via the HI-LO input terminals to the programmable input attenuator, which provides precisely caltbrated attequations for flll-scale ranget of $0.1,1,10,100$, and 1000 volts. The GUARD terminal is provided for connecting the vic chassis to the low side of the voltage source. Thus connected, the guard shields the inputa to the vfc, atteruating common-mode noile.

The output from the attenyptor is transformed by the vfc to a proportional pulse rate. The integrating amplifier (-A in Figure 3-1) generates a charf: Ting current for $C$ whose value is directly proportional to the input voltage. This current charges capacitor $C$ to a negative or positive voltage that is . Inverted with respect to the voltage Deing measured. At a specified level, the voltage acrgas $C$ triggers the negative or positive inputs channel. The , pulse from the triggered channel opposes the original amplifier input, discharging capacitor $C$.. At thê end of this pulse, the amplifier output cur-. rent recharges capacitor $C$ to a level hat triggers one of the inputs channels. The average pulse rate thus generrated is directly proportional to the average input voltage. The ofic output pulses are coupled through the couns ler control circuit and the gignal gate to the countin/display decades when the FUNCTION awitch is eet to VOLT. The average vfc output rate is 100 KHz for a full-scale input. Although vfc output pulses are generated contin-c ually whilte an input voltage is connected to the HP-2401C, they are counted only during ample periods.
The counter control circult recelves the pulses from the positive or negative tnpute channel and provides output pulses for triggering the counting/ display decades in the counter section. These pulses are also applied to an overiond detector. In addition, the counter control circuit providea up/ down count commands to the counting/display decader and a polarity signal that lighte the + or -polarity indicator of the digited display during de voltage meaturement.
During each aample period, the counting/diaplay decadea count the pulse - output from the counter control circuit when the aignal gate in opened and

the FUNCTION switch is set to VOLT. The decades count up during the entire eample period if the input polarity does not chande. If the input polarity changes, the counter control circuit changes ite count up command to a count down command. The decades then count down toward zero. If ecro is reached during down counting; the counter control circult changes its count down command to a count up command. At the qame timedtio polarity dieplay is awitchod. At the end of the sample pefiod, the digital dieplay reade out the algebraic average of the applied input voltage, tagged with the correct polarity.

The overload datector alwaya receives a pulse train output from the counter control circuit. If the pulee rate exceeds $810 k$ its ( $810 \%$ of full ecale) at any time, the overloed detector turns on an OVERLOAD indication on the digital dieplay and switches the programmahle attenumbor to its higheat range ( 1000 V ). The overlond detector is reset yit the etart of each new sample period.

### 3.1. 2 Prequency Mocsurement

A signal whoe irequency is to be meamured is applied to the counter gate circuits via an amplitude diecriminator. The amplitude diecriminator consiats of an amplifier and a schmitt Triceer. The amplitude of the amplifier output atgal is bat by the iroat panal ATTENUATION control. The schmitt circult stapes the amplifier output to provide a fact-rise, conctantamplitude atgal for driving the. $10^{\circ}$ counting/dieplay docado. During the aample period this signal ia naplied to the $10^{\circ}$ decade through the aignal gate if the FUNCTION switch is eet to FREQ. Refer to Section 2.5.5 for special pulec measurement requirements.

## 3.1 .3 Sample/Dieplay Peried Control

The sample period of the HP-2401C for voltrge or frequeney meagurements is normally controlled by an output from the time base dividers. However, aumple period can also be controlled manually to atart and atop counting to provide any deaired interval.

The time bace dividere divide the 100 kHis signal from the cryetal-controlled Foforence oacillator by factors of 10 . Thi produces accurate sample iperiods of $0.01,0.1$, and 1 second. The output from the divider that produces the celected aample period is coupied to an AND gate. When this adgnal is present and no inhibit is applied irom the aample rate multivibrator, the gate binary nipa. Thic opens the signal gate and allows voltage or irequency pulees to be counted. The inhibit from the ample rate multivibrator is removed at the end of the dieplay interval. The duration of the inhibit is set by the 8AMPLING RATE control on the front panel.

The pulces from the algnal gate are counted during the selectid cample per- 1 tod. This period is ended by a trigger (firom one of the decade dividera) that flipe the gate binary, cloaing the atonal gate and atopping the count.

The trandition $\alpha$ the gate binary to count lahibit atate triggers the aample rate multivibrator, etarting the deplay interval. During this interval no
new count can be darted. At the and at this interval the reset generator is triggered; which cmices the counting/diepiay aud divider decades to be recet. Then, after a small delay that is provided to allow circuita to stabilize, aignal from the appropriate divider decade initiates a new sample peribod.

### 3.1.4 Display vinins (and Decimel Contrel

The unite readout to the left of the six-digit decimal dieplay indicates the unite being measured (e.g., VOLT8 or KC). This readout position is controlled via logic networke in response to contral eettinge or programming. These logic circuite interpect the various measurement control inputs and cauce the appropriate units to be indicated on the units dieplay. The logic circuits aleo interpret the contral eettinge to determine the correct position for the docimal point indication. This ascures that the display will be direct reading in the units indicated.


### 3.2.1 Proyrammable Aftenueter A23-(Pigure 4-2n

Programmable attenuator aceembly 128 standardizes the current ( 1 microappere full scale) that is applied to aymming point P30 of integrating amplifier Asy. Thus, the vic cutput with 1000 volt input on the 1000 volt range is the aime as with 100 millivolt input on the .1 volt fange.
Attepuation (voltage range of the HP-2401安) is controlled by relays K1 to K5 in aummarized in the RANGE awitch table in Figure 4-29. These relays are controlled by the RANGE switch when the FUNCTION switch is set to VOLT, or by progigmming when the FUNCTION awitch is set to EXT SEL pagition. Range control (a routed through attenuator coupling logic assembly A8 (diecuared in Section (25.1).

## Syetem Operation

3.2.2 Imegreting Amplifigr A31 (Figures 3-2, 4-29, and 4-30) a rate that is proportional to the input current applied to its negatively at P30. This develops an output potential that is continually applied to negative and positive trigger level detectors As2 and Ass. At 0.1 volt, this potential triggers one $\alpha$ the detectors. The polarity and which detector is triggered
are determined by the polarity of the input voltage being measured. For example, negative input voltage causes a positive-going potential that triggers negative trigger level detector A32 at +0.1 volt.

The triggering of A32 or Ass produces a constant area pulse that causes a pulsed current flow to the ramming point which is greater than the input current. Amplified by Asl, this current partly discharges C25. At the end of each such pulse, the input current to the amplifier again causes charging of C25 to the trigger potential. The design of the vic is each that the average of the pulsed discharge currents if equal to the input current and proportional to the voltage being measured. Thus, the pulse rate is proportional to input voltage.

Integrating amplifier Asl consists of an operational amplifier with feedback coupled through C25. The gain of the operational amplifier is 50 high ( $-10^{7}$ to $-10^{\circ}$ ) that the feedback (C25) and input ( $\mathrm{R}_{\mathrm{in}}$ ) impedance determine coperation.

When a dc voltage is connected to the input of the HP-2401C, a mall current, proportional to the magnitude of the input, flows through $\mathbf{R}_{\text {in }}$ to the amplifier. The inverted and greatly amplified output from the amplifier is fed back through C85 as an opposing current. The result is an extremely high integrating amplifier input impedance. Since the current e at the amming point very nearly cancel, the arming point voltage is virtually zero. Thus, the voltage at the amplifier output is that which is developed across C25 as it is charged by the feedback current. This voltage is directly proportional to the integral of the input current. The mathematical expression for the relationship shows that for a step input voltage ( $e_{i n}$ ) the amplifier output ( $e_{0}$ ) increases linearly at a rate that is determined by the constant factors $R$ and $C$, as follows:

$$
e_{0}=\frac{-1}{c} \int i_{\text {in }}\left(d t=\frac{-1}{R C} \int e_{\text {in } d t}\right.
$$

This expression is true for both the measurement input and the reset input to the arming point. The result is the balancing of input current by pulsed reset current, as discussed in the second paragraph under section 3.2.2.

## Internal Functions

The functional elements $\alpha$ integrating amplifier Ai are shown in Figure 3-2. These include a chopper amplifier, a wideband amplifier, the integration feedback circuit, and a non-linear feedback network. The circuit diagram is Figure 4-30.
Chopper Amplifier -- The chopper` amplifier amplifies dc and low frequency signals, after their conversion to ac by a photochopper. Because only ac is amplified, the chopper amplifier introduces no dc drift into the amplifying system. DC drift error caused by the wideband amplifier is divideed by $10^{4}$, the effective dc gain of the chopper amplifier. The resulting drift is so mall that it has no effect upon the' accuracy of the digital readout.



Figure 3-2. Integrating Operational'Amplifier A31, Functional Diagram

The chopper amplifier input and output are modulated and de-modulated synchro, pously by solid-state photoresistors V1-V4 which are driven by Gashes of light from the neon bulbs of a relaxation oscillator. The oscillator frequency is set by the DRIVE OSC ADJ reastor to be 240 Hz , ith power line voltage at 102 or 204 vac. The photochopper mechanical equivghent is shown in Figure 3-2. After filtering, the pulsed signal from demoylating photoresistors V. 3 and V4 is a smooth, amplified and inverted replica of the de and low Irequengy components of the signal at the summing point. The output is cpupled directly to one input of the wideband amplifier. The chopper amplifier output is prevented from exceeding $\pm 0.5$ yolts by CR6 and CR7.
Wideband Amplifier;-- The wideband amplifier amplifies dy and low frequency signal compontints from the chopper amplifier and high Ir equency signal components coupled through C22. The high irequency signal componente are connected to the inverting input of differential input etage Q5-Q8. The output from Qy is amplified without further inversion by Q9-Q12. Complementary push-pull emitter followers Q13 and 214 form a fow-impedance. singleended output atage that has practically equal output inppedance for either output polarity. The output current charges C25 to the frigger level of A32 or As3.

$$
\Rightarrow \quad 1
$$



Gain and response of the wideband amplifier are shaped_by negative feedback from Q10 to QO and from Q13-Q14 to Q11. A filter network in the Q9 base circuit completes the ahaping of response. Overall, the wideband amplifier amplifies input aignals from dc to about 1 megacycle, with a 6 db /ctave rolloff of aignal gain at frequencies above 100 Hz .

Potentiometer R34, the front panel ZERO adjualtment, is set to make zero input current produce zero out put current from the integrating amplifier. It cancels fixed de offeet voltages exiluing within the integrating amplifier by applying a stable equivalent voltage of oppositve polarity to the wideband amplifier de input (the base of ©5).

Non-Linear Feedback Network -- Protection of the amplifier from severe chort-term overloading is provided by non-linear feedback nefivork whose principal elements are voltage breakdown diodes CR16 and CR17. Whenever the amplifier output voltage exceeds the breakdown potential of CR16 or CR17, these diodes conduct a negative feedback current that prevents saturation of the amplifier, which could cause exceastve recovery time.

### 3.2.3 Trigger Level Defecters A32 and A33 (Figure 4-29)

A32 and A3s are voltage-sensitive pulse generators. These detectors are easentially identical, except that one reaponds to negative voltage and the other to positive voltage. Either of these pulse generators provides a constant voltage-time area pulse of a polarity opposite to the polarity of the input aignal.

Operation of detector A3S is typical. When a positive voltinge is being meacored, the potential from the output of Asi increande negatively until it reaches the -0.1 volt trigger level of Ass. The trigger level is met by potentiometer R27. At the trigger level, blocking occillator 03 is triggered through emitter follower ©0, non-inverting amplifier © , and emitter follower ©4. The output from ©s is a charp pulce that triggers binary Q1©2. This pulse is also transformer-coupled through the guard shield to the counter control circult on A16.

The pulse from the blocking oscillator triggers a change of binary state, causing reversal of current in the primary of a special saturating-core transformer, T1. This produces a pulse in the secondary, which is connectedifor full-wave rectification. A diode within transformer TI polarizes the output pulse. Because of the precisely controlled saturation characteristics of the T1 core, the output, pulse has constant volt-time area. The output pilse in: applied to summing point P30 through a resiator network. Through inter witing amplifier A31 this resets the potential across C25 to a level that is below the trigger level. d
If the input yoltage in-atil present, the amplifier output contiones to move toward the trigger levg. Each time the trigger level is reached another reset pulse is generatod, tending to keep the amplifier output constant near the trigger level, as fhown in Figure 3-3.

Over any given interval the mum of the aryas of the reset puises is equal
to the total integral of the input aignal. By counting the number of aucbr
pulses generated during the sample period a direct measurement of the average input voltage is obtained. For example, if each reset pulse has an area of 10 microvolt-seconds (i.e., 10 volt amplitude and 1 microsecond duration), one volt at the input will produce 100,000 output pulses per second $(100,000 \times 10$ microvolt-segonds $=1$ volt-second).


Figure 3-3. VF Converter Waveforms

### 3.3 COUNTER CONTROL A16 (FIGURES 4-7, 4-8 AND 4-18)

The logic on A16 generates the count direction commands for reversible decade counters A11-15 and 46 and provides the signals that light the correct polarity indicator and produce the correct BCD function output. This logic also generates delayed counter trigger pulses and undelayed rate output pulses for the overload detector, A10.

### 3.3.1 Derivation of Counf Direction Commands

The count direction commands are derived from the positive and negative channel pulse outputs of the voltage-to-frequency converter ( vf ), and the state of the zero detect lipe from the revetsible decades. The control state memorits for this logic are input polarity flip-flop Q3-4 and count pqlarity Ilip-flop Q7-8. Basically, the count up command is produced when both flip- (lops are in the same state (i. e., both in positive state or both in negative state). The count down command is produced when the flip-flops are in different states (i. e., Q3-4 in positive state and Q7-8 in negative state, or vice versa).

States of the Pol ${ }^{\text {ar ity }}$ Flip-Flops
The positive state of ${ }^{3}-4$ is $Q 3$ off, with its collector near -35 volts, and Q4 on, with its collector near ground. The positive state of Q7-8 is Q7 off. with its collector near -35 volts. and Q8 on, with its collector near ground. The negative states of both flip-flops are the reverse of the positive states.

## The Count Up Command

The count up command consists of two outputs from A16. One of these out-
puts is an inhibit from the count down (not down) logic line. The positive state of the count down logic line closes the down count AND gates on the reversible decade counters. The other output is the negative state of the up (not up) logic line that lets the up count AND gates on the reversible decade counters remaiy open.

## Derivation of the Count Up Command

When both flip-flops are in the same state, the negative outputs from Q3 and Q7 or from Q4 and Q8 produce a negative output from AND gate CR9-10 or from AND gate CR7-8. Either negative output is coupled through OR gate CR11-12, and AND gates CR13 and R35-36 to logic inverter Q9. The positive output from Q ${ }^{\circ}$ cuts off the coint up logic inverter, Q13-14, which leaves the count up line negative. The positive output from Q9 is inverted and re-inverted by Q10 and Q11-12, which makes the coiunt down line positive, inhibiting down counting as mentioned previously.

## The Count Down Command

The count down command is the complement of the count up command. The positive inhibit is applied to the reversible decades along the count up logic line, cloging the up count AND gates. The negative state of the count downlogic line lets the down count AND gates on the reversible decades remain open.

Derivation of the Count Down Command
When flip-flops Q3-4 and Q7-8 are in different states, the negative output from Q3 is accompanied by a positive output from Q7, or vice versa, and the negative output from Q8 is accompanied by a positive output from Q4, or vice versa. Neither AND gate CR9-10 nor CR7-8 couples a negative output to OR gate CR11-12. The output of OR gate CR11-12) to logic inverter $Q 9$ is positive. The negative output from 89 is inverted by the count up logic inverter Q13-14, which applies a positive inhibit to the up count AND gates of the reversible decades via the up logic line. The negative output from Q9, inverted and re-inverted by Q10 and Q11-12 produces a negative down output that leaves the down count AND gates on the reversible decades open.

## Typical Operating Sequence

When the first pulse during a sample period is from the positive channel, the output from Q1 triggers Q3-4 to positive state. Because the decades are all in the zero state, the negative output from zero detect emitter follower Q22 and the negative output from Q3 sets count polarity binary Q7-8 to the identical (positive) state by turning on Q8. Turn-on of Q8 cuts off Q7, which sets the +signal line positive and lights the +polarity indicator lamp through AND gate Q6. With both Iip-flops in positive state, the A16 logic commands up counting as described previously.

If input voltage polarity crosses zero and becomes negative during the sample period, the first pulse from the negative channel triggers Q3-4 to negative state (Q3 on and Q4 off). Because the count is not zero, the count polarity binary remains in the positive state. The A16 logic now commands
down counting because the flip-flops are in different states. Down counting continuesiantil the sample period ends or until a zero count is reached.

* If the decades all reach a count of zero, the detection of zero, coupled through Q22, opens the count polarity binary input AND gates to the negative input from Q4. The negative output from AND gate CR3-R10 sets Q7-8 to the same (negative) state as Q3-4, by turning on Q7. This reverses the signals applied to the polarity signal lines and indicator lamps and switches the A16 logic so that up counting is commanded. The decades now accumulate an increasing count that is identified as negative.


### 3.3.2 Overload Oufput

$\downarrow$
OR gate CR15, 33 couples positive or negative channel pulses from Q1 or Q2 to overload detector A10 through pin 1 of A16.

### 3.3.3 Counter Output

OR gate CR26-27 couples positive or negative channel pulses from Q1 or Q2 to one-shot Q18-19. Each positive pulse from OR gate CR26-2T cuts off Q18, triggering the one-shot to its unstable state. The negative palse from the Q18 collector is coupled through emitter follower Q20, logic assembly A19, and a differentiating circuit to the trigger input of reversible counter decade A11. The differentiated, positive-going trailing edge of the Q18 output pulse triggars decade All after a 1.5 microseconds delay.

Whenever zero is detected or input polarity changes, the delay of the counter trigger is extended to assure triggering after all circuit logic changes have occurred and cettled. Delay is extended by reducing the turn-on bias that is applied to the base of Q18. This increases the time that Q18 remains cut off. When the Q12 and Q18 collectors are both negative Q25 is turned on through a resistance-capacitance ( $\mathbf{r}-\mathrm{c}$ ) delay circuit. Conduction through Q25 reduces the Has voltage that is applied to Q18. As determined by the r-c delay, conduction through Q25 decreases exponentially at a rate that permits turnion of Q18 after it has been off for about 6 microseconds. Similar r-c circuits turn on Q17 when input polarity flip-flop Q3-4 changes states. The conduction through Q17 that is timed by these circuits extends cutoff time of Q18 to about 9 microseconds.

### 3.3.4 Zere D́efect Legic

During display periods, the sero detect logic is disabled by a ground input from A17Q8 to pin F, which closes the zero detect AND gate. During the sample period this inhiblt is removed, opening the gate to the negative zero detect input from counting/dieplay decades A11-A15 and A46. The input from (hese decades is negative only when all binariesw in the zero state. The negative zero detect input is coupled through $\mathbf{Q} 22$ to the count-polarity Input AND gates and the 6 microsecond delay AND gate. The disabling of the zero detect output from Q22 prevente the count polarity binary from changing states untll the next measurement period.

### 3.3.5 Polarity Output

The state of count polarity flip-flop Q7-8 is coupled through AND gates Q5 and Q6 to the + and - lamp and signal lines (pins 7, H, and J). The positive state of:Q7-8 (Q7 off, Q8 on) opens Q6, setting the + lamp and signal lines positive (near ground). The negative state of Q7-8 ( $\mathbf{8 7}$ on, Q8 off) opens Q5, setting the -lamp and signal lines positive. The polarity indication is inhibited by cutoff of polarity blanking amplifier Q24 when FREQ, AC, or $\Omega$ (ohms) measurement function $\gamma \quad$ is s\&lected, clamping in $P$ of A16 to ground.

### 3.4 OVÉRLOAD DETECTOR AIO (FIGURES 4-7, 4-15 AND 4-16)

The pulse train output from the vfc is coupled through counter control assembly A16 to overload detector A10, pin 1. When the pulse rate exceeds approximately 310 kHz ( $310 \%$ of full scale), the overload detector generates an overload signal, causing:
a. An OVERLOAD indication on units indicator display A24;
b. Input attenuator switchover to 1000 volt range by energizing relay K 5 and de-energizing previously energized range prgframming relays;
c. An overload signal to J1, pin e for switching the HP-2410B to 1000 volt range and to printer coupling card A2e for recording.

### 3.4.1 Overload Signal Memory

For serial prefix 610- and above flip-flop Q3-Q4 serves as the overload signal memory (see figure 4-15). Each negative reset pulse, inverted by Q1, resets Q3-Q4 to overload not state by cutting off Q4. Because Q3 is conducting, the overload not state cuts off overload signal driver Q5. When the output rate from the vic exceeds the overload threshold (which can range from 305 to 320 kHz ), a positive pulse from the Q2 collector cuts off Q3, setting Q3-Q4 to overlond state. With Q3 cut off in overlondstate, -35 volts turns on overload signal driver Q5 through R20 phd R25. Conduction thrpugh Q5 clamps the overload line to ground, dausing all of the actions noted in Section 3.4.

## $\stackrel{ }{4}$

For serial prefix 501 - through 605-, the overload signal memory is 4-layer diode CR6 (see ifgure 4-16). CR6 is turned on by a pögitivegoing pulse coupled to ite anode from the collector of Q1. Once it is turned on, CR6 contimues conducting, clamping the overload logic line to ground (true) untH its holding current is interrupted. CR6 is cut off and the overload indication is reset when a positive pulse is applied to the CR6, ceathode through C7 and R13. The positive pulse is produced by grounding J 1 (d) through an external contact closure. The negative-going reset pulse, which turns on Q2, produces the same effect as grounding Ji (d). The reset pulse is generated by assembly A18 or A7 as described in Sections 3.6.4 and 3.17.1.

### 3.4.2 Overlead Defection

For serial prefix 610- and above, the overload detector is a blocking oscillator whose feedback is switched from negative to positive by the voltage output from a frequency-to-voltage converter (fvc). The threshold at which feedback switches from negative to positive is set by means of variable resistor R3 at approximately 310 kHz ; the permissible range for this threshold is 305 to 320 kHz .

When'the input voltage to the Voltmeter is increased, the vic output frequency increases. As the vic frequency increases, current through fve diode CR2 reduces the negative ćharke across C5. At

- Input frequencies below the threshold, the voltage at the cathode of CR3 is more negative than the voltage al the cathode of CR4. Because of this, the only feedback path from the collector to the base of blocking oscillator Q2 is negative, through windings 3 and 1 of T1. At the threshold frequency, the charge across $\mathbf{C 5}$ makes the voltage at the CR3 cathode less negative than the voltage at the CR4 cathode. Now the feedback path from the Q2 collector to base is regenerative, through windings 3 and 2 of T1. Noise initiates the blocking oscillator action of Q2, which generates trigger pulses for the overload detector memory.

So long as the overload condition keeps the cathode ol CR3 less negative than the cathode of CR4, the blocking oscillator pulses will continue to trigger the overload signal memory. This action is repeated at a rate that is determined by the time constant of R5 and C4, assuring that the switching of the attenuator to 1000 volt ranye is not delayed by reset. Usually only a few pulses are generated before the attenuator is switched to the $\mathbf{1 0 0 0}$ volt ranye, removin' the overload.
For serial prefix 501- through 605-, the positive overload memory trigger pulse from the collector of Q1 is developed when current flows through the No. 2 winding of transformer TI. If the vfe is not overloaded, current flows only through the N . 1 winding of
 Ing No, 1 to winding No, \& are the voltage levela exinting at tho oathodes of CRIS and CR4. The voltage at the onthode of CR4 in an to about -25 volte by potentiometor RA: The voltage at the cathode per fras ja'doterminod by the froquency of the pulaon arriving at pin 1. Theme puimen; apuplad

 eroquency. For mulao irequonatón lom than 810 ko the voltage moroma Cs. in much that the cathode of CRS ip more newative than the oathode of CR4 and ourront flowa from ground, through R5, and, winding No. 1. Readom thermal nolas voltugen doveloped acromn no ma remult of the curront flow - aro couplod to amplifior Q1. Tho coutput al amplifior Q1 ia tranaformor couplod back tif winding No. 1. Bgeaume of the phame rolation botweon the primary and acoondipy whidiyr No. 1, tho foodback, voltage in out of phamo with the tuput, romulting in ouncollation of tie notge voltago.
If tho linput pulao froquendy pouchon or oxcoeda 310 lelin, tujo voltago acromen C10 rises to a lóvol that materi the oathode of CRS inoro donitive than the cathode of CRA. At thif polnt fine aurront awitahon from windlas No. 1 to winding No. 2. Typ randinernbise voltago devolojed morona RS in now amplifiod and linvortod by Q1 and couplod back to winding No. 2.: Tho foodback from tho primary to acoondary winding No. 2 in lin phaso wilh tho amplifior linput. Rogenoration quickly maturatom tho amplifior, senorating a ponitivo pula largo enough to trigsor comduction of t-layor diode CRS. The regen. orative'action alao incroanom current to the polnt whore the trapaformor core aturatos and no bongor priwidan the oouplings notion. Thin atopin tho-kogemorative Colion. Amplifior conduction then docreanom, rofurning to the provious unmaturatod condition. Rfter a tumandolay that iy omaentially dotorminod by tho time conmant of 1 l ( and C 2 , the comparison circult is roady to cyclo again. Than action continuon as long an tho ovorlond, producting a train of poaltivo-bolng pulsas from tho collector of Q1. Altiough omly ono pulao in roquirod to lurn on the 4-layar diode, tho aerion of pulaon provonta romoval of thif ovorlond Indication by roactling until tho ovorload condition has boon corrpotod. Unually only alow. pulaos are generntod bofore the attonator is awitehed to the 1000 volt rango.

### 3.5 ATHENUATOR COUPLINO LOOIC AB AND IV RILAY TIMINO AFI

### 3.5.1 Alfenuator Coupling Logic AB (Nigure 4-13)

The attonuator coupling logic controle rango programming relayn $K 1$ through K4 of attonuator asmombly A2B. Durlan normal manual oporation, thar RANGE switch provides a ground comection through the FUNCTION awitch to the lin-1 put losic line for the desirod rango. During oxtornal programinlang, the ground comiection mupl be preydded at the correct ply of PROgRAM CONNECTOR J1, from which it is routed through an EXT BEL contacf of the FUNC'IION awitch to the lnput logle line. For example, a ground comaction to pin 12 of AB programs the 100 volt fampe. Couplod through diode CRE, this causen transiator Qis to conduct, enorgialix 100 volt range relay Ki, provided that no overlond condition exists and that no ac or ohms measuremget using a IIP-2410B is belng made. This examphe in typical of operation of the other
range programming lines, oxcopt for the 0.1 voltrange. When the 0.1 volt range in eolegied, relaya K1 and K2 are both energized.

The detection of an overlond by the circult ton A10 caumen pina 2 and 15 of AB to be grounded. The grounding of pin 15 energizen 1000 volt range relay K4. The grounding of pin 8 , amplificd by 95 and $Q 4$ and connoctedtirough dredea
 programming rolay K1 through fity cmuling thom to do-enorgizo.

When a lip-2410B is ungé with the Hip-2401C for ac or ohma measuroments, a ground is comnectod to pin 4 of Ag from the ifp-2410B unite couplling card, AO. This algnal ia used to turn on © 0 , onorgizing the 1 voli range relay K2. Amplifiod by Q1 and Qu, thile aignal disabion the otior range gating tranaintora.

### 3.5.2 I Voil Roley Timing A47 (Figures 4.13 and 4-29)

The $i$ vole rolay timinys circult on 147 timos the energlaing and de-onerktalnk of Th ranye reluy $\mathrm{K}^{2}$ oit 120 so that 11 and 1000 V range relay K are never ener-
 lbeo Volls could be applited as roqs attonuator rontator Rd2. For a bried periled 042 woild disalpute 100 watto, adatalating chamage proportional to the duration of the overload.

Whon $K 2$ in not prosrammod, conduetton through Q1 diachargoe capacitor C2. When K2 la programmed, C2 intlally prosenth a dow limpedance path while it chargea. Tho long time constant charglap ta 62 holds $k 2$ doLonorgleod untll all othor rolaya, Including K 5 , have pad lime to de-emergize. When the attenuator in awitchod from iv to 1000 v ranke, programming of relay $\$ 2$ in intorruptod: Tho onerky atored in tho coll of $k 2$ dischargees actons capper
 doluyod, by capacitor C102 (acrones the KB coll) witll K2 has de-enorkized. At the aumo timo capacitor C2 of AA7 is diacomented from fio K 2 ralay - Goll by the revorsib of voltape polaritien acroas diode CRI. It in diachargod by Q1 and thus han no dfoct upon de-morgize thming of K2.

### 3.6 GATE CONTROL AIT AND DISPLAY CONTROL AIA <br> (Figures 4-7 and 4-19)

Gato and diaplay control aspembllea 117 and Als operate tokether to com-
 dende A11. Thof abo control the daplay pertod and the tranalor of mach new meanírement to the digltal deplayb of the derade counter a. Thabe func: foms are performed an directed by the arthapis of the sAMPLE: PERIOD) awitch and the BAMPLING RUATE control.

### 3.6.1 Measurement Phase

The measurément/diaplay cycle of the HP-2401C is illustrated in Figure 1-21. The measuroment phase (ample pertod) of this cycle bektins when
the decade divider output seldeted by tre SAMPLE PERIOD suftch is applied to gyart/otop input pin/4 of gate control aasembly A17 via logic anaemblyaj1. The poaltiveogoing part of the decent divider algnal cute off
 mally lahibite triggering $\alpha$ the firat docade counter, All. The next poal-tive-going empurition of the time bapt input aignal cite of A17ci, turning on A17Q1, blanking counter input triggere appiliod to A11 pin 10, and terminating the ample period.

### 3.6.2 Tranafor to dieifal Display

1
Th positive-going valtage from the A17Q1 collector at the end of the gamphe period cute off A18G2 of tranfor one-ahot A18Q1-GR. The one-ght remalna in thia unstable atate (A18ge off, A18Q1 on): for about 70 milliseconds. Durjfig this period, atorage gate amplifior AiBQs is cut alf, allowing the collint of the decade binaripa to be tranaferred to the dieplay torage circuits. At the ond of this period conduction through A180. turne on storage gate amplifier A18Q3, which holda the new count untll the next trankfer pulse is triggered.

- 'The proviously-described tranafor mechaniam is effective only when STORE/ DISPLAY awitch 87 is in STORE position. When 87 is in DISPLAY position AIBQS is discomected and the states of the decade countor binaries are displayed at all times, not just after tranafor.


### 3.6.3 Variation Duration Display Phace

The negative transfor pulse from the $A 14 Q 2$ collector tumfa on A1BQ4, cutthag off A1BQS of the display timing fip-flop. (Flip-flop A1BQ4-Q5 ia actually a one-shot whenovor the SAMPLING RATE contribl is not awitched to STOP position.) Duration-a this undable atate, determined by the time constant of A18C8 and the setting of SAMPLING RATE potentlometor R204, may range from ${ }^{\circ} 0.2$ to 7 seconds. Conduction through $A 1 B Q 4$ inhibits start AND gate A17C1-R3 of gate flip-flop A17Q1-Q2, by culting off A18CR7 and A17Q4. This preventa the start of in monsuroment during the diaplay poriod.

An extornal clamp to ground from a digital recorder, programmer, or othor digital data processing device may be applied to $\mathrm{J} 2(22)$ to hold the display and recording outputs longer than the normal period. This clampa coupled through A17CRE to pli 10 of A1B, holds A1BQ5 off untll it is removed.

### 3.6.4 Resotting

The negative-golng tralling edge of the signal from the AlBQt collector triggers a negative reset pulse via amplifiers A18Q6-Q7. This negative pulse resets decade dividers A1-A5, decade counters A11-A15 and A16, pate flip-flop A17Q1-Q2, and the overload alpalal memory on overload detector A10. After resetting, the measurement phase can be liltated as described in Section 3.6.1.

Current genermtor A1797 conducts additional blas to A18Q during the perlod between redetting and the atert triggering of gate flip-flop A17Q1-Q2. This acsures that A18G4-OS remping in the atable "meacurement enable" atate until it in triggered to inftiste the diaplay poriod.

### 3.6.5 Manual Cpimerel pf. Mecsurement Phase

During manual operation, the automatic measurement/diaplay controin lopic is bypassed. The atarting and atopping of the measurement is controlled by the START and STOP poaltions of the SAM PLE PERIOD switch. The START and STOP poaltiong both apply a clamp via the manual logic line and pin 10 that holda AIBQS cut off, lintiblting triggering by the time base input from A21, pin 24. The ponitive START level cuts off A17Q1, starting the measurement. A negative level produced by switchink to STOP poaltion turne on A17Q1, atopping the measurement.

### 3.6.6 Resep-Trigeered Measuremen and Display

Switching the SAMPLING RATE control to STOP poaklon converts AIBQ4Q5 to a flip-flop. The measurement-display cycle is then tripgered by a poaltive-golng reaet pulac from the -35 volt regulator and reset card, A7. Through A1BCR0 this pulse cuta off A18Q4, which turns on A1BQ6, enabling the start triggering of gate flip-flop A17Q1-CR as deacribed in Section 3.0.1. Tranafor one-ahot A1BQ1-Q2 and display $1 / m \operatorname{lng} \mathrm{fl} / \mathrm{p}$-flop A1BQ4Q5 are trikgered as noted in Sections 3.6.2 and 3.6.3, excejt that A1BQ4QS continues to inhlbit measurement until it is reset by a positive-kolnk pulse from A7.

### 3.6.7 Apcord Signal Imitter Pollowers

Record algnal emitter followers A17Q5 and A17QB couple the atate of gate flip-flop A17Q1-Q2 to the digltal recorder or other dikital data proceselnk device that may be connected to the BCD OU'TPUT receptacte of the Hib2401C. Durlak the ample period, A17Qs clamps the -record command line to kround (positive truo) AITQB clamps the trecord command lline to ground during the diaplay pertod, when the bed coutputa of the HP-2401C are not changlas.

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4
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### 3.7 J00KHz OSCILLATOR AND SCHMITY TRIOOER AG (Figures 4-7 and 4-1I)

The internal time base standard for the wanter bection is kemerated by a l00kita crysuat controlled oscillator. The output of the oscillator in rentod to the 100 KC STD Buflech, SB. The INT poestion of ixi commecta the 100 kll . piscillator output to a Schmilt trjeker circult. The output of the Schmilt trik. ger is a 100 kHz square wave that is used to trikger the first decade divider (A1). A rear-panel BNC comentor, 100 KC STD OUTPUT/INPUT, (J3), is comnected via the INT position of Bwiteh So to the oxifut of the Schmitt trik-

Section III
ger 00 that the internally generated 100 kHz aignal can be used externally. The EXT position of 88 connects receptacle J3 to the Schmitt trigger input. The Schmitt cirdint may then be triggered by an external time base algnal cominected to J3.

### 3.8 TIME BASE DIVIDERS AI-AS (Figures 4-7 and 4-10)

There are five identical time base dividers operating in series to divide the 100 kHz time base frequency successively by ten, These dividers provide output frequencies of:
$\left.\begin{array}{r}\left.\begin{array}{r}10 \mathrm{kHz} \\ 1 \mathrm{kHz} \\ 100 \\ 10 \\ 10 \\ \mathrm{~Hz} \\ 1\end{array}\right\} \text { Used to check operation of the counter section. }\end{array}\right\}$ Used for the standard $0.00 \mathrm{H}^{\circ}, 0.1,1$ second sample periods.
Each decade divider consists of gur cascaded transistorized binaries, puch that the output of the first is coupled to the input of the second, and op on. Feedback networks are arranged on the binarles to provide 4-2'-2-1 bipary code weighting and input-to-output division ratio of 10:1:/

At the end of each counter display period the decade dividers are reset.
 During normal operation, when the sampling rate is determined by variable setting of the SAMPLING RATE control (i.e. 0.2 to 7 seconds), the reset pulpe from the diaplay control circult (A18) resets the decade di- . viders (A1-A5) to 87033. This means that 2907 counts (or 29.67 mulliseconds) are required before the outputs of the decade dividers can start another sample period. This delay allows A18C8 (the capacitor determining the 0,2 to 7 seconds display time) to discharge before the next display perfod starts. In the fast sampling mode of -operation, when the SAMPLING/RATE control is in the STOP position dind resetting from A7 is used, the decade dividers are reset to 00033 . This means that 907 counts (or $0.07 \mathrm{millisec} \mathrm{m}_{\mathrm{d}}$ ) are required before the next count can start. This small delay provides attenuator switching time and settilng time for the HP-2411A Guarded Data Amplifier, if used.

### 3.9 ATTENUATION CONTROL, INPUT'AMPLIFIER, AND TRIGGER CIRCUIT A25-A 27 (Figures 4-7 and 4-27 or 4-28)

When the HP-2401C is used for making direct frequency measurements, the
 input frequency is connected to the front or rear pancl FREQ $\mathbb{N}$ PUT connector. It is then routed through the attenuation control circuit where the level of the input algnal is adjusted by the ATTENUATION control to provide a reliable count. When the ATTENUATION control is in the CHECK position, the 10 kHz frequency from the first decade divider, $\mathrm{Al}^{1}$, is routed through the attenuation dontrol circult to be counted. The output of the attenuation control circuit is coupled through the input amplifier to the trigend ger circult. The trigger circult is a Schmitt trigger that provides a fastrise, constant-amplitude output square wave which is routed througt the; counter logic on A19 to decade counter A11. The trigger circuit must be adjusted for pulse measurements (see Section 4.7.11).
3.10 RIVEREAELE 300 KHz DICADE COUNTERS All-A1S, A46 (Figytres 4-7 and 4-17.)
Six Identical reveraible decade counting unite comected in series count input pulses and dieplay the count an alx-digit number. The poaltive inpyt triggers are coupled to the firat counting decade, A11, through logic on A18 and a differentiating network. Gating of the triggera is controlled by A17as. deecribed in section 3.6.1.

### 3.10.1 Counting

$\Gamma$
The counting decades can count either forward or backward. The count direction is determined by the atates of the count $\overline{u p}$ and count down control lines from counter control assembly A16. Regardleas of count direction, the feedback between the binaries is arrauged to produce a count output in 4-2'-2-1 binary-coded-decimal (bcd) form. The bed outpute from the decades are connected to the rear finel BCD OUTPUT receptacle J 2 .

Up Counting
The decades alwaye count up during irequency measuremente and during the firat phase of voltage measurementa. Up counting in enabled when the count down line te clamped to ground and the count up line ta placed near negative , 35 volte by the counter control loxic on A/6. This closes the down count AND gaten and openf the up count AND gates. Positive trikgers are coupled from the collectora odd-numbered tranalators (Q1, Q3, Q5, Q7) to succeeding stages. Each trigger advancea the count by one. After the count reaches 0 and is then advanced to zero, the first decadegenerates a trikger which advancea the count of the second decadejy and so, on through all six countling units. The waveforms assoclated with up counthin are shown at the left of the dashed line in the Figure 4-17 waveforms diagram. The comint progigesston is as follows:


## Down Counting

The decades are commanded by the counter control logic fo ecouit down when the polarity of the input voltage reverses. The down chunt conthues until a zero count is detected. Down counting is enabited when the cinnt $\overline{\mathrm{up}}$ line is clamped to ground and the rount down line is placed wear nek-
ative 35 volte by the counter control logic on A16. This opens the down count AND gates and closes the up count AND gates. Poaltive triggera are coupled from the collectors of even-numbered tranatators ( $Q 8, \mathbf{Q}$, Q8, Q8) to eucceeding atages. II the up count accumulated belore reverasal of the count commandi is 10 , it consiats af aero atates in the A11 decade, 1 etate in the A12 decade, and zero atates in the remaining decades. The firat down dount trigger ecte the All decade to the count of 9, which triggera the A12 decade to zero. The progreasion of the down count is the exact-reverse of the up count progreasion.

### 3.10.2 Zero Defection

Decade counting unite A11-A15 and A46 contain an 18-input AND gate (CR9, CR10, and CR13 of each decade) whose output in a poaltive-true inhibit if any of the decade binaries aroyin other than a zero etate. All binarien in a decade aro in zero atafe when the odd-numbered tranalators (Q1, QS, Q5, © ) are conducting. When all blparies in the counting decadea are in zero state, the zero detect line in no longer clamped to ground by conductioh through wan even-numbered transiator (Q2, Q4, Q8) in any od the decades. During a measurement period, removal of the clamp activatea the zero detect logic of A16. In responme to the detection of zero, the counter control logic commands up counting by the decades.

### 3.10.3 Displey Section

The $4-2{ }^{-2} \mathbf{2}$ bed output from the decade binaries is conrected to neon lamps that are associated with a photgconductive tranalator matrix. The pattern of lighted neon tampa sets up (low-resistance path through the translator matrin that causen the correct humeral to light in the digital display tube. For example, a 5 count Jights neon lamps DS1A, DS2A, DS3B, and DS4A. When decoded by the matrix; the lighted atates of DS1A, DS3B, and DS4A light the 5 numeral in the diaplay tube.

The position of STORE/DISPLAY switch 57 determines when each count is displayed. The DISPLAY pofition of 57 disconnects the store signal from the neon transfer line. This is used for continuous display of the blnary states before, during, and after each count. The STORE position of 57 comects the atore aignal (a relatively low-impedance ground return) to the neon transfer line. The store dignal is interrupted at the end of each count by a 70 millisecond transfer pulse that is generated on display control assembly A18. This interruption connects the binaries to the neon lamps. Restoration of the store signal at the end of the transfer pulse keeps the neon lamps on and off in the conflguration established during the transfer pulse by providing a return path that is independent of the blinfies.

### 3.10.4 Resepting and Presotting

Reversible decade counters A11-A15 and A46 are reset by a negative pulse appiled to pln $R$. This reset pulse turns on all odd-numbered transistor (Q1, Q3, Q5, Q7), estaplishing the zero state.


Presetting is used for special data system applications. It involves applyIng a negative pulse to pins $L, 6, F$, and $E$ of the vithrious decades as required to achieve the desired initial count states. the negative preset pulse turns on the translators) to which it is applied, publishing preset count in standard 1-2-2'-4 bed code at follows:

| BCD Weighting | 1 | 2 | 2 | $\mathbf{4}$ |
| :--- | :--- | :--- | :--- | :--- |
| Preset Pin | L | 6 | F | E |
| Translator Turned | On | Q 2 | QA | QB |
| Q 6 |  |  |  |  |

UNITS/COUNTER INPUT LOGIC A19 (Figures 4.7, 4-9, and 4-20)
The unite logic $\alpha$ A10 connects to the front-panel FUNCTION and SAMPLE PERIOD switches and provides aignal outputs for lighting the units display, for decimal point logic assembly $A 20$ and for blanking/time base selection assembly A21. The units logic is Illustrated in Figures 4-9 and 4-20.
By means of positive AND gates the counter input logic determines whether the counter gate is controlled manually or by one of the standard sample periods. When voltage is to be measured, the volt signal at pin 15 of Ala is negative. This signal opens AND gate Q10 to the negative pulses that are received from the vic via counter control assembly A16. These pulses are coupled through AND gate Q10 to units decade counter All through a trigger differentiating circuit. The positive triggers produced by this circult are counted when the counter gate opens.

When the frequency of a signal is to be couitited the freq signal at pin if is negative. This signal opens AND gate Q11 to the positive pulses from the Schmidt trigger $0^{0 n}$ A27. The output pulses ion Q11 are routed to (11Its decade counter Abs in the samopmanner as voltage pulses.
When opening and closing of the counter gate (flip-flop A17Q1-Q2) He manyally controlled (SAMPLE PERIOD switch in START) or STOP position, fe man logic line is negative. This opens AND gate) Q12 to the logic level on the start-stop logic line. When the SAMPLE DERIOD switch is set to START, the ground clamp output from Q12 sets A17Q1-Q2 to measurement enable' state. When the SAMPLE PERIOD switch is set to STOP position, the neg. ative-golng voltage passed by the base-collector diode of Q12 turns on A17Q1, setting A17Q1-Q2 to measurement inhibit state.

### 3.12 DECIMAL POINT LOGIC ASSEMELIES A20 AND A30

Decimal Point Logic Assembly A20 (Figures 4-9, 4-21, and 4-32)
The decimal point lamps are controlled via) a photoconductor assembly. (See Figure 4-33.) When a given decimal lamp lis to light, the appropriate neon lamp (NE-1 to NE-5) in the photoconductor assembly is lighted by the declmat polit logic circuits on A20. The light from the neon lamp reduces the resistance in the associated photoconductor, allowing the proper decimal lamp

In the decimal assembly to light. When an incomplete measurement program occurs, a aignal from the blanking logic circuit on A21 lights NE-6, which prevente any of the other decimal lamp controlling neond (NE-1 to NE-5) from lighting. This in turn prevents lighting of any of the decimal pointe on the vigual diaplay. (The instrument is also awitched to 1000v range resulting in a low reading when programming ie incomplete.)

The decimal point logic circuitry, consiating of diode and transiator gates, tranalates the control settinge for the various modes of operation to determine the proper decimal point poaition. Thid ascures that the digital didplay is direct reading in volte, millivolts, of kilohertz. (This logic aleo provides the correct decimal point placement for ac voltage meacurement and resiptance measurements when a HP-2410B is used with the HP-2401C.

The decimal point logic is Illuatrated in Figure 4-9. ... Easentially, the diode and transistor gates combine negative- and positive-true inpute to light one of the five neon lamp: (NE1-NE5) in the photoconductor aseembly. The poaltive-true input, a valtage range ( $0.1,1,10,100$, or 1000) for voltage meaguremente, completes an emitter ground for one or more of the trandstor gates. A negative true input appliled to the bace of one of these transistor gates then produces a positive true collector output that lights the associated neon lamp. The negative true transiator AND gate input is assembled by a diode AND gate; it represente the removal of all positive true inputs, which are clamps to ground.

Decimal point placement is determined by the function measiured (VOLT or FREQ), the voltage range (if VOLT function is selected), and the sample period. For example, when FREQ function is selected, transistor AND 4 gates Q5, $\subset$ (1, or Q9 arg enabled via OR gate CR14-CR15. Selection of sample period determines which transigtor AND gate opens and which ne-

$-$

Neon Lápp
Lighted
NE2
NE3
NE4

Decimal Placement On Digital Dieplay
00000.0
0000.00
000.000

Only one neon latur, The can bo positive at any one time; all other lines are negative. If none of the line is positive, the output of negative AND gate CR24-CR28 is negative, indicating an incomplete program. This negative signal is coupled to logic on A21, causing, the decimal point display to blank and the 1000 v attenuator relay to energize.

### 3.12.2 HP-2411A Decimal Point Logic Card A30 (Pigyre 4-31)

Logic card A30 provides for correct positioning of the decimal point when the HP-240 C is used with a HP-2411A Guarded Data Amplifier. The logic shifts the decimal one place to the left, or two places to the right while lighting the MILLI portion of the MILLIVOLTS display, when the HP-2411A 18 set for +10 galn.
$\cdots$
As an example $o f$ the ASO logic, assume that the HP-2401C is programmed for IV PANGE and . 01 8EC MMPLE PERIOD. Thit grounde the emitters of NND gates Q9, Q10, and Q1 via the NE4 logic' line and A20. When the HP-2411A is set for +1 Crin, the falee atate (nequ -35 volta) of the X10 logic line turne on Q1, grdinding the X10 logic 1 nge arid closing AND gates 49 and Q11: AND gate Q10 is opened, lighting NE-4 on the photoconductor assembly. When the HP-2411A is set for +10 gain , QI is cut off and Q2 conducta. This closes Q10 and leaves Qg and Q11 gubject to the falae atate $\alpha$ the millidrive line, which turns of Q3, grounding the millidrive line and cloaing AND gate Q11. AND gaté ©9 is opened, lighting NE-2. This decimal shift two places to the right is matched by the lighting of the MILL portion of the MILLVOLTS display because the grounding of the X10 line is coupled to the millidrive output line through OR diode CR1 When. IV RANGE and 1 SEC SAMPLE PERIOD are selected, the NE4 and millidrive lines are both true' (near ground). When the X10 line is aldo true, gates Q9 and Q10 are closed and Q11 is opened, lighting NE-5. This degimal ahift one place to the left converts the 000.000 MILLIVOLTS dieplay to 00.0000 MILLIVOLTS dieplay.

UHP2411A Deolmal Point Logic card A30 is not inatalled in the HP-2401C, a jumper board is installed in receptacle XAso. The connections completed by this board are thown in the upper right corner of Figure 4-31.

### 3.13 BLANKINGLOGIC/TIME BASE BELECTIONA21

(Pigures 4-7, 4-9, and 4-22)
The blanking logic/time base eelection circuitry combines appropriate operating logic signals to blank the decimal point lamps on the display and energize the 1000 v attenuator range relayowhen programming incompra. It aldo selects one of the three efandard time base frequencies ( 100 Hz , , 10 Hz , or 1 Hz ) to gate the counter section when using pae of the stanadard sample periods.

If programming-ts incomplete, assembly A20 provides no ourput for lightIng any of decimal neons NEI-NE5; therefore, none should be lighted. Nevertheless, additional logic is required to program the 1000 v range. Logic is also provided to blank the decimal neong without programming the 1000 v A20 pin 6 to A21 pin 17 and the "false" state of the freq - man logic line produce a positive output from AND transistor Q5. This output lights NE6 on the photoconductor block, inhlbiting the lighting of any of NE1-NE5. This output also programs the 1000 v relay logic line, setting attenuator A28 to 1000v range.

The "truey" state of the freq • man logic line, coupled through diode CRG, lights NE-6. This blanks all decimal neons but does not switch A28 1000v range because AND transistor Q5 is cut off through CR8.
The time base selection circuitry selects one of three standard time bases by opening one of three positive AND gates connected to the time base out-
puts of the decade dividers. For example, if a . 01 BEC eample period is selected, the input at pin 16 of 121 will be negative (indicated by .01 8EC). (See Figure 4-7. This signal opens AND gate © . When the 100 Hz signal from the degade divider goel positive, AND gate al providel a positive output. This output is coupled through a ponitive OR gate to the gate control circuit on A17.

### 3.14

## HP-2410: AC AND OHMS GATE DELAY A23 (Figure 4-25)

The ac and ohms delay gate delays measurements as required when a HP$2410 \mathrm{BAC} / \mathrm{Ohms}$ Converter is used with the HP-2401C. The delays provided differ with the type of measurement, las follows:

| $\checkmark$ | Type of Measurement |  | Delay (Milliseconds) |
| :---: | :---: | :---: | :---: |
|  | e | AC (Normal) | 500-550 |
|  |  | AC (Fast) | 200-220 |
|  |  | Ohms | 100-110 |

The programming of a measurement using the HP-2410B cuts off Q2 through OR diode CR5, CR6, or CR7, opening AND gate Q2-CR8. Each negative
reset pulse/from the reset bus is then passed through the AND gate, trigOR diode CR5, CR6, or CR7, opening AND gate Q2-CR8. Each negative
reset pulse/from the reset bus is then passed through the AND gate, triggering flip-flop Q3-Q4. The negative-going output from the Q4 collector gering flip-flop Q3-Q4. The negative-going output from the Q4 collector
is coupled through emitter follower Q1 to a resistance-capacitance $(r-c)$ delay circuit. The negative output from the Q1 emitter allows capacitor
Function coding is shown in Table 2-5.


The printer coupling circuit tranalates decimal position, range, and function information to appropriate'bcd codes for digital recording. The decimal position is a number from 0 through 7. This number ( n ) stands for a negative power of ten multiplier (i.e., $10^{-4}$ ) that indicates the position of the decimal point on the ricorded measurement for the selected units. A sample digital printout follows:


The decimal position information is received from the outputs of the standard decimal point logic assembly A20, (and HP-2411A Decimal Po Logic Card A30 if installed) and then interpreted by the logic networks on A22. The deciphl point logic network on A22 translates millivolt readings on the HP-2401C idsplay to equivalent readings in volts for the recording output. For example areading of +0001.23 MILLIVOLTS on the HP-2401C is recorded as 10001235 , indicating that the function is +VDC and the decimal point is five places to the left (1.e., 0.00123).

C1 $\alpha$ the r-c delay circuif to charge negatively at a rate that in determined by circuit realatance.

When the negative voltage acrose capacitor C1 reaches a certain level, the flip-flop le driven to ite original atate. -The delay time required for this action le determined by the meacurement function that is programmed. When ohme is programmed, resietore R1, R2, and RS are effectively connected in parallel through doden CR2 and CR4, thue providing the minimum delay of 100-110 milliseconds. When AC Fant is programmed R2 and RS are in parallel, providing a longer delay of 200-220 myliseconds. When AC normal is programmed, RS determines the longent delay, which is $\mathbf{5 0 0 - 5 5 0} \mathbf{~ m i l}-$ liseconds.

While the filp-flop is in the reget-triggered delay atate, a negative-going pulae, coupled via non-Inverting amplifier QS, blanks the trigger input to the second time base divider, A2. The transition of ©9-Q4 to non-delay state triggers the 4 -millisecond ane-ahot, 98-Q7. The output pulse from the 96 emitter prolongs the meacurement delay an additional 4 milliseconde. After this delay the, time base cample gate is generated as usuag

### 3.16 HP-24108 UNITS COUPLING A9 (Figures 4-9 and 4-14)

The HP-2410B units coupling circult is required when a HP-2410B AC/Ohms Converter is used, This circult interprets the programmed range and function inpute' and provides output aignalg to light the appropriate units and decimal on the digital display.

When the 10 megohm range is programmed by a ground connection to pin 15 of A9, the signal in coupled through A8 to light the "M $\Omega$ " lamp on the units display, and to the 10 volt logic line to position the decimal point on the digital display. At the same time, this signal is coupled through a positive OR gate to cut off transistor AND gate QS so that the "K $\Omega$ " lamp cannot be lighted.' The blanking of the $K \Omega$ lamp is necessary, because whenever the 10 megohm line is programmed, the ohms line is also programmed. This would ordinarily allow Q3 to conduct; lighting the K $\Omega$ lamp. When the ohms line is programmed, the "VOLT", "MILLI" and polarity-lamps are blanked.

The $K \Omega$ lamp will light under measurement conditions equivalent to those which light the VOLT lamp when voltage measurements are made. This requires that the 10 megohm and milli-drive lines not be programmed (i. e., negative) and that the ohms line be programmed (i.e., positive). The ohms line is always programmed for resistance measurements.

The " $\Omega$ " lamp lights when the milli-drive and ohms lines are positive and when the frequency and manual gate lines are negative. (The $\Omega$ lamp is equivalent to the MILLI and VOLTS lamps when voltage measurements are made.)

```
1 1
```

The programming of AC measurements grounds pin 8, lighting the AC damp. The programming of either AC or ohms measurements has two additional effects. The polarity blanking amplifier, A 16 Q 24 , is cut off, blanking the polarity outputs from the counter control assembly. The positive true (ground)
state of the AC or ohms logic line is connected to the attenuator coupling logic on A8, energizing iv range relay A28K2 and causing all other altonuator range relays to be de-energlzed. This is done because all measuremontes made with the HP-2410B must use the iv range of the HP-2401C.

## $3 A 7$ <br> -33 VOLE REGULATOR AND RESET CIRCUIT AT AND +CV BIAS CIRCUIT

 A29
### 3.17.1 A7) Reset Circuit (Figures .8-7 and"4-12)

- The reset circuit on card Att is designed to provide counter section reset pulses in response to pulse or contact-closure reset triggering. Pin 12 of A7, the closure input to, the react circuit, is connected to the frontpanel RIESET publibutton and to pin " 0 " of rear-panel RROGRAM CONTROL connector J1. When pin 12 is grounded, a Schmidt trigger, Q4-Q5, is flipped after delay of approximately 3 milliseconds. This delay is caused by an integrating network, R17-C2 which discharges toward ground when pin 12 is grounded. This network smooths out Irregularities in the input signal caused by contact bounce, preventing the triggering of multiple reset signals. When the voltage across C2 reaches the emitter bias level, the Schmidt trigger is flipped as Q4 is cut off. The output of the Schmitt trigger is a fast-rising, positive-going pulse which is coupled out pin 9 to reset the display timing flip-flop on A18 to the non-display state. The 'Schmitt trigger output, amplified and inverted by Q7, is also coupled out pin 8 as a negative pulse to the reset buss. This pulse resets the decode counting units, the decade dividers, and the overload detector.

Pin 14 of A7 is a second linput to the reset circuit that is connected to the rear panel COUNTER RESET receptacle J4. The, reset circuit is designed to respond to a negative 15 -volt, 25 -microsecond reset pulse with a risetime of less than 2 microseconds. The pulse reset signal is assumed to be much cleaner than a contact closure signal applied at pin 12, and therefore the pulse is simply amplified and inverted by Q6 and Q7 and coupled out pins 9 and 8 as previously mentioned.

### 3.17.2 A7 -35 Volt Regulator (Figure 4-12),

The - -35 volt regulator provides regulated $\mathbf{- 3 5}$ vac power for the transistorized circuits of the HP-2401C and the bed reference level voltages that are required by an HP 562A Digital Recorder. The + reference on pin 4 of A7, approximately -2 vdc , is the reference for a binary " 1 ". The reference on pin 6 , approximately -25 vdc , is the reference for a binary " 0 ". These reference levels are connected to rear-panel BCD OUTPUT receptacle J2.

The $\mathbf{- 9 5}$ volt regulator circuit consists of a differential amplifier, Q2-Q3, and an emitter follower, Q1. The output from Q1 is coupled externally by a chassis-mounted emitter follower, Q3, to series regulators Q1 and Q2. The'series regulators are on a chassis-mounted heat sink. The regulator output is set at -35 volts by means of variable resistor R10. Differential
amplifier QR-QS compares the potential tapped by R10 with that developed dcrons resistor R6. Output voltage variations, coupled through breakdown diode CR1, amplified and inverted by. Q2-Q3, and coupled by Q1 provide the negative feedback that regulates the -35 volt output. The negative feedback from the amplifiers on A7 increases or decreases conduction through the chassis-mounted series regulators enough to correct variations of output voltage almost completely.

### 3.17.3 A29.46V Bias Circuif (Fiqure 4-12)

The $+6 v$ bias circuit on card A29 supplies regulated positive 6 vdc bias to counter control card A16 gnd reversible counting decades A11-A15 and A46. In addition, rectifier-filtor circuits mounted on this card (A29) provide unregulated +150 vdc and -150 vdc outputs to the digital and decimal displays.

The +6 volt reference is provided by voltage breakdown diode CR3. The potential dropped across CR3 is coupled to the +6 volt bias line by emitter follower Q1.

### 3.18 POWER SUPPLY FILTER A36, SERIES REGULATOR A34, AND CALIBRATION STANDARD A35 (Figure 4-32)

### 3.18.1 Filfor Board A36

Filter board A36 supplies rectified and filtered dc voltages to series regulator assembly A34 and to calibration standard assembly A35. It also provides rectified and filtered 300 vdc to the photochopper driver oscillator on A31.

### 3.18.2 Series Regulator Assembly A34

The series regulator assembly contains the circuits that control the positive and negative 12.3 vdc outputs of the HP-2401C power supply. These outputs power vfc assemblies A31, A32, and A33. The series regulators perform this function in response to inputs received from calibration standard assembly 195.

### 3.18.3 Calibration Standard Assembly 435

The callbration standard assembly contains the calibration standard supply and amplifiers that control the positive and negative 12.3 vdc series regulators. These circults are discussed separately in the following para-. graphs.

The negative 12.3 vdc output from the power supply is set by potentiometer R9. Output voltage variations are fed back to series regulator A34Q1 through differential amplifiers Q11 and Q1-Q2 and dc amplifier A34Q2. DC amplifier $A 34 Q 2$, on series regulator card $A 34$, provides the inversion nec-


Figure 3-4. Typical Unguarded Input Circuit


Figure 3-5. HP-2401C Guarded Measurement Technique


Figure 3-6. Rejection of Superimposed Noise


Figure 3-7. Rejection Around 60 or 50 Hz
essary for negative feedback and'regulation of the negative 12.3 volt output potential. The voltage reference of the negative 12.3 volt regulator amplifier is provided by avalanche diode CR1, in the base circuit of Q10.

The positive output voltage from the powef supply is set by the negative output voltage, which is used as the reference for the positive regulator amplifier. The output voltage from the positive supply is held approximately equal in magnitude to that from the negative supply by emitter follower Q9, dc amplifier Q8, and series regulator A34Q3. Equal positive and negative voltages applied across divider R25-R26 place the Q9 baseemitter near ground potential. This allows conduction through de amplifier Q8, which biases series regulator A34Q3 to conduct the load current required from the +12.3 vdc power supply circuit. Variation of the +12.3 vdc supply output potential with respect to the negative output is amplified and inverted by Q8. Negative feedback from the Q8 collector to series regulator A34Q3 largely corrects output voltage variations. Any increase or decrease of the negative output voltage establishes a new reference that causes a corresponding increase or decrease of the $+12.3 \mathrm{vdc}{ }^{\text {A }}$ output potential. The positive regulator operates to keep the Q9 base emitter near ground potential, which is the operating point of dc amplifier Q8.

The calibration standard circuit consists of voltage reference diode CR3, which is aged and selected for less than $\pm 0.006 \%$ drift in six months. The reference potential developed across this diode is compared with the output from series régulator Q4 by differential amplifier Q6. The inverted output from the collector of Q6A is coupled without inversion through a second differential amplifier, Q3-Q5, to series regulator Q4. The negative feedback thus provided holds the series regulator output voltage constant. This output is applied across a drift-compensated voltage divider network, from which is tapped the 1 volt output of the calibration standard.

### 3.19 REJECTION OF COMMON MODE AND SUPERIMPOSED NOISE

### 3.19.1 Rejection of Common Mode Noise

Common mode voltages are those dc and ac voltages that are common to both input leads of the Digital Voltmeter. These voltages result when the signal source ground and the Digital Voltmeter ground are not at the same potential. The potential difference between the signal source and the Digital Voltmeter grounds is the common mode voltage source. Unless precautions are taken, the common mode voltage source will cause unwanted currents to flow through the signal source impedance, producing a significant error in the signal voltage measurement. The proper way to eliminate this error is to break the common mode ground loop. In the HP2401C the ground loop is broken by a technique knownas guarding, in which the input to the Digital Voltmeter is completely isolated from the chassis and its associated ground.
"Figure 3-4 shows a typical unguarded circuit where the comtinon mode voltage source is represented by $\mathrm{V}_{\mathrm{c}}$. The ground loop currents of concern are
those through the LO input side of the Digital Voltmeter (i.e., through $\mathbf{R}_{\mathrm{r}}$, $\left.R_{L}, C 1\right)$; currents through the HI side are insignificant because of the high input impedance. With a typically large value of $C 1(0.1 \mu \mathrm{f})$ and $\mathrm{R}_{\mathrm{L}}=1 \mathrm{~K}$, the common mode rejection (defined as the ratio between the common mode signal and the voltage it causes to be superimposed on the signal source) is limited to about 29 db at 60 Hz . The common mode pickup can be minimized by utilizing a shield to shunt the common mode current path, but the additional rejection obtained is negligible because of the low value of $\mathrm{R}_{\mathrm{c}}$ with respect to the shield resistance.

Figure 3-5 shows the guarded input circuit used in the HP-2401C. In this instrument the common mode ground loop is broken by using a separate "guard" shield to isolate the analog part of the measuring circuit from the chassis. Except for a slight voltage drop in $\mathrm{R}_{\mathrm{s}}$, the guard operates at the potential of the signal source, resulting in a negligible current through C2. and thus a negligible current through $\mathrm{R}_{\mathrm{L}}$. The circulating ground current forced by $V_{c}$ is now effectively shunted away from the measuring circuit and flows through $\mathrm{R}_{\mathrm{s}}$ and C3. By utilizing the guard shield the leakage capacitance ( C 1 ) between the measuring circuit and the chassis has been reduced to less than 2.5 picofarads. Reduction of C1 to this low value yields a common mode rejection of 120 db at $60 \mathrm{~Hz} \mathrm{( } 160 \mathrm{db}$ at dc) even when the value of $R_{L}$ is as much as , 1000 ohms.

### 3.19.2 Rejection of Superimposed Npise

Superimposed noise voltages are primarily those unwanted ac signals that are superimposed on the input signal, usually as a result of electromagnetic plek-up from any ac field. When this occurs, the superimposed noise is added directly to the signal to be measured. Techniques used to combat common mode noise will not eliminate this type of noise since there is no ground loop to break.' The problem of superimposed noise is effectively dealt with in the HP-2401C by the process of integration, in which the input signal is integrated over a preselected sample period to obtain an average reading. If the period of the superimposed noise is such that its average value over the selected sample period is zero, no error results in the reading. For example, the fixed sample periods in the HP-2401C are multiples and submultiples of one second, and the average value of 60 Hz ac noise over a one second interval is zero. As a result the instrument provides infinite rejection at 60 Hz .

Figure 3-6 shows a graph of rejection versus noise frequency at three different fixed sample periods. Note the infinite rejection cusps such as occur at 60 Hz At other frequencies, for example at 55 Hz over a 0.1 sample period, $20^{\circ} \mathrm{db}$ of rejection is obtained. The rejection increases 20 db per decade ( 6 db per octave) increase in frequency.

Noise rejection characteristics around 60 (or 50 ) Hz for 1 second and 1 second sample periods are shown in Figure 3-7. As indicated, rejection is never more than 25 db poorer than that provided by an ideal Twin-T filter. With respect to the filter characteristic, rejection provided by the HP2401C improves with increasing deviation from 60 Hz .


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## SECTION IV MAINTENANCE

### 4.1 GENERAL

This section contains instructions for maintenance and servicing of the HP2401C Integrating Digital Voltmeter. Included are instructions for in-cabinet performance checks, air filter servicing, troubleshooting, instrument cover removal, repair, and calibration. These instructions are supplemented by a list of recommended test equipment (Table 4-1), a maintenance schedule (Table 4-2), test setup, troubleshooting, logic, parts location illustrations, and schematic diagrams (Figures 4-1 through 4-34).

### 4.2 IN-CABINET PERFORMANCE CHECKS

The In-Cabinet Performance Checks, Table 4-3, may be used to verify specifications of the equipment. The Performance Check Test Card, which follows Tảble 4-3, may be used as a permanent record of the instrument's performance when filled out. Values or answers in parenthesis below or to the right of test card entry blocks specify correct reading or reading tolerance. The entry numbers on the card correspond to the checks in Table 4-3. The checks in Table 4-3 and in Section 2.2 verify correct operation of all circuits in the HP-2401C and may be used:
a. as part of an incoming inspection check of instrument specifications;
b. periodically, as specified in Table 4-2;
c. as part of a troubleshooting procedure to locate malfunctioning circuits;
d. after repairs or adjustments, before returning the instrument to regu-- lar service.

During the Performance Checks the HP-2401C should be connected to the ac line through a variable voltage device so that line voltage may be varied $\pm 10 \%$ from nominal ( 115 or 230 vac ) to assure that the instrument operates correctly at various supply voltages.

1
Table 4-1. : hecommended Test Equipment (Sheet 1 of 3)

| Instrument Type | Required Characteristics | Use | Recommended Model |
| :---: | :---: | :---: | :---: |
| DC Standard | $0-1,0-10,0-100,0-1000$ vdc outputs accurate to $\pm 0.01 \%$ stability $\pm 0.003 \%$. | Performance check and calibration. | HP-740A or HP740B DC Standard Differential Voltmeter with 11054 A and $110-$ 55B Accessory Cables |

Table 4-1. Recommended Test Equịment (Sheet 2 of 3)

| Instrument Type | Required Characteristics | Use | Recommended Model |
| :---: | :---: | :---: | :---: |
| Standard <br> Frequency <br> Source | $100 \mathrm{kHz}, 1 \mathrm{~Hz}$ outputs accurate to $\pm 5$ parts in $10^{8}$. | Performance check and calibration of counter time base. | HP100E Frequency Standard |
| Oscilloscope | 10- MHz bandwidth, dualtrace plug-in, calibrated time base and vertical channel, ext sync capability. | Observe waveforms and measure timing relationships during performance checks, troubleshooting, and calibration. | HP-175A Oscilloscope <br> HP-1750A or HP- <br> 17.50B Dual-Trace <br> Amplifier <br> HP-10003A Voltage <br> Divider Probe (2) |
| DC Null <br> Voltmeter | Low range $0-3 \mu v_{2}$ infinite impedance at null, operation independent of ac line. | Null sensing and voltage measurements during.performance checks and calibration. | HP-419A DC Null <br> Voltmeter |
| Precision <br> Volt Box | 1:1, 10:1, 100:1, 200:1, 300:1, 400:1, 500:1,600: 1, 700:1, 800:1, 900:1, 1000:1 resistance ratios accurate to $\pm .001 \%$ at $1000 \Omega / \mathrm{v}$. | Performance checks and calibration. | Julie VDH-1000 or VDN-1000 Precision Voltage Divider |
| Variable Line Voltage Source with Meter | Variable from 103-127 vac (or 207-253 vac). | Performance checks. |  |
| 1 Volt Calibration Standard | 1 vdc output calibrated from primary standard to $\pm 0.001 \%$ accuracy or better. | Transfer standard for performance checks and calibration. | HP-735A Transfer Standard |
| Isolation Transformer | 50-60 cycle, 115v primary, 1:1 ratio. | Common mode noise rejection check. |  |
| Portable <br> Oscillator | Sine wave output from 5 Hz to 300 kHz , operation independent of ac power line. | Performance checks and calibration. | HP-204B Portable Oscillator |
| Test Oscillator | Sine wave output from 300 kHz to 1.2 MHz . | Performance check of M29. | HP-650A or HP651B Test Oscillator |

Table 4-1. 'mended Test Equipment (Sheet 3 of 3)

| Instrument Type | Ru. .ed Characteristics | Use | Recommended Model |
| :---: | :---: | :---: | :---: |
| AC Vacuum Tube Voltmeter | $10,30,100,300 \mathrm{mv}$ ranges, measurethent of rms voltage. | Performance check of superimposed nolse rejection. | HP-400D VTVM |
| Pulse <br> Generator | $-1 v, 2 \mu s$ pulse output at 1 kHz . | Performance check of frequency measurement sensitivity to pulse inpyt. | $\begin{aligned} & \text { HP-212A or HP- } \\ & \text { 8003A Pulse } \\ & \text { Generator } \end{aligned}$ |
| Square Wave Generator | Square wave output from 1 Hz to 20 kHz , 27 v p-p from $600 \Omega$ output. | Performance check of pulsed counter resetting from external source. | HP-211A Square <br> Wave Generator |
| BNC "T" <br> Adapter |  | - | HP-1250-0072 |
| Electronic Counter | Time interval measurements at $10 \mu_{\mathrm{s}}$ resolution. | Response time and measurement speed performance checks. | HP-523C or D or 5233L Electronic Counter |

Table 4-2 Maintenance Schedule

| Interval | Maintenance Operation |
| :--- | :--- |
| Daily or Each <br> Turn-On | For maximum accuracy of measurements perform preopera- <br> tional check and calibration per Section 2. 2. |
| Wepkly | Verify accuracy of internal time base per check 3 of Table 4-3. <br> If necessary; calibrate Internal time base per Section 4.7.5. <br> Clean air filter per Section 4.3. |
| Monthly* | Calibrate internal 1v reference per Section 4. 7.4. Perform checks |
| Every 6 Months |  |
| 1through 11 in Table 4-3. If necessary, calibrate overload detec- |  |
| tion per Section 4.7.3; calibrate input attenuator per Seqtion 4.7.8. |  |

*Shorten this interval if the instrument is operated more than 80 hours per month or if it is operated in a shop environment where no special care is taken to minimize airborne vapors and dust.


## 1. VOLTAGE MEABURIEMENT RANGLE

```
Full scajo rrangea:
\(0.1,1,10\),
```



``` 1000 V.
Overranging:
To 200 ', of fall acale oxcept on 1000 V rango.
Overload Protection: HP-2401C awltchee to 1000V range at 910\% (300-910\%) of full acalo.
```

n. Sot IP-240IC Power awitoh to $O N_{\text {g }}$ other conleola an followa:

PUNCTION: : $\quad$ VOLT.
RANGE:
SAM PLIE PIERIOD:
SAM PLING RATE:
18 1 C
100 KC STD (rear panil): IN'T.
b. Refer to Figure 4-1 and comect tho 4 and- OUTPUT torminala of the DC Blandard to the 14 and LO lerminnte of Ulo HP-2401C. Jumpe the GUARI tormimal to tho LO torminal.
c. Turn on the DC Btandard and an' it to providat de outputs ap lated bolow; the HP-2401C rendouts should be approxlmatol as followar

| DC standard Output | HP-240IC Rainge : |
| :---: | :---: |
| (Voits) | (Volts) |
| 1000 | 1000 |
| 100 | 100 |
| 10 | 10 |
| 1 | 1 |
| 0.1 | 0.1 |


| Approximato HP-2401C Display |  |
| :--- | :--- |
| +1000.00 | VOLTS |
| +100.000 | VOLTS |
| +10.0000 | VOLTS |
| +1000.00 | MILIIVOLTS |
| +100.000 | MILLIVOLTS |

d. Check HP-2401C (worranglag operathoir as follows:

| DC Standard Output (Volts) | HP-2401C Range (Volts) | Approximat | C HP-2401C Dioplay |
| :---: | :---: | :---: | :---: |
| 0.3 | 0.1 | + 700.000 | MILAIVOLTS |
| 3 | 1. | + 3000.00 | MILLVOLT8 |
| 30 | 10 | +30.0000 | VOLTS |
| 300 | 100 | +300.000 | volts |

e. Increase DC Standard output voltage alowly until OVERLOAD indicator lights on lip2401 C digital digplay. Sot IIP-2401C RANGE switch to 1000 V and record reading, which should be $+312.5,7.5$ VOLTS. If ficprect, callbrate overload detection per Bection 4.7.3.
2. VOLTAGE MEASUIREMENT - INTEGRATION

The HP-2401C displays the true integral of the input aignal with correct polarity even If the signal crosses through zero during the sample period.
a. With MP-2401C on and operating, set controla as follows:

| SAM PLE PEIRIOD: | SIOP. |
| :--- | :--- |
| STORE/DIBPLAY (rear panel): | DISPLAY. |
| FUNCTION: | VOLT. |
| RANGE: | IN'T-IV. |

b. Set HP-2401C SAMPLE PERIOD Bwiteh to START until 0-digit negative count is accumulated; thon set switch to STOP.

Table 4-9. In-Cubinet Porformance Checks Std © Opti" 20 Instruments (Sheot 2 of 15)
2. c. Sot HP-240IC RANGE awitch to INT+1V and reset SAMPLE PERIOD awitch to START. Observgloounting down to zero (viatble on the two mont mignificant digita), reversal of polaritifindication to $t$, and count up of +voltage. Set BAMPLE PERIOD ewitch to STOP and recerd observationa.

NOTE
IIIT 1 dealred to view this procese in greater detill, apply an input voltage that is about $1 / 10$ or $1 / 100$ of the full acale range selected. After the indial count is accumulated, reverce this input.

## 9. INTERNAL TME BABE

Frequency: 100 kHz .
Stabillity: Aging Rate $< \pm 2$ parte in $10^{6}$ per week. Temperature $< \pm 100$ parts in $10^{\circ}$ over range of $10-50^{\circ} \mathrm{C}$.
a. Turn on flp-2401C, the Frequency Standerd, and the Oacilloacope; note time.
b. Set $100 \mathrm{~K} \backslash$ 8TD wwith on rear $\alpha$ HP-2401C to INT poaltion.
c. Connect anC cable from the 100 KC 8TD OUTPUT/INPUT receptacle, J3, on the rear

Tof the HP-2401C to a vertical input of the Oreilloncope.
d. Bynchronize the Oecilloscope externally from the 1 cpa output of the Frequency Standard.
e. Sot Oncilloscope for difplay of the $1.2 \mathrm{~V} \mathrm{p}-\mathrm{p}, 100 \mathrm{kHz}$ equare wave time base output from the HP-2401C at $1 \mu 8 E C / C M$ aweep rate.

1. After the MP-2401C has been operating for at least an hour, observe square wave display on Oacilloscope to determine degree of drift, if any. Left drift is - , right drift is t.
g. The horizontal drift of the equare wave in CM/BEC is the difference between the Standard Frequency and the Counter time base irequency in parts in $10^{6}$. Determine this difference and record It on the Performance Check Tpiat Card.

## NOTE A

Tomperature muat be within $\pm 5^{\circ} \mathrm{C}$ a the temperature at which internal time base oacillator was calibrated. I a record $\alpha$ the temperature and date of laat calibration is not avallable, the irequency offset should not be conaldered drift or aging rate of the 100 kHe cryatal.

NOTE $B$
Yr diII of the internal time bace is greater than $\pm 2$ parta in $10^{6}$, recalibrate per Section 4.7.5.
h. Check long term atability by repeating the procedure $\alpha$ ateps a through $g$ one week later.

1. II a preciecly controlled temperiture chamber is avallable, check temperature stability by repeating the procedure of steps a through g after the HP-2401C has been on and operating at $10^{\circ} \mathrm{C}$ for at leat $1-1 / 2$ hours, but use $10 \mu \mathrm{SEC} / \mathrm{CM}$ sweep rate. Repeat after $1-1 / 2$ hour warmup at $50^{\circ} \mathrm{C}$. The horizontal drift of the equare wave in CM/SEC is the difference between the atandargfrequency and the Counter ume base in 10 parts In $10^{6}$. Determine frequency difference, which ahould be no greater than $\pm 100$ parts in $10^{6}$.

Table 4-3. In-Cablnet Performance Checks Std \& Opt. 29 Instruments (Sheet 3 of 15)
4. INTERNAL CALIBRATION SOURCE

Voltage: $\quad$ IV $\pm .002 \%$ (after factory adjustment).
Drift: $\quad< \pm .006 \%$ in six months.
Temperature Coefficient: $\quad 10-40^{\circ} \mathrm{C} \pm .001 \%$ per ${ }^{\circ} \mathrm{C}$. $\quad 40-50^{\circ} \mathrm{C} \pm .0015 \%$ per ${ }^{\circ} \mathrm{C}$.
a. Set DC Standard for IV output.
b. Zero the HP-2401C per the procedure in Section 2.2.2.
c. Connect the DC Standard, DC Null Voltmeter, IV Calibration Standard, Precision Volt Bax, and HP-2401C as shown in Figure 4-1(A). Operate the DC Null Voltmeter from its internal batteries; do not connect it to the ac line.
d. Set the DC Standard output voltage to produce a null on the most sensitive range of the DC Null Voltmeter.
e. Set the HP-2401C to IV RANGE and set the CAL+ adjustment for +1000.00 MILLIVOLTS indication on the digital readout.

1. Reverse the connections of leads 2 and 4 to the HP-2401C HI and LO terminals and set the CAL- adjustment for -1000.00 MILLVOLTS indication on the digital readout.
g. Set the HP-2401C RANGE awitch to INT-1V and record the digital readout. This reading thould be $-1000.00 \pm 0.10$ MILLIVOLTS (maximum drift of $\pm 0.006 \%, \pm 0.002 \%$ initial calibration, $\pm 0.001 \%$ accuracy of external standard, $\pm 1$ digit).

NOTE A
If reading is not within $\pm 0.10 \mathrm{mv}$ of 1000 MIILIVOLTS, recalibrate the internal standard per Section 4.7.4 and repeat steps a through g.

NOTE $B$
Immediately after calibration, at the calibration temperature, the digital readout should be within $\pm 0.05 \mathrm{mv}$ of -1000.00 MILLIVOLTS (initial calibration to $\pm 0.002 \% \pm 1$ digit.
h. Check long term stabllity by repeating the procedure $\alpha$ atepa a through $g$ monthly for six months.

NOTE
If a precieely controlled temperature chamber in available, the temperature coefficient of the internal calibration source may be checked per the procedure of etep: i through 1.

1. Hold the HP-2401C on and operating at $40^{\circ} \mathrm{C}\left( \pm 1^{\circ}\right)$ for at least $1-1 / 2$ hours.
j. Repeat ateps a through d , above, to obtain a $1 \mathrm{~V} \pm 0.001 \%$ external atandard.
k. Read voltage of external atandard on IV range; then read voltage from internal calibration mource on corresponding INT IV.range and aubtract the difference in readinge. This difference should be no greater than $\pm 0.17 \mathrm{mv}$.
2. Repeat the procedure of steps $i$ through $k$, above, after $1-1 / 2$ hour warmup at $50^{\circ} \mathrm{C}$ and at $10^{\circ} \mathrm{C}$. The $50^{\circ} \mathrm{C}$ difference should be no greater than $\pm 0.30 \mathrm{mv}$; the $10^{\circ} \mathrm{C}$ difference should be no greater than $\pm 0.17 \mathrm{mv}$.

Table 4-3. In-Cabinet Performance Checks Std \& Opt. 29 Instruments (Sheet 4 of 15)
6. VOLTAGE MEASUREMENT - FULL SCALE ACCURACY

At $25^{\circ} \mathrm{C}$ : $\quad \pm .01 \%$ rdg $\pm .005 \%$ fs $\pm 1$ digit (1).
Temperature Coefficients: $\quad 10-40^{\circ} \mathrm{C}, \pm .001 \% \mathrm{rdg}$ per ${ }^{\circ} \mathrm{C}$
$40-50^{\circ} \mathrm{C}, \pm .0015 \% \mathrm{rdg}$ per. ${ }^{\circ} \mathrm{C}$ (2).
$0.1 V$ range, $\pm .00 \% \%$ rdg $\pm .0005 \%$ is per ${ }^{\circ} \mathrm{C}$
Other ranges, $\pm .002 \%$ rds $\pm .0002 \%$ fs per ${ }^{\circ} \mathrm{C}$
(1) Holds for all ranges at $25^{\circ} \mathrm{C}$, ascuming daily calibration against internal atandard, calibration $\alpha$ internal etandard every aix monthe, line voltage variation no greater than $\pm 10 \%$.
(2) When calibrated against internal standard at operating temperature.
(3) Over the range of $10-50^{\circ} \mathrm{C}$ when calibrated againet internal atandard at $25^{\circ} \mathrm{C}$.
a. After 1-1/2 hour warmup at $25^{\circ} \mathrm{C}$ with instrument zeroed per Section 2.2 .2 and controls set an epecffied below, set the CAL-aduatment for -1000.00 MILLIVOLT reading on
the HP-2401C didital dieplay.
100 KC 8ID (rear panel):
FUNCTION:
RANGE:
SNMPLE PERIOD:
SMMPLING RATE:
INT.
VOLT.
INT-IV.
1 sEC.
Clockwise from STOP.
b. 8et the IPP-2401C RANGE witch to DNT+1V and set the CAL+ adjustment for $\mathbf{+ 1 0 0 0 . 0 0}$ MILIVOLT reading on the digital dieplay.
c. Set the BP-24010 to IV RANGE and act the DC 8iandard to procuce a null on the most condtive range of the DC Null Voltmeter (connections are as shown in Figure 4-1 (A), except for leade 2 and 4 to the HP-2401C, which are reversed, as at the end of check 4).

NOTE A
TII voliage reading tolerances noted in this check include the potential inaccuracy of the external voitage atandard ( $\mathbf{~} \mathbf{0 . 0 0 1 \%}$ for $1 V, \pm 0.00 \% \%$ for other voltages).

NOTE B
If any range is out of tolerance at $25^{\circ} \mathrm{C}$ ambtent, calibrate per section 4.7.8.
d. Record the naxt readout. This reading ahould be within $\pm 0.17 \mathrm{mv}$ of $-1000.00 \mathrm{MILLI}-$ voLT8.
e. Connect leads 2 and 4 exactly as shown in Figure $4-1(A)$ and record the next readout. This reading ehould be within $\pm 0.17 \mathrm{mv}$ of +1000.00 - MILLIVOLT8.

1. Change compections to thooe shown for. IV check in Figure 4-1(B) and eet the HP-2401C RANGE switch to. IV. Record the next digital readout. This reading should be within $\star 0.018 \mathrm{mv}$ of $\pm 000$. 108 MILLVOLT8.

## NOTE

Trive io0x inpat impedance of the BP-2401C on the. IV RANGE loads the output of the Preciaion Volt Box so that the input voltage $18+99.108 \mathrm{mv}$. The accuracy tolerances total $\pm 18 \mu v$ for this reading, scale, and digits; including the $\pm 0.002 \%$ tolerance of the voltage source.

Table 4-3. In-Cabinet Performance Checks Std \& Opt. 29 Instruments (Sheet 5 of 15)
6. g. Change connections to those shown for 10V check in Figure 4-1(B). Set the HP-2401C RANGE switch to 10 V and set the DC Standard to exactly 10 V , as indicated by a null reading on the most sensitive range of the DC Null Voltmeter.
h. Record the next reading. This reading should be within $\pm 0.0018 v \alpha+10.000$ VOLTS.
i. Change connections to those shown for 100V check in Figure 4-1(B). Set the KP-2401C RANGE switch to 100 V and set the DC Standard to exactly 100 V , as indicated by a null reading on the most sensitive range d the DC Null Voltmeter.
j. Recard the next reading. This reading should be within $\pm 0.018 \mathrm{v}$ of +100.000 VOLTS.
k. Change connections to those shown for 1000V check; set the HP-2401C RANGE switch to 1000 V and set the DC Standard to exactly 1000 V , as indicated by a null reading on the most sensitive range of the DC Null Voltmeter.

1. Record the next reading. This reading should be within $\pm 0.18 \mathrm{v} \boldsymbol{\alpha}+1000.00$ VOLTS. NOTE
If a precisely controlled temperature chamber is available, the valtage measurement temperature coefficient may be checked per the procedure of steps $m$ through 0.
m. Hold the HP-2401C on and operating at $40^{\circ} \mathrm{C}\left( \pm 1^{\circ}\right)$ for $1-1 / 2$ hours.
n. Repeat steps c through e , and determine the difference between the readings for 1 V input at $25^{\circ} \mathrm{C}$ and $40^{\circ} \mathrm{C}$, which ahould not be greater than $\pm 0.35 \mathrm{mv}$.
2. Repeat ateps $c$ through e after 1-1/2 hour warmup at $50^{\circ} \mathrm{C}$ and after $1-1 / 2$ hour warmup at $10^{\circ} \mathrm{C}$. The $50^{\circ} \mathrm{C}$ difference ahould be no greater than $\pm 0.57 \mathrm{mv}$; the $10^{\circ} \mathrm{C}$ difference should be no greater than $\pm 0.35 \mathrm{mv}$.
3. VÖLTAGE MEASUREMENT - LINEARITY
$\begin{array}{ll}\text { At Less Than Full scale: } & \pm .01 \% \mathrm{rdg} \pm .005 \% \text { is } \pm 1 \text { digit. } \\ \text { At } 3 \text { Times Full Scale: } & \pm .025 \% \mathrm{rdg} \pm 1 \text { digat. } \\ \text { At } 2 \text { Times Full Scale: } & \pm .02 \% \mathrm{rdg} \pm 1 \text { digit. }\end{array}$
With ambient temperature at $25^{\circ} \mathrm{C}$, line voltage variation no greater than $\pm 10 \%$.
a. After 1-1/2 hour warmup at $25^{\circ} \mathrm{C}$ and with instrument zeroed and calibrated per Sections 2.2.2 and 2.2.3, set controls as specified below.

100 KC STD (rear panel): INT. FUNCTION:
RANGE:
VOLT.
RAMPLE 1000 V.
SAMPLE PERIOD: 1 SEC.
SAMPLING RATE: Clockwise from STOP.
b. Connect the DC Standard, DC Null Voltmeter, 1V Calibration Standard, Preciaion Volt Box, and HP-2401C for $10 \%$ is interval linearity checks as shown in Figure 4-1(A) and (B) and set the DC Standard for 900 V output.

Table 4-3. In-Cabinet Performance Checks Std \& Opt. 29 Instruments (Sheet 6 of 15)
6. c. In turn, connect lead from HI input terminal of the HP-2401C to each of the terminals af the Precision Volt Box that are listed following this step and reset output from the DC Standard for a precise null reading on the most sensitive range $\alpha$ the DC Null Voltmeter. At each point, record the reading.

| Precision Volt Box Terminal | \% Full Scale | Reading (Volts) | Tolerance (Volts) |
| :---: | :---: | :---: | :---: |
| 800:11 | \% 80 | +0800.00 | $\pm 0.17$ |
| 800:1 \% | 80 | +0800.00 | $\pm 0.16$ |
| 700:1 , 4 | 70 | +0700.00 | $\pm 0.14$ |
| 600:1 | 60 | +0600.00 | $\pm 0.13$ |
| 500:1 | 50 | +0500.00 | $\pm 0.12$ |
| 400:1 | 40 | +0400.00 | $\pm 0.11$ |
| 300:1 | 30 | +0300.00 | $\pm 0.10$ |
| 200:1 | 20 | +0200.00 | $\pm 0.08$ |
| 100:1 | 10 | +0100.00 | $\pm 0.07$ |

## NOTE

AII voltage reaf, ing tolerances noted in this check include the potential inaccuracy of the external voltage standard ( $\mathbf{~} 0.002 \%$ ).
d. Set the DC Standard for output of approximately 3 vdc and change connections to those shown in Figure 4-1(B) for 3X check.
e. Set the DC Standard output to exactly 3 vdc , as indicated by a null reading on the most sensitive range of the DC Null Voltmeter.
f. Set the HP-2401C RANGE awitch to $1 V$ and record the next reading. This reading should be within $\pm 0.82 \mathrm{mv}$ of +3000.00 MILLIVOLTS.
g. Reverse the connections to the HI and LO terminals of the HP-2401C and record the next reading, which should be $-3000.00 \pm 0.82$ MILLIVOLTS.
h. Change connections to those shown in Figure 4-1(B) for 2X check.

1. Set the DC Standard to exactly $2 V$, as indicated by a null reading on the most sensitive range of the DC Null Voltmeter. Record the next reading. This reading should be within $\pm 0.45 \mathrm{mv}$ of -2000.00 MILLVOLTS.
j. Reverse the connections to the HI and LO terminals of the HP-2401C and record the next reading, which should be $+2000.00 \pm 0.45$ MILLVOLTS.

## 7. VOLTAGE MEASUREMENT - REJECTION OF COMMON MODE NOISE

140 db .
a. With the HP-2401C on and operating, connect only the equipment shown in Figure 4-1(C). Set variable voltage transformer for minimum output voltage.
b. On the HP-2401C, select . IV RANGE and 1 SEC SAMPLE PERIOD. Set SAMPLING RATE control fully clockwise and record the next reading.
c. Increase output voltage from the variable transformer to maxdmum, or until the reading on the HP-2401C changes more than $\pm 2$ digits. Determine and record rms voltage across secondary of the isolation transformer.

Table 4-3. In-Cabinet Performance Checks Std \& Opt. 29 Instruments (Sheet 7 of 15)
7. d. Repeat the procecture of steps a through $c$ for .1 and .01 SEC SAMPLE PERIOD. The common mode line frequency signal required to produce the apecified change in reading should be greater than 100 V rms at each sample period.
8. VOLTAGE MEASUREMENT - RENECTION OF SUPERIMPOSED NOISE

At $55 \mathrm{~Hz}, 0.1 \mathrm{Sec}$ Sample Period: $>20 \mathrm{db}$. At $550 \mathrm{~Hz}, 0.1 \mathrm{Sec}$ Sample Period: $>40 \mathrm{db}$.
(Increases 20 db per decade increase in frequency.)
a. With HP-2401C on and operating, connect test equipment as shown in Figure 4-1(D).
b. Set controls of the HP-2401C as follows:

| FUNCTION: | FREQ. |
| :--- | :--- |
| SAMPLE PERIOD: | 1 SEC. |
| SAMPLING RATE: | Fully clockwise. |
| ATTENUATION: | Fully clockwise. |

c. Turn on the Portable Oscillator and set it to provide 0.055 kHz output, as counted by the HP-2401C.
d. On the HP-2401C reset controls as follows:
$\begin{array}{ll}\text { FUNCTION: } & \text { VOLT. } \\ \text { RANGE: } & 10 V\end{array}$
SAMPLE PERIOD: . 1 SEC.
e. Set the Portable Oscillator for minimum output amplitude and note the reading dieplayed by the HP-2401C.
f. Slowly increase the Portable Oscillator output amplitude until the 10 mv dight (second from right) changes.
g. Determine and record the rms output from the trancidrmer eecondary. More than 100 MV rms ( 20 do greater than the eecond, 10 mv digit) should be required to procuce the specified change in the HP-2401C reading.
h. Repeat steps a through c, above, but set the Portable Oacillator to provide 0.550 kHz output as counted by the HP-2401C.
i. Repeat steps $d$ through $g$, above. More than $1 V$ rms ( 40 do Geater than the 10 mv digit) should be required to produce the epecified change in the HP-2401C reading.

NOTE
If desired, a similar technique can be used to verify the noise rejection of the HP2401C for other sample periods and other frequencies. See Figure 3-6 for superimposed noise rejection characteristics with respect to nolse frequency and aample period.

Table 4-3. In-Cabinet Performance Checks Std \& Opt. 29 Instruments (Sheet 8 of 15)

## 9. FREQUENCY MEASUREMENT RANGE - 5 Hz TO 300 KHz (TO 1.2 MHz WITH OPTION 29

a. Set HP-2401C Power switch to ON, other controls as follows:

100 KC STD (rear panel): INT. FUNCTION: FREQ.
SAMPLE PERIOD:
.1 8EC. SAMPLNG RATE: Clockwite from STOP. ATTENUATION:

Fully clockwise.
b. Connect output of Portable Oscillator to HP-2401C FREQ INPUT and to an Oscilloscope with a BNC "T" connector.
c. While holding Oscillator output amplitude constant at 0.1 V rms $(0.28 \mathrm{~V} \mathrm{p}-\mathrm{p})$, vary the output frequency downward from 100 kHz to determine the lowest frequency that is counted reliably. This frequency should be 5 Hz or lower. Then increase Oscillator frequency to determine highest frequency that is counted reliably. This frequency should be 300 kHz or higher. Record loweat and highest frequencies.

NOTE:
For high end testing of HP-2401C-29 instruments, substitute a Test Oscillator for the Portable Occillator and increase frequency from 300 kHz with amplitude set at 0.5 V rms ( $1.4 \mathrm{~V} \mathrm{p}-\mathrm{p}$ ) to determine and record the higheat frequency that is counted reliably. This frequency should be 1200 kHz or higher.

## 10. FREQUENCY MEASUREMENT - SENSITIVITY

Sine Wave Input:
Pulse Input (Std. or Option 29):
Std. HP-2401C, 0.1 V rms (max.) at 300 kHz .
HP-2401C-29 0.5V rms (max.) at 1 MHz .
Polarity, negative or positive.
Minimum peak amplitude, IV (max.). Minimum duration, $2 \mu \mathrm{~m}$ (max.),
a. With HP-2401C on and operating and its controls set as follows. increase amplitude of 300 kHz Oscillator output from zero until consistent measurement is obtained.

| 100 KC STD (rear panel): | INT. |
| :--- | :--- |
| FUNCTION: | FREQ. |
| SAMPLE PERIOD: | . SEC |
| SAMPLING RATE: | Clockwise from STOP. |
| ATTENUATION: | Fully clockwise. |

b. Determine and record the rms output voltage from the Oscillator (use AC VTVM); the voltage should be no greater than 0.1 v rms.
c. Check 1 MHz sensitivity of Option 29 instrument $w$ ith the Test Oscillator set for 999.999 kHz output. Increase Oscillator output from zero until consistent measurement is obtained. Then determine and record the outpat voltage, which should be no greater than 0.5 v rms.
NOTE: Perform steps $d$ through $f$ only if trigger circuit has been adjusted for pulse operation according to Section 4.7.11.
d. Connect output of Pulse Generator to HP-2401C FREQ INPUT and to input of Oscilloscope with a BNC "T" connector. Set Pulse Generator for negative lv. $2 \mu \mathrm{~s}$ pulse with 1 kHz repetition rate.
e. Increase pulse amplitude from minimum until consistent measurement is obtained. Record the peak amplitude, which should be no greater than 1 v .
f. Set pulse amplitude at $1 v$ and increase pulse duration from minimum until consistent measurement is obtained. Record the duration, which shquid be no greater than $2 \mu \mathrm{~s}$.

Table 4-3. In-Cabinet Performance Checks Std \& Opt. 29 Instruments (Sheet 9 of 15)

## 11. RESPONSE TIME AND MEASUREMENT RATE

Reaponse time and selected ample period determine maximum measurement rate for data system applications, as follows:

a. Connect test equipment as indicated in the aketch. Close 81 to energize K1. Set DC Standard for 20V output. With HP-2401C on and operating, set controls as follows:

FUNCTION:
RANGE:
SAMPLE PERIOD:
SAMPLING RATE:
100 KC STD (rear panel):

VOLT.
10V.
1 SEC.
Clockwise from STOP. INT.,

b. Set the Electronic Counter for time interval measurement in ms, etarted by poedtivegoing input and atopped by negative-guing Input. Time interval readinge on the Electronic Counter should be $29.67 \mathrm{~ms} \pm 0.02 \mathrm{~ms}$. Voltage readings on the HP-2401C should be approvimately $-20,0000$ VOLTS. Record voltage reading, then set the BP-2401C SAMPIING RATE control to STOP.
c. Open 81 to do-energize K1, disconnecting the 20 V input to the RP-2401C. Then reset the HP-2401C and the Electrgic Counter. The HP-2401C should now read OV $\pm 1$ count.
d. Close 81 to energise K1, connecting the -20 V . Then record the reading on the Electronic Counter and the difference between this voltage reading on the RP-2401C and that previcualy recorded. The Counter reading should be $9.67 \mathrm{~ms} \pm 0.02 \mathrm{~ms}$, and the voltage reading on the HP-2401C should be within $\pm 0.0002$ VOLT8 of that recorded in atep $b$.

Table 4-3. In-Cabinet' Performance Checks Std \& Opt. 29 Instruments (Sheet 10 of 15)
11. e. Set the Electronic Counter for time interval measurement stopped by positive-going input and repeat steps $c$ and d at . 01 SEC, . 1 SEC, and 1 SEC sample periods. Record the Electronic Counter readings, which should be as follows $( \pm 0.02 \mathrm{~ms}$ ):

| Sample Period ( Sec | Time Interval Reading (M8) |
| :---: | :---: |
| . 01 | 19.67 |
| . 1 | 109.67 |
| 1. | 1009.67 |

12. TME BASE - OUTPUT (Rear Panel)

100 kHz equare wave.
Negative 1.2v p-p.
1 K output impedance.
a. With HP-2401C on and operating and 100 KC STD switch set to INT, connect Oscilloacope to rear panel 100 KC STD OUTPUT/INPUT receptacle, J3.
b. Oacilloscope should dieplay a 100 kHz square wave, negative-going to 1.2 v . Record the signal amplitude.
c. The output impedance is determined by a fixed value 1 K resistor ( R 15 ), which can be seen in the assembly A6 ctrcuit diagram, Figure 4-11.
13. TIME BASE - EXTERNAL INPUT (Rear Panel)

2v p-p madmum into 1.2 K .
a. With the HP-2401C on and operating, set controls as follows:

100 KC STD (rear panel): EXT.
FUNCTION:
SAMPLE PERIOD: 1 SEC.
SAMPLING RATE: Clockwise from STOP.
ATTENUATION: Fully clockwise.
b. Connect 100 kHz 2v p-p output, ffom the Fortable Oscillator to the HP-2401C FREQ INPUT and 100. KC STD OUTPUT/INPUT receptacle with a BNC "T" connector.
c. Increase Oncillator output amplitude from minimum to the point where consistent measurement is obtained.
d. Determine and record the p-p amplitude of the Oscillator output. Amplitude should be no greater than 2 v p-p.
e. The input impedance is determined by a fixed value 1.2 K resistor (R6), which can be seen in the assembly A6 circuit diagram, Figure 4-11.
14. RECORDNG OUTPUTS - BCD DATA

6 dights.
4-line 4-2'-2-1 code.
" 0 " atate level, -35 to $-24.5 v ; " 1$ " atate level -2.5 to $0 v$. source impedance 100K.

Table 4-3. In-Cabinet Performance Checks Std \& Opt. 29 Instruments (Sheet 11 of 15)
14. a. With the HP-2401C on and operating, set controls as follows:

| 100 KC STD (rear panel): | INT. |
| :--- | :--- |
| SAMPLE PERIOD: | START. |
| ATTENUATION: | CHECK. |

b. Connect a $10 \mathrm{pf}, 10 \mathrm{X}$ attenuation, 10 M probe to one channel of the Oscilloscope.
c. With the probe, verify " 0 " and " 1 ", state levels for each data digit at the following pins of J2. These levels will be represented by a 22 to 35 v p-p square wave. (The square wave frequency differs at each pin of J2.) Record a yes on the test card for each correct 4-line digital output.

| $\underline{\text { Digit }}$ | Decade |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $10^{\circ}$ | A11 | J2 Pins: | 3 | 4 | 28 | 29 |
| $10^{1}$ | A12 | $\frac{\text { of }}{}$ | 5 | 6 | 30 | 31 |
| $10^{2}$ | A13 |  | 7 | 8 | 32 | 33 |
| $10^{3}$ | A14 |  | 9 | 10 | 34 | 35 |
| $10^{4}$ | A15 |  | 11 | 12 | 36 | 37 |
| $10^{5}$ | A46 |  | 13 | 14 | 38 | 39 |

d. The source impedance is determined by fixed value 100 K resistors, which can be seen In the assembly A11-15, 46 circuit diagram, Figure 4-17.
15. RECORDING OUTPUTS - BCD FUNCTION

1 digit.
4-line 4-2'-2-1 code.
" 0 " state level, -35 to -24.5 v ; " 1 " state level -2.5 to. 0 v . Source impedance 33K.
a. With the HP-2401C on and operating, set as specified below to determine and record de' function levels at the following pins of J2:

|  |  | J2 Pins: | 41 | 40 | 16 | 15 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Control Settings | Function | Code: | 4 | $2{ }^{\prime}$ | 2 | 1 |
| VOLTS, INT+1V | +VDC |  | 0 | 0 | 0 | 1 |
| VOLTS, INT-曾 | -VDC |  | 0 | 0 | 1 | 0 |
| FREQ | KC |  | 0 | 0 | 1 | 1 |
| EXXT SEL, 1Y | K ${ }^{\text {® }}$ (W/HP-2410B) |  | 0 | 1 | 1 | 0 |
| EXT SEL, 1V | M ${ }^{\text {(W/HP-2410B) }}$ |  | 0 | 1 | 1 | 1 |
| VOLTS, 1V* | OVERLOAD |  | 1 | 1 | 1 | 1 |
| EXT SEL, 1V | VAC (W/HP-2410B) |  | 1 | 0 | 0 | 1 |

(*)*With de input sufficient to produce OVERLOAD indication.
b. The source impedance is determined by fixed value 33 K resistors, which can be seen in the assembly A22 circuit diagram, Figure 4-23 or 4-24.
16. RECORDING OUTPUTS - BCD DECIMAL POINT

1 digit.
4-line 1-2'-2-1 code.
" 0 " state level -35 to $-24.5 v ;$ " 1 " state level -2.5 to $0 v$. Source impedance 33K.

Table 4-3. In-Cabinet Performance Checks Std \& Opt. 29 Instruments (Sheet 12 of 15)
a. With the HP-2401C on and operating, set FUNCTION switch to VOLT, other controls as specified below; determine and recard dc decimal levels at the following pins of J2; shortcircuit HI, LO, and GUARD terminals to assure all zeros reading.

*With HP-2411A Guarded Data Amplifier operated at $+10 \mathrm{gain}(10$ MILLIVOLTS full scale); FUNCTION switch set to EXT SEL position; HP-2411A Decimal Point Logic Card A30 installed.
b. Set HP-2401C FUNCTION switch to FREQ, ATTENUATION control Just clockwise from switched CHECK position, other controls as specifled below; use DC Null Voltmeter to check decimal levels at the following pins of J 2 :

Sample Period

| mple Period | Decimai |
| :---: | :---: |
| (Sec) | Position |
| . 01 | 00000.0KC |
| . 1 | 0000.00KC |
| 1. | 000.000KC |
| STOP | 000000 |


| J2 Pins: | 27 | 26 | 2 | 1 |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Code: | 4 | $2{ }^{\prime}$ | 2 | 1 |  |
|  | 0 | 0 | 0 | 1 | $\left(10^{-1}\right)$ |
|  | 0 | 0 | 1 | 0 | $\left(10^{-2}\right)$ |
|  | 0 | 0 | 1 | 1 | $\left(10^{-3}\right)$ |
|  | 1 | 0 | 0 | 1 |  |

c. The source impedances are determined by fixed value 33 K resistors, which can be seen in the assembly A22 circuit diagram, Figure 4-23 or 4-24.
17. RECORDING OUTPUTS - REFERENCE LEVELS
" 0 " State Level: -24.5 to -21.5 v , source impedatice $800 \Omega$.
"1" State Level: -5 to $-4 v$, source Impedance $380 \Omega$.
a. With the HP-2401C on and operating (FUNCTION: VOLT; RANGE: 10V), connect HP-2401C LO terminal to J2, pin 50 and connect $H I$ terminal to J 2 pins as specified below and re card readings.

HI Terminal to J2 Pin
25
24

Reference Measured

+ (iI" Level)
- ('"0" Level)

Tolerance of Reading Range
-4.00 to -5.00 V
-24.50 to -21.50 V
b. The source impedances are determined by fixed value $1.2 \mathrm{~K}, 2.0 \mathrm{~K}$, and $470 \Omega$ resistors (A7R13-R15) which are shown in the A7 and A29 circuit diagram, Figure 4-12.
18. RECORDING OUTPUTS - RECORD COMMANDS

$$
\begin{aligned}
& \text { " } 0 \text { " State Level: }-24.5 \text { to }-21.5 \mathrm{v} \text {, source impedance } 5 \mathrm{~K} \text {. } \\
& \text { " } 1 \text { " State Level: } \\
& -5 \text { to }-I v, \text { source impedance } 1 \mathrm{~K} \text {. }
\end{aligned}
$$

Tablo 4-3. In-Cablnot Porformanod Chookn Bid a Opx. 20 Indrumontw (Bliod is of 10)
18. 6. With the HP-8401C on and operating, act oontrole ne followat

BAMPLIE PIEROD;
BAMPLNNO RATE: 100 XC TTD (rear panel):
.01 BEC
Pully olookwice.
INT.
b. Connect Onoilloecops to pinc 11 and 28 to verify " 0 " and " 1 " date levala. The Oecilloecope will dieplay the owitghing betweon theme levele at a auare wave with 20.0 to 80.0 v p-p amplitude. Rwoord p-p algnal amplitudes.
c. The "1" etate couroe Impedanoe is determined by fixed value IK reatetors Re and RT, which are show in the A17 and A18 oircull diagram, Figure 4-10, conneoted to pina 11 and 17 at A17. The 'g" atate cource impedince is determined ty fixed value 8. 0x realetore (A17R18 and A17M1), which are also ahown In Figure 4-10.
19. EXTERNAL PROORAMMING - HOLD OFF DNPUT'

Hold sato: $\quad+1$ to +18 r at 4.6 ma .
Non-Hold Blate: -1 to -8fv.
a. With HP-2401C on and operating, eot controle an followe:


100 KC ETD (rear panel); FUNCTION: INT. RANOE:
$\lambda$ volut. Troneldigilay (roar parint iv. wrong oisplay (roar panol): RAMPLE PERUOD: SAMPLINO RATE: DIEPLAY. . 01 BEC. Pully olock iffeo.
b. Connect a voltage eource that can be varied oonlinuoualy from -iv do to tiv de to J1,
 -iv do outpult.
c. Blowly aghint cource for more poaltive (leas negative)' output until the HP-2401C mean-urement-dilplay cycle atopa. Then meagure and record the hold-off voltage whlle the voltage eource is alll oonnected to the HP-2401C. ,
20. EXT ERNAL PRTOCRAMMINO - FUNCTION INPUT

Input Requiroment: External contact closire to ground or clamp that holde Input pin at -IV do or more poatuve while eupplying 70 ma . With no programming, VOLTS.
-Programmable function, FREQ and with HP-2410B Unile Coupling Card AO inotalled, 0, AC Normal, and AC Fant.
a. With HP-2401C on and operating, eot controla as followa:

FUNCTION:
SAMPLE PERIOD: RANOE:

EXT BEL.
1 BEC.
1V.
b. Record lighted MP-2401C unts diaplay which ahould be VOLTB.

Table 4-3. In-Cubinot Porformance Checks std a Opl. 20 Indrumente (Bheot 14 of 15 )

|  | 0. Conneot a jumper from J1, pin 2, to each of the following other JI ping in forn, recording HP-8401C unitio deplay lighted at each toet. $y^{\prime}{ }^{\prime}$ |
| :---: | :---: |
| 1 |  |
|  | a. With HP-2401C on and operating, 'ed controls an follows: <br> TUNCTION: VOLT. <br> SAMPLINO RATE: <br> - RAMPLE PRRIOD: <br> Clock wiee from STOP: <br> EXT 5 L. <br> RANOE: <br> ETT+1V. <br> b. Connect a jumper trom J1, pla Z , to each of the following other J1 plne in turn, re.cording aldital readout at eech tock. |
|  | EXTERNAL PROCRAMMINO - RANGE INPUT <br> Input Requirement: <br> External contact alowire to ground or clamp thit holds in- <br> Programmable Ranges: put pin at -1V de ar more poaltive while eupplying 70 ma . $.1,1,10,100,1000 \mathrm{~V}$. <br> . 01 V w/hp-2411A Dectmal Point Logic Card Aso Installed. <br> 10M w/hp-2410B Unit Coupling Card A9 installed. |

a. With the HP-2401C on and operating and controle act an epecified below, connect a jumper between the II and LO terminals.

| FUNCTION: $f$ | EXT BEL. |
| :--- | :--- |
| GAMPLE PLRIOD: | 1 8IC. |
| RANGE: | IV. |

b. Connect a jumper from JI, pin A, to each of the following other J1 pine in turn, recording didial readout at each tem. Then, deconnect jumper from HI and LO terminals.

| $\frac{\text { Jumper J1 Pln } 2 \text { to } \operatorname{Pin}(0)}{6}$ | Arprodminte Didtal Readout | Programmed Range |
| :---: | :---: | :---: |
| H | O000.dOMV | 1. V |
| J | 00.0000 V | 10. $V$ |
| K | 000.000 V | 100. V |
| $L$ | 0000.00V | 1000. V |
| a and 8-W/Aso | 00.00003V | O.1V and +10 Gain |
| O and C ) | 000.0000 | $0.1 V$ and $\Omega$ |
| H and C | 0.00000kn | 1. $V$ and $\Omega$ |
| $J$ and $C$ W/AO | 00.0000 x R | 10. $V$ and $\Omega$ |
| $K$ and $C$ | 000.000En | 100. V and $\Omega$ |
| $L$ and $C \mid$ | 0000.00 Kn (1M $\Omega)$ <br> 00.0000 MR (10MR) | 1000. V and $\Omega$ |

Table 4-3. In-Cabinet Performance Ohecks Std \& Opt. 29 Instrumenks (Bheot 15 of 15)
29. EXTERNAL PROCRÄMMING - EAMPLE PERIOD ETART/BTOP

8tart/8iop Enabing: By contact clooure to ground or clamp that holde input pin at - Iv de or mare poative.

Sample Period start: By contact cloeure to ground or -1 to +5 v de level.
Sample Period 8top: By opening coatact clomure or -5 to -30 v de level.
a. With the HP-2401C on and operating, set controle ats followe:
gTORE/DISPLAY (rear phincl): DIBPLAY.
100 ECC EID (rear panel): FUNCTION:
SAMPLENG RATE:
DNT.

8AMPLE PMRIOD:
VOLT.
8AMPLE PHRLOD:
RANGE:
Clockwise irom STOP.
EXXT $8 E L$.
INT+1V.
b. Connect jumpers irion J1, pin Z, to pine a and b $\alpha$ J1; record (etart) on the teat card if counting etarts.
c. Dieconnect the Jumper from pin b af $J 1$ and record (intop) on the teat card if counting etope. Then dieconnect Jumper from pin a.
24. EXTERNAL PROCRAMMMNG - RESET

Counter Recet Line: Eixternal contact ciomure to ground or clamp that holds input pin between 0 and -Iv dc.
Counter Recet Input: Negative $15 \mathrm{v}, 25 \mu \mathrm{f}$ pulee with rise time $<2 \mu$ to J 4 on rear panel.
a. With KP-2401C on and operating, set BAMPLE PNRIOD to .01 EEC and BAMPLING RATE to 8TOP; leave other controls act an epecified in etep a of check 28.
b. Connect a jumper from pin $Z$ to pin $c$ of $J 1$ and observe HP-2401C digdtal.dieplay. Record yes on test card if counting is triggered for one sample period.
c. Disconnect jumper. Record no on tent card if counting is not triggered.
d. Connect \&quare Wave Generator $600 \Omega$ output to COUNTER RESET receptacle on rear of HP-2401C through a pulee shaplng network at shown below.

e. While monitoring output of pulse chaping network with an Oecilloscope, set Square Wave Generator for 15 V p-p at 20 kHz output frequency, then for 1 Hz output irequency.
f. Record a yei on the tent card if counting is triggered about once a eecond.


HP-2401C
$\qquad$
$\qquad$
. VOLTAGE MEASUREMENT RANGES
.1, 1, $10,100,1000 \mathrm{~V}$ reading correct?
$.3,3,30,300 \mathrm{~V}$ readings carrect?

(yes)
Reading of overload voltage
2. VOLTAGE MEASUREMENT INTEGRATION

Polarity reversal reverses count?
Polarity symbol changes at zero?
Forward counting resumes at zero?
3. INTERNAL TME BASE

Frequency Ofiset From 100 kHz :
At start $d$ test
1 week later
Aging rate difference
(At $25 \pm 5^{\circ} \mathrm{C}$ ambient temperature.)


CHECK RESULTS


(yes)

parts $\ln 10^{6}$

NOTE
Because considerable time and a precisely-controlled temperature chamber are required, it is anticipated that few users of the HP2401C will check the effects of temperature upon the time base, the internal calibration standard, and voltape measurements. For ths reason, no spaces are prowided for entering lemperature test results in any of the cherks. However, pricectures are presented in Table 4.3 of the handbor* for those users who desire to check the effect of temperature upon the performance of the instrument.
$\qquad$ - $\qquad$ DATE $\qquad$
5. VOLTAGE MEASUREMENT FULL SCALE ACCURACY

Input Measured, Volts: $-1$
$+1$
0.099108

10

100

1000

## Voltage:

At etart $\alpha$ teat
1 month later
2 monthe later
3 months later
4 months later
5 months later
6 monthe later

CHECK RESULTS
4. INTERNAL CALBRATION BOURCE

( $1000 \pm 0.10 \mathrm{mv}$ )
At $25^{\circ} \mathrm{C}$ ambient; quoted toleranye includes potential inaccuracy ( $\mathbf{~} \mathbf{0 . 0} \mathrm{i}^{\mathrm{b}}$ )
a external atandard.
$(-1000 \pm 0.17 \mathrm{mv})$

( $+1000 \pm 0.17 \mathrm{mv})$

(+099. $108 \pm 0.18 \mathrm{mv}$ )
$\square$ volTs
$(+10 \pm 0.0018 \mathrm{v})$
$(+100 \pm 0.018 \mathrm{v})$
VOLTS
$(+1000 \pm 0.18 \mathrm{v})$
At $25^{\circ} \mathrm{C}$ ambient; the quoted tolerance includes potential insccuracy ( $~\left(0.001^{r}\right.$ t, for $1 v, \pm 0.002 \%$ for other voltages) $\alpha$ external standard.

2 of 8

HP-2401C PERFORMANCE CHECK TEST CARD
SER $\qquad$ --_ oate $\qquad$

$\qquad$ - $\qquad$ date $\qquad$

hP. 2401 C PERFQRMANCE CHECK TEST CARD
sen. $\qquad$ -

DATE $\qquad$
DESCRIPTION
11. RESPONSE TMAE AND MEASUR EMENT SPEED
Reading al eteady 20V input
Difference betwen previous reading and reading
irom atop input (ame voltage)
Reaponee time to

## CHECK RESULTS


13. TDE BASE EXTERNAL NPUT (Rear Panel)

Minimum amplitude required to trigger time base
14. RECORDNG OUTPUTS BCD DATA

| Decade: | Outpute Correct At J2 Pins: |  |  |  |  |  |
| :---: | :--- | ---: | :--- | :--- | :--- | :---: |
| $10^{\circ}$ | (A11) | 3 | 4 | 28 | $29 ?$ |  |
| $10^{\prime}$ | (A12) | 5 | 6 | 30 | $31 ?$ |  |
| $10^{2}$ | (A13) | 7 | 8 | 32 | $33 ?$ |  |
| $10^{3}$ | (A14) | 9 | 10 | 34 | $35 ?$ |  |
| $10^{4}$ | (A15) | 11 | 12 | 36 | $37 ?$ |  |
| $10^{5}$ | (A48) | 13 | 14 | 38 | $39 ?$ |  |


(yea)

HP. 2401 C PERFORMANCE CHECK TEST CARD
SER $\qquad$
$\qquad$ DATE $\qquad$


ChECK RESULTS
5. RECORDING OUTPUTS -

BCD FUNCTION

(yes)
16. RECORDING OUTPUTS bCD DECIMAL POINT

|  | Outputs Correct at J2 Pins |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :---: | :---: |
| Display: | $\cdot \frac{27}{2}$ | $\frac{26}{2}$ | $\frac{2}{1}$ | $\frac{1}{1}$ |  |  |  |
| $000000 . \mathrm{V}$ | 0 | 0 | 0 | 0 | $?$ |  |  |
| 00000.0 V | 0 | 0 | 0 | 1 | $?$ |  |  |
| 0000.00 V | 0 | 0 | 1 | 0 | $?$ |  |  |
| 000.000 V | 0 | 0 | 1 | 1 | $?$ |  |  |
| 00.0000 V | 0 | 1 | 1 | 0 | $?$ |  |  |
| 0000.00 MV | 0 | 1 | 1 | 1 | $?$ |  |  |
| 000.000 MV | 1 | 1 | 0 | 0 | $?$ |  |  |
| 00.0000 MV | 1 | 1 | 0 | 1 | $?$ |  |  |

Note: "0" = -35 to $\mathbf{- 2 4 . 5 v} \mathbf{d c} ; " 1 "=-2.5$ to $0 v d c$.
17. RECORDNG OUTPUTS REFERENCE LEVELS
" 1 " atate reference at $\mathrm{J} 2, \operatorname{pin} 25$
" 0 " state reference at J2, pin 24

$v$

6 of 8
$\qquad$
$\qquad$ oate

19. EXTERNAL PROGRAMMING HOLDOFF

## Hold-ol! voltage

20. EXT ERNAL ProGRAMMING -
FUNCTION

| J1 Pin $Z$ Connected To P1n | Programmed Function |
| :---: | :---: |
| None | VDC |
| E* | FREQ |
| C | онмs |
| D | Vac |
| E | vac |

21. EXTERNAL PROGRAMMING SAMPLE PERIOD


(between - atlv dc)

UNITS READOUT


(yea)

7 of 8
$\Lambda$




Figure 4-2. Troubleshooting

### 4.3 AIR filter

Inspect the air filter (center of rear panel) regularly and clean it before it becomes dirty enough to restrict air flow. Proceed as follows:
a. Remove filter-housing assembly (unlock the two quarter-turn fasteners and slide housing to rear).
b. Wash filter in warm water and detergent. * ${ }^{\text {b }}$
c. Remove cleaning polution from filter-housing assembly by shaking. Allów the assembly to dry completely before securing it to the rear panel.

## CAUTION

DO NOT APPLY ANY COATING COMPOUND TO THE FILTER. ${ }^{2}$ -

### 4.4 TROUBLESHOOTINO

When trouble is suspected it can often be isolated rapidly to a specific assembly or group of assemblies by performing a series of brief checks, such as those diagrammed in Figure 4-2. From start, and before the instrument's cover is removed, the counter is checked, with various aspects of the check reaulle dagrammed as diamond-shaped decision points. The decision point "yes" outputs form a main sequence that leads to and through the voltmeter (VM) full-scale calibration check, the range-overranging-overload check, and the integration check. "No" outputs point leftward toward checks off the main sequence or toward the component(s) that could cause an incorrect check result at the decision point.

After the initial check has isolated the trouble area, remove the instrument cover per Section 4-5 to permit completion of troubleshooting and repair. This next atage $\alpha$ troubleshooting may be greatly simplified by substituting for each auspected assembly in turn a spare assembly that is known to be operating correctly. Component assembly locations in the HP-2401C are indexed in Table 4-4 and illustrated in Figures 4-3 and 4-4. When the faulty assembly is found, trouble may then be traced to the defective component, or the faulty assembly may be shipped to your Hewlett-Packard field office for repair

If spare assemblies are not available for troubleshooting by substitution, the strouble must be located by signal tracing with oscilloscope and voltmeter. This procedure is also used to locate defective components on a faulty ascembly. The HP-2401C overall logic diagram, Figures 4-7 through 4-9 and the wiring diagram, Figure 4-34, are provided to assist the signal tracing process. Equally uceful are the detailed parts placement illustrations, circuit diagrams, and circuit descriptions for each assembly that are $\ln$ dexed in Table 4-4, with the assembly locations. For easy access to assembly circuits during operation, use the printed circuit assembly extension card provided with your instrument.

### 4.5 INSTRUMENT COVER REMOVAL AND ACCESS TO ASSIMBLIES

To remove the top wraparound cover, unscrew the six screws from the lower right and lower left sides of the instrument. The top cover may then be lifted from the instrument.

## WARNING

DISCONNECT ANY HIGH POTENTIAL (MORE THAN 50 VOLTS) FROM THE HIGH, LO, AND GUARD TERMINALS TO ELDMINATE SHOCK haZARD AT THE VFC CHASSIS AND SHELD PLATES.

Remove the upper shield plate from the vic by pulling up on the white plastic fasteners. All components thown in Figure 4-3(A) ahould now be visible. For access to componenta ahown in Figure 4-3(B) pull up 6n white plontic fasteners at corners of the integrating amplifier card rack.

With the instrument upaide down, unscrew the seven attaching serewa and remove the bottom cover. The lower vic chield plate is removed in the same manner as the upper shield. For access to the preciaion readetors in A28, remove both attaching screws and the cover. These operations expose the components shown in Figure4-4(A). For access to the components shown in Figure 4-i(B), release the swing chassis fasteners and open the swing chasels.

When replacing plug-in printed circuit ansemblies and other components, make certain they are installed in the correct place. Reverse the procedure used to gain access to assemblies when troubleshooing, repair, and calibration of the HP-2401C are completed.

### 4.6 REPAIR

### 4.6.1 Assemblies That Should Net Be Repaired in The Field

Satisfactory repair of certain assemblies is difficult to achieve without apecial training and/or apecial equipment. Consequently, it is recommended that these assemblies be returned to your Hewlett-Packard field office for repair. The assemblies which should receive this treatment are as follows:
a. Integrating Operational Amplifier As1.
b. Trigger Level Detector A32 or A33 -- if R1, R2, R5, R6 or T1 must be replaced.
c. Reveraible Decade Counter A11-A15, or A46 -- if photoconductor plate V1 must be replaced.

### 4.6.2 Replacoment of Components on Primed Circuit Assemblies

Component lead holes in the printed circuit boards have plated walla to assure good electrical contact on the opposite sides of the bourd. Apply heat sparingly and work carefully to avoid damage to this plating.

The following replacement procedure is recommended:
a. Remove defective component.
b. Melt solder in component lead holes, using clean dry soldering iron to remove excess solder. Clean holes with a toothpick or woooden splinter. Do not use a metal tool for cleaning because it may damage the throughhole plating.
c. Shape leands of new component to match those of component being replaced and insert leads into the lead holes. Make certain diodes and .capacitors are oriented correctly, then solder the component in place. using heat and solder sparingly.
d. Repair any breaks in through-hole plating (indicated by separation of the round conductor pad on either side of the board) by pressing the conductor pads against the board and soldering component lead to pads on both sides of the board.

## CAUTION

Use only rosin-core solder or rosin fluxx for soldering components of the HP-2401C. Use of other fluxes for soldering can cause erratic and unsatisfactory performance.

### 4.6.3 Post-Ropair Cloenup

Fallure to clean a printed circuit board or other assembly after repair can be a prime cause of substandard performance. Performance of attenuator A28. integrating amplifier A31, and trigger level detectors A32 and A33 is particularly susceptible to lowering of leakage resistance and electrolytic effects caused by soldering flux, spattered solder, bits of wire. finger marks. etc. It is partly because of this susceptibility that factory repair of A31. A32. and A33 is strongly recommended.

When cleaning, it is most important to keep in mind that solvents can damage certain parts if not used carefully. The photoconductors in that photochopper assembly on A31, the photodecoder on the counting/display decades, and other plastic encased parts are definitely subject to damage from solvents. For this feason, any cleaning solvent should be selected carefully and applied sparingly. Particularly to be avoided is the total immersion of any assembly in a solvent bath of any sort. The best way to clean a repaired assembly is with Isopropyl Alcohol or with a rosin solvent, such as Dupont TE-35 Freon (HP stock number 8500-0275). The solvent should be applied with a cottontipped swab, such as a Q-tip, that is used to scrub-clean the repaiged area. All solvent should then be wiped off with a dry swab.

### 4.7 CALIBRATION

For normal day-to-day operation of the HP-2401C only the zero and full-scale calibration adjustments specified in Sections 2.2.2 and 2.2.3 are required. The calibration adjustments given in this section should be accomplished at the intervals specified in Table 4-2, or to correct power supply-output voftages or substandard performance.

## 4

Section $\frac{1 V}{V}$

The instrument should be calibrated only if correct tent equipinent, operating within its calibration period, is used. The instrument should be given a 1-1/2 hour warmup at operating temperature before any adjustment is made.

### 4.7.1 Adjusfment of -12.3V Power Supply Output

With the DC Standard Differential Voltmeter measure the potential acroas filter capacitor C32. If the potential is not within $\pm 0.002$ volte of 12.3 voltspadjust A35R9 for exactly 12.3 volte across C32. (Soe Figure 4-3(B) for locationi.) Tap circuit board Ass to verify atability of the sefting; if necesagy, reset AS5R9 for 12.3 volt butput.

### 4.7.2 Adjustment of -35V Power Supply Oufput -

With the DC Standard Differential Voltmeter meacure the potential acrome filter capacitor C10. If the potential is not within $\pm 0.15$ volts 0 olta, adfuet A7R10 for exactly 35 volte acrose C10. (See Figures 4-3(A) and 4-4(B) for locations.)

### 4.7.3 Calibretion of Overlead Defection

Calibrate Overload Detection whenever the OVERLOAD indicator is lighted by an overrange input that is less than $305 \%$ of full acale or greater than $320 \%$ of full scale. (See performance check 1, Table 4-3.) Proceed an
follow: follow:
a. On any range but the 0.1 I range, apply a negative dc input voltage that is $312.5 \%$ of full scale on the next lower range. (For example, apply $-31.25 \% \mathrm{vdc}$ to the $\mathrm{HP} \mathbf{-}-24010$ set for 100 v range.)
b. Select next lower range and check for OVERLOAD indication.
c. If OVERLOAD indicator does not light, slowly adjust A10R2 counterclockwise to make it light. (See Figure 4-3 for location of adjustments.)
d. If OVERLOAD indicator lights in step b, set A10R2 clockwise untll it no longer lighte, then perform step $c$.
e. Repeat steps a-d with positive input voltage, but set A16R86 for correct reaponse instead of A10R2.

### 4.7.4 Celibration of Imernal IV Reforence Sfandard

Whenever the internal reference reading obtained from performance check 4 of Table $4-3$ is not within $\pm 0.10$ millivalts of 1000.00 MILLIVOLTS, set A35R21 to obtain a reading of $1000 \pm 0.02$ MILLVVOLTS. Tap circuit board A35 to verify mechanical stability of the setting; if necessary, reset A35-

R21 for correct output from the internal reference standard. (See Figure 4-3B for location of AS5R21.)

### 4.7.5 Calibretion of Internal time Ease

Whenever the horizontal drift of the internal reference equare wave, determined in performance chéck 3 of Table 4-3, exceeds 2 centimeters in 1 second, set capacitor C4 for minimum drift. Improve brightneas of oscllloscope digplay by aynchronizing from 100 kHz output of Frequency Standard. (Spe-figure 4-3(A) for location of C4.)

### 4.7.6 Coarse Full-Scele Cellbretion Adjustments (Mgure 4-a A)

Perform these adjustmenta only after replacement of printed circuit assembly As1, As2, or Ass or parts on any of theee ansemblies. Gain access to adjustments per Section 4.5 (leaving 128 shield in place) and proceed as followa:
a. Zero the inctrument per Section 2.2.2.
b. Set the RANGE awitch to INT +1 IV and mechanically center the front panel CAL+ adjuatment.
c. Set A33R4, the +FULL SCALE CAL ADJuntment, for reading of $+1000.00 \pm 0 \cdot 20$ MILLIVOLTS. Tap plug-in aesembly Ass to check mechanical atability of the eetting; if neceasary, remet AS3R4 for correct reading.
d. Repeat ateps $b$ and $c$ with the RANGE awitch at INT-1V and the CALadjustment centered. Set A32R4 for reading of $-1000.00 \pm 0.20 \mathrm{MILL}-$ VOLTS.
e. Complete normal full-acale calibration of the HP-2401C per Section 2.2.3.

### 4.7.7 + And - Trigger Leval Adjustments

Perform elther or both of these adjustments after replacement of printed circuit assembly AS2 or As3 or parts on either of these assemblies. With top and botom of the inatrument both acceasble as shown in Figures 4-3(A) and 4-4(A), proceed as follows:
a. Set the RANGE ewitch to INT+IV.
b. With oscilloscope, monitor waveform at A31(15); ground oscilloscope probe at A31(P29). See Figure 4-3(A) for locations of A31(15) and (P29).
c. Set A33R27 for a maximum negative pcak amplitude of -0.1 v .

See Figure 4-4(A) for locations of A33R27 and A32R27.
d. Bot the RANOE awitali to INT-IV.
-. Bot As2Rat for maximum posilive poak of *0. iv.

### 4.7.4 Input Amonuater Callbrallon

Calibration of the linput attenuator roquiren the ofuipment and aetupaned
 apocified In Beotion 4. B, but do not remova the Aso oover elifeld. Procood an follom (aoo Figuron 1-I(A) and (B), and 4-4(A):
a. Zoro the HP-p401C ualing the proooduro in Bection 2.2.2.
b. Connoot Uio DC•Btandard, DC Null Voltniotor, 1 Volt Calßbration Btandard, Precialon Volt Box, and IiP-2401C an ahown. In Figuron 4-i(A) *and (B) for O.IV chock.

## NOTIC

Oporato tho DC Null Voltmotor from itm Intornal battorion; do not comect it to the ac line.
c. Sot tho DC Etandard output voltago to produco a null on tha mont easaltivo range of UisoriSC Null Voltmotor.
d. On the HP-2401C, mot tho RANGE ewitoh to. iV and tho CALt adjuatmont for to0. 100 MILLIVOLTESreading.

## NOTE

The 100K input Impodance of the HP-2401C on tho. IV RANOE loade tho output of the Prociaton Volt Box mo that the ingut voltage is +00.108 millivolta.
o. Change IfP-2401C connection to that ahown in Piguro 4-1(A) for iv chock.
f. Sot HP-2401C RANGE awitch to $1 V$ and not tho iV callbration Filjuatment (markod on 120 covor) for 11000.00 MILLIVOLTS reading.
K. Change connoctions to those shown in Figure 4-1(B) for 10 V chack and aot IDC Btandard to produce a null on the mom mensitivo rango of tho DC Null Voltmotor.
h. Sot IRANGE nwitch to 10 V nad set tho 10 V callbration adjustmofit for , +10.0000 VOLT'S readling.

1. Change connections to those ahown in Figure 1-1(13) for 100 V check and set DC Btandard to permuce a mull on the most benaltive range of the DC Null Voltmoter.
J. Bot RANOE awitch to 100 V and set the 100 V calibration adjustment for +100.000 VOLTE reading.
k. Change connegtions to those ahown in Figute 1-1(B) for 1000 V check and mot DC Btand d to produce a null on the most aenalive ranse of the DC Null Voltmotor.
2. Bot RANOE awitoli to 1000 y and set the 1000 V calibration adfustment fof $+1000,00$ VOLTS reading.

## 

The nogative and poattive overrunge lineurlty adjuatments of the HP-2401C ure AS2RS2 and AS3R32. These adjuatmente are sol at the factory to provide overrange accuracy bottor than that apecified for tho inatrument and should not be
, resot unloas improfed overranging linearity is ubsolutely necessary. An udjustable de atandard capable of supplying a suftable range of positive or negative voltagen that are known accurately to $\pm 0.002 \%$ or beller is required. If much a atandard ia avallable, overranging linearlty can be optimized by the following genoral proceduro:
u. After 1-1/2 hour warmup, gero the HP-2401C per Suction 2. 2. 2. Perforin the full-acale adjustments in Section 2. 2.3, but use the IV RANGE and, and - -1.00000 volt Inpute (rom the dc. atand $r$ rd.
b. Boforefuuching As2Rs2 or Assirg2, mukd a complete plot from full acale tothroe timos full scale, ut 0.1 full scalo or ahorter intervals, of tho h His or low deviation of HP-2401C readings from the known voltages suppiliod by the de standard. Plot botli positive and negutive inputs.
c. If tho linearlty charactoriatic plotted in stop it is unaccepxable, adjust A32R32 or A33R32 to correct It. When capactior C0 (Figure 4-20) is noxt to R32, clockwiso adjugtmont of R32 compensates for low roadings. If un inductoris in the CO position, clockwise adjustment of R32 compensutos for high roadings.

- d. Repoat stops b and ${ }^{\circ}$, untll acceptable linearlty is achlevod. Then roset coarse full acato calibration adjuatmontes an spocifiod in section 1. 7. 6.


### 4.7.10 Phetechiopper Drive Osclliator Ad/ustmem

The DIRIVE OSC ADI realator Betes the frequency of the photochoppur drive obsellator. On InBtrumenta wilh Aprial Profix b0t-. This adjust mont is localed on the babe of the awing chasala card rack ab bhown th the inade on Figure 4-3 (B). On Inatrumenta wilh Bortal Profix 521- and aloove. Hila adjuatmoint Ia located on abBembly A31 (Bee Figure 1-30). The frequency ahould be 240 + $511 \%$ when llne voltage to tho Hp-2AdiC la at 102 or 204 vate. The frequency may be counted through a high impedance prober at rllher terminat of A31C27 when the drlve osellator cover lis removed as shown in Figure 4-30.


- Bupplied with the lip-2410B.
- Bupplited with the hip-2411A (a jumper bourd is linatalled in the A30 position if the HP-240ice is or dered by ltself).

Table 4-4. Component Location and Theory Index (Sheet 2 of 2)

| $\begin{aligned} & \text { Reforence } \\ & \text { Desigmation(s) } \end{aligned}$ | Component Name or Purpose | REFESENCES |  |
| :---: | :---: | :---: | :---: |
|  |  | Location(0) Figure | Detall: Figure(a) |
| Capacitora |  |  |  |
| C1 | +160V filter | 4-4 | 4-12 |
| C1 | Fultering at input to -36V coriea regulators | 4-3 | 4-12 |
| Cs | Countar triesor differentiating | 4-1 | 4-18, 10, 20 |
| C4 | 100 kth oecilistor trimmer | 4-3, 4 | 4-11 |
| C5 | 100 kHz ocelliator pedior | 4-1 | 4-11 |
| C7 | -38V requlator output filtor | 4-4 | 4-15, 16, 20 |
| C32, C 34 | + -12.2V requlator output flltor | 4-3 | 4-32 |
| A28C101, A28C 102 | Attemuator relay ewitching delay | 4-4 | 4-13 |
| C202 | Coupling for recet-tricsered mencur ement diaplay cycle | 1-4 | 4-10 |
| Diodes |  |  |  |
| CRS, CRS | -36V power aupply rectifior | 4-3 | 4-12 |
| A89CR101, | Attenuator relay murge euppresaion | 4-4 | 4-13 |
| A89CR $103-A 89 C R 105$Relaya |  |  |  |
| A88K1-A28K5 | Attenuator control | 4-4 | 4-13420 |
| Inductore | 90V 1 |  |  |
|  | -36V eupply filter | 4-3 | 4-12 |
| Pluge <br> P1/FL1 |  |  |  |
|  | AC line input receptacle a notse filter | 4-5 | 4-12 |
| Tranalatora |  |  |  |
|  | -36V aupply serten regulator | 4.3 | 1-12 |
| Realetore |  |  |  |
| R1 | Current limitung | 4-4 | 4-12 |
| R2 | -36V reculier filter output lond | 4.1 | 4-12 |
| RS | Series regulator 93 emitter load | 4-4 | 1-12 |
| R4 | 10 kliz check attemuator | 4-4 | 4.27 \& 28 |
| R6 | Capacitor C1 diecharge | 4-4 | 4.12 |
| R0, R7 | - C -record command aource | 1-4 | 4-10 |
| Re, Re | Counter trigger differentuating | 4-4 | 4.15, 10. 20 |
| R48 | Allemutor realator, . IV range | 4-3 | 4-20 |
| R49 | Part of calt/zero divider network | 4-4 | 4-20 |
| Rso | Part of cal + /zero divider notwork | 4-3 | 1-20 |
| R01, R02 | + a -channel output tranalormor (FS, T4) load | 1-3 | 4.29 |
| A2BR101, A2bR102 Allonuator rolay dolay <br> A2BR108-A20R107 |  |  |  |
|  |  |  |  |  |
| Bwitchon |  |  |  |
| 81 | ranoe | 4-3 | 4.12820 |
| 82 | FUNCTION | 4-4 | 4-1920 201 |
| 85 | 8AMPLE PEPIOD | 4.4 | 4-10, $20 \& 22$ |
| 88 | bampling rate | 4.4 | 4.10 |
| Tranatormora |  |  |  |
| T1 | Power for -98, +6, 1150 V power supplien | 4.3 | 4.12 |
| T2 | Power for $\pm 12.3 \mathrm{~V}$ power dupply \& IV Calliration Standar | d 4-4 | 4-32 |
| T4, T5 | + a -channel outjut yoty | 4-3 | 4-29 |
| Cryatals |  |  |  |
| Y1 | 100kliz for time bane oncillator Af | 4.3 | 4-11 |

### 4.7.11 Adjustmenf Per Pulee Mocsuramen (Figures 4-27 or 4-20)

Optimum adjustment for pulse measurement will differ from the factory-set optimum sine wave adjustment. Use this adjustment only for pulse measurements. Input Trigger A27 may be adjusted for either positive or negative pulse measurements at frequencies between 5 Hz and $300 \mathrm{kHz}(1.2 \mathrm{MHz}$ with Option 28).
a. Connect output of Pulse Generator to HP 2401C FREQ DNPUT connector.
b. Set Pulse Generator for positive or negative 1 volt, $2 \mu$ sec pulse, with 300 kHz repetition rate.
c. Adjust A27R2(A27R3 If applicable) for a steady 300 kHz display.
4.7.12 Readjustment Por Sine Wave Measurement (Figures 4-27 or 4-28)

If the instrument was adjusted for pulse measurements, it must be readjusted for sine wave measurement. This adjustment is to factory tolerances and must be made to assufe that the instrument will operate within stated spectfications. Proceed as follows:
a. Set Portable Osctllator for 300 kliz and adjust output to zero. Connect the Portable Oscillator output connection to the HP 2401C FREQ INPUT connector and to ac vtem.
b. Adjust Portable Oscillator for 50 millivoll output.
c. Adjust A27R2(A27R33 If applicable) for a steady 300 kHz display.
d. Slowly reduce the Portable Oscillator output. The display should disappepr completely before the output reaches 40 millivolts.
r. It the requirements of tep dare not met. Increase the Portable Oscillator outpul ( 100 millivolts maximum) and repeat steps a and d until the requirements of 40 -millivoll dropout are met.


View A
(See parts list beginning on page 5-42.)



- AIDNF ON SCRIAI PREIIM SOI THAU 605
ma AJTHS POH BGARO STOCK NO 3060 SOl6
View B
(See parts list beginning on page 5-42.)

Fipure 4-3. Top Internal View


(A28) Attenuator Assembly
(See parts list beginning on page 5-46.



[^0]


Figure 4-8. Overall Logic Diagram Counter Control and HP 2410B Coupling





Stock NO. 5212A-65F
(AB) 100 KHz Oscillator and Schmitt Trigger
(See parts list beginning on page 0-5.)


NOTES
2. unless otherwise indicateo:

RESISTANEE TN OHMS AND


05060-2400


Hege scrimatic diagnam fon m, ne, amo wi uanee.
Stock No. 5060-2006 (Serial Préfix 614 and above)
Stock No. 5060-3830 (Serial Prefix 501 thru 610)
(A7) -35V Regulator and Reset (See parts list beginning of page 5-6.)


Stock No. 5060-3805
(A29) +6V Bias
(See parts list beginning on page 5-32.)


A


Stock No. 5060-5870 (Serial Prefix 610 and above)
(A8) Attenuator Coupling Logic Assembly
(See parts list beginning on page 5-7.)

(A47) IV Relay Timing Assembly (See parts list beginning on page 5-42.)




Figure 4-14. HP 2410 B Units Coupling (A9)


Stock No. 5060-5655 (Serial Prefix 610 and above)
(A10) Overload Detector
(See parts list beginning on page 5-11.)



Stock No. 5060-2181 (Serial Prefix 501 thru 605)
(A10) Overload Detector (See parts list beginning on page 5-10.)




- crase is under oie and crésg is under oig.

Stock No. 5060-3809
(A16) Counter Control
(See parts list beginning on page 5-15.)



Stock No. 5060-5002 (Serial Prefix 501 thru 622) Stock No. 5060-6224 (Serial Prefix 637 and above)
(A17) Gate and Display Control (See parts list beginning on page 5-17.)


Stock No. 5060-2058
(A18) Gate and Display Control
(See parts list beginning on page 5-19.)

*



Btock No. 0060-3820 (Borial Profix 001 thru 000)
Slock No. 5000-8072 (Borial Prefix 010 and above)
(AID) Units/Countor Input Logic
(Beo parts list beginning on page 6-20.)



Stock No. 5060-2000
(A20) Decimal Point Logle
(See parts list beginning on page 5-22.)



* CRIz not used on serial prefix bol and s2l.

Stock No. 5060-2010 (Serial Prefix 501 thru 605)


Stock No. 5060-5873 (Serial Prefix 810 and above)
(A21) Blanking Logic/Time Base Selection (See parts list beginning on page 5-23.)



Stock No. 5060-5610 (Serial Prefix 537 and above)
(A22) Printer Coupling
(See parts list beginning on page 5-26.)


Figure 4-23. Printer Coupling (A22) For Serial Prefix 537 and above


Stock No. 5060-2111 (Serial Prefix 501 thru 533)
(A22) Printer Coupling
(See parts list beginning on page 5-24.)
,



Stock No. 5060-3771 (Serial Prefix 501 thru 605.) Stock No. 5060-5874 (Serial Prefix 610 thru 622) Stock No. 5060-6206 (Serial Prefix 637 and above)
(A23) HP 2410B AC and Ohms Delay Gate (See parts list beginning on page 5-28.).


DISASSEMBLED VIEW

Stock No. 5060-3818
(A24) Units Indicator
(See parts list beginning on page 5-20.)


NOTE:
A25 not illustrated.


Stock No. 05232-6007 (Serial Prefix 735 and above)
(A26) Input Amplifier (See parts list beginning on page 5-30.)


Stock No. 05232-6006 (Serial Prefix 735 and above) (A27) Trigger
(See parts list beginning on page 5-31.)


NOTE:
A25 not illustrated.


Stock No. 05214-6014 (Serial Prefix 501 thru 637)
(A26) Input Amplifier
(See parts list beginning on page 5-30.)


Stock No. 5060-5016 (Serial Prefix 501 thru 637)
(A27) Trigger
(See papts list beginning on page 5-31.) )


0080 -183




Stock No. 5060-3848 (Serial Prefix 501)


Stock No. 5060-5145 (Serial Prefix 521 and above)
(A31) Integrating Operational Amplifier (See parts list beginning on page 5-34.)



Stock No. 5060-2108 (Serial Prefix 501 thru 605) Stock No. 5060-5875 (Serial Prefix 610 thru 622) Stock No. 5060-6203 (Serial Prefix 637 and above)
(A30) HP 2411A Decimal Point Logic (See parts list beginning on page 5-32.)




cseso-1928

Figure 4-33. Photoconductor and Decimal Lamp


Figure 4-34. Interconnections (Sheet 1 of 3)



Figure 4-34. Interconnections (Sheet 2 of 3)




## SETION V <br> CONTENTS

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## LIST OF BOARD ASSEMBLIES

NOTE: Refer to introduction of this section for an explanation of letter codes in note column.


## LIST. OF BOARD ASSEMELIES (Cont'd)

- NOTE: Refer to introduction of this section for an explanation of letter codes in note column.

| Reference Designation(s) | Description | Stock Number | Note | Page <br> No. |
| :---: | :---: | :---: | :---: | :---: |
| A22 | Logic Card | 5060-2111 | A-E | 5-24 |
|  |  | 5060-5610 | F-X | 5-26 |
| A23 | AC and Ohms Delay Gate | 5060-3771 | A- ${ }^{+}$ | 5-28 |
|  |  | 5060-5874 | J-L $\dagger$ | 5-28 |
|  |  | 5060-6206 | M-X | 5-28 |
| A24 | Units Display | 5060-3818 |  | 5-29 |
| A25 | Attenuator Control | 5060-2018 |  | 5-29 |
| A26 | Input Ampliffer | 05212-6014 | A-S | 5-30 |
|  |  | 05232-6007 | T-X | 5-30 |
| A27 | Schmitt Trigger | 5060-5016 | A-S | 5-31 |
|  |  | 05232-6006. | . T -X | 5-31 |
| A28 | Programmable DC Attenuator | 5060-5115 |  | 5-46 |
| A29 | ${ }^{+6 \mathrm{~V}}$ Bias Supply | 5060-3805 |  | 5-32 |
| A30 | HP 2411A Decimal Point Logic | 5060-2108 | A-H** | 5-32 |
|  |  | 5060-5875 | J-L** | 5-32 |
|  |  | 5060-6203 | M-X | 5-32 |
| A31\# | Operational Amplifier | 5060-3848 | A | 5-34 |
|  |  | 5060-5145 | B-X | 5-34 |
| A32\# | Negative Channel PC | 5060-5001 |  | 5-37 |
| A32A1 | Amplifier PC | 5060-6275 |  | 5-37 |
| A32A2 | Binary PC | 5060-3838 |  | 5-38 |
| A33\# | Positive Channel PC | 5060-3849 |  | 5-38 |
| A33A1 | Amplifier PC | 5060-6274 |  | 5-38 |
| A33A2 | Binary PC | 5060-3838 |  | 5-39 |
| A34 | Series Regulator | 5060-3782 |  | 5-40 |
| A35\# | Power Supply Amplifier | 5060-3783 |  | 5-40 |
| A36 | Rectifier Filter PC | 5060-3806 | - \% | 5-42 |
| A46 | Reversible Decade Counter | 5060-3781 | - | 5-42 |
| A47 | Relay Time Circuit | 5060-3691 |  | 5-42 |

## SECTION V PARTS LIST

### 5.1 INTRODUCTION

This section contains two lists of information for ordering replacement parts. Table 5-1 lists parts alpha-numerically by reference designation. It provides HP part numbers, a general description of the parts and any applicable notes. The Note column also contains letter codes which identify parts variations between instruments having different serial prefix numbers. Where the Note column has been left blank, the parts apply to all instruments. Following are the codes for the instruments covered by this manual.

| Code | Ser Prefix/Ser No. | Code | Ser Prefix/Ser No. |
| :---: | :---: | :---: | :---: |
| A | 501 - | M | 637-01271 |
| B | 521 - | N | 637-01388 |
| C | 526- | $\mathbf{P}$ | 637 ¢01488 |
| D | 529- | Q | 637-01588 |
| E | 533- | R | 637-01738 |
| F | 537-00371 | S | 637-01938 |
| G | 537-00621 | T | $735-$ |
| H | 605- | U | 739 - |
| J | 610- | V | 749- |
| K | 614 - | W | 751 - |
| L | 622 - | X | 811 - |

Table 5-2 lists parts alpha-numerically by their HP part numbers and provides the following information on each part:
a. General description of the part.
b. Typical manufacturer of the part expressed as a five-digit code. (A list of manufacturers and their code numbers appear in Table 5-3.)
c. Manufacturer's part, stock, or drawing number.
d. Total quantities used.

### 5.2 ORDERING INFORMATION

To order a part from Hewlett-Packard Co., address your order or inquiry to your local Hewlett-Packard Sales and Service Office. See the listing at the rear of this manual

Specify the following information on each part
a. Model number and complete serial number of instrument.
b. Stock number.
c. Circuit reference designation.
d. Description.

To order a part not listed in Table 5-1, give complete description and nclude function and location of the part in the instrument and/or system.

### 5.3 ABBREVIATIONS USED



### 5.4 RICOMMENDED INDUSTRIAL SPARES

In situations where down-time of the equipment is of critical importance, it is recommended that one of each of the following plug-in etched circuit boards or assemblies be stocked. The instrument can then be kept in operation while the faulty board or assembly is being repaired. Where more than o stock number is listed, check the instrument serial number prefix and Paragraph 5.1 to determine the applicable stock number

| Circuit <br> Reference | 3 |  | Usable <br> On Code |
| :---: | :---: | :---: | :---: |
|  | Description | HP Stock No. |  |
| A1-A5 | Decade Divider | 5212A-65C |  |
| A6 | 100 kHz Oscillator | 5212A-65F |  |
| - A7 | -35V Regulator \& Reset | 5060-3830 | A-J |
| ก |  | 5060-2006 | K-X |
| A10 | Overload Detector | 5060-2181 | A-H |
|  | / | 5060-5655 | J-X |
| A11-A15, A46 | Reversible Decade | 5060-3781 |  |
| A16. | Reversible'Counter Logic | 5060-3809 |  |
| A17 | Gate Control | 5060-5002 | A-L |
| 0 |  | 5060-6224 | M-X |
| A18 | Display Control | 5060-2052 |  |
| A19 | Control Logic A | 5060-3829 | A-H |
|  |  | 5080-5872 | J-X |
| A26 | Input Amplifier | 5060-6014 | A-S |
|  |  | 5060-6007 | T-W |
| A27 | Schmitt Trigger | 5060-5016 | A-S |
|  |  | 5060-6006 | T-X |
| A31* | Operational Amplifier | 5060-3848 | A |
|  |  | 5060-5145 | B-X |
| A32* | Negative Channel | 5060-5001 |  |
| A33* | Positive Channel | 5060-3849 |  |
| A34 | Series Regulator | 5060-3782 |  |
| A35* | Power Supply Amplifier | 5060-3783 |  |

Table 5-1. Reference Designation Index

| $\begin{aligned} & \text { Referente } \\ & \text { Desimation } \\ & \hline \end{aligned}$ | (1) Part No. | Description \# | Note |
| :---: | :---: | :---: | :---: |
|  |  | A1 5212A-65C |  |
| A1 | 5212A-65C | Decade divider |  |
| AlCL | 0150-0121 | C:FXD CER O.1 UF +80-20\% 50VOCH |  |
| ${ }^{\text {AlC }}$ A | 0140-0194 | C: ExD MICA 110 PF 58 |  |
| Alc Alc AlC4 | $0140-0195$ $0140-0195$ |  |  |
| Alc5 | 0140-0196 | C:FXD MICA C:FXD MICA 150 PF |  |
| Alc6 | ¢140-0196 | C: FXD MICA 150 PF $5 \%$ |  |
| ${ }^{\text {AlC }} 1$ | 0140-0196 | l:FXD MICA 150 PF 58 |  |
| AlC AlC ald | $0140-0199$ $0140-0195$ | L: FXD MICA 240 PF 58. |  |
| Alc 10 | 01400195 $0.40-0195$ |  |  |
| AlCl1 | 0140-0194 | C:FXO MICA 110 PF 58 |  |
| AlC12 AlCl | $0140-0190$ $0140-0198$ | $\begin{array}{llllll}\text { C: FXD } & \text { MICA } & 200 & \text { PF } & 58 \\ \text { C: FXO } \\ \text { HICA }\end{array}$ |  |
| AIC 14 | 0140-0200 | C: FXD MICA 390 PF 58 |  |
| AICRI | 1910-0016 | diode: germanium louma at 0.85V gopiv |  |
| A1CR2 | 1910-0016 | diode:germanium looma at 0.85V gopiv |  |
| A1CR3 | 1910-0016 | DIODE:GERMANIUM 100MA AT 0.85V 60PIV |  |
| AlCR4 AlCR5 | $1910-0016$ $1910-0010$ | OLODE: GERMANIUM 100MA AT 0.85 SV GOPIV |  |
| A101- Al0 | 1850-0002 | thansistor:germanium alloy junction |  |
| AlR1 | 0683-3915 | R:FXD COMP 390 ОНल $581 / 4 \mathrm{~N}$ |  |
| ${ }_{\text {AlR } 2}$ | 0683-4735 | K: FXD COMP 47K ОНM 5 z 1/4W |  |
| AlR3 A1R4 | $0683-6825$ $0683-4735$ | R:FXD COMP $6800 \mathrm{OHM} 581 / 4 \mathrm{~W}$ |  |
| ${ }_{\text {AlR }}$ | $0683-4735$ $0683-1035$ |  |  |
| AlRg | 0683-3925 | K : FXD COMP $39000 \mathrm{OHM} 581 / 4 \mathrm{~W}$ |  |
| AIR7 | 0683-2015 | R:FXD COMP 200 OHM 58 $1 / 4 \mathrm{~N}$ |  |
| AlR8 | 0683-3925 | R: FXD COMP $3900 \mathrm{OHM} 581 / 4 \mathrm{~N}$ |  |
| AlR AlRIO | 0683-6825 | R:FXD COMP 68000 OHM $581 / 4 \mathrm{~W}$ |  |
| AIRII | 0683-1035 | R:FXD R: FXD COMP lik |  |
| AIR12 | 0683-4735 | R: FXO COMP 47K OHM 58 1/4W |  |
| AlR13 AlR14 | $0683-4735$ $0683-6825$ | K: FXD COMP 47K UHM $5881 / 4 \mathrm{~N}$ |  |
| AlR15 | 0683-4735 | K : FXO COMP 47K 0 HM $5811 / 4 \mathrm{~N}$ |  |
| A1R16 | 0683-8225 | R : FXD COMP 8200 OHMS $581 / 4 \mathrm{~N}$ |  |
| A1R27 | 0683-3925 | R: FXO COMP 3900 OHM 58 1/4W |  |
| AR1818 AlR19 | -0683-2015 |  |  |
| A1R20 | ${ }_{0}^{0683-6825}$ |  |  |
| A1R21 | 0683-4735 | R: FXD COMP 47K OHM 58 1/4N | 4 |
|  | C |  |  |


\# 8ee introduction to this section for ordering information

Table 5-1. Reference Designation Index (Cont'd)

\# See introduction to this section for ordering informption






5-12

Table 5-1. Reference Destgnation Index (Cont'd)


Table 5-1. Reference Designation Index (Cont'd)
Table 5-1. Reference Designation Index (Cont'd)

| $\begin{aligned} & \text { Xeforence } \\ & \text { Destmation } \end{aligned}$ | Part No. | Description \# | Note |
| :---: | :---: | :---: | :---: |
|  |  | $\begin{aligned} & \text { A115000-3781 (CONTD) } \\ & \text { A12-A15, A60 5000-3781 } \end{aligned}$ |  |
| Al1R16 AllR17- | 0683-1045 | K:FXD COMP 100k OHMS 58 1/4W |  |
| AllR26 | 0683-2235 | RifxD Comp 22K OHM 58 1/4W |  |
| Al1R27 | 0686-5625 | RifxD Cowp 5600 OHM $581 / 2 \mathrm{~W}$ |  |
| AllR 28 | 0686-5625 | R PXD COMP 5600 OHM $581 / 2 \mathrm{~W}$ |  |
| A11R29 | 0686-5625 | R: FXD COMP 5600 OHM $581 / 2 \mathrm{~W}$ |  |
| A11R30 | 0686-5625 | K2 FXD COMP $5600 \mathrm{OHM} 581 / 2 \mathrm{~W}$ |  |
| Al1R31 | 0683-6835 | R:FXD COMP 68K OHM 58 1/4W |  |
| A11R32 | 0686-5625 | R PFXD COMP 5600 OHH $58 \mathrm{~s} 1 / 2 \mathrm{~W}$ |  |
| A11R33 | 0686-5625 | R:FXD COMP 5600 OHM $581 / 2 \mathrm{~W}$ |  |
| A11R34 | 0683-6835 | Ri FXD COMP 60K OHM 58 1/4H |  |
| A11R35 | $0683-6835$ | R:FXD COMP 68K OHM 58 1/4W |  |
| A11836 | 0686-5625 | RIFXO COMP 5600 OHM 58 1/2W |  |
| A11R37 | 0686-5625 | RsFXD COMP 5600 OHM 58 1/2W |  |
| Al1R38 | 0683-6835 | R: FXD COMP 68K OHM 58 1/4M |  |
| A11R39- |  |  |  |
| Al1846 | 0683-2735 | R3FXD COMP 27K OHM $581 / 4 \mathrm{M}$ |  |
| A11R47 | 0683-3335 | R3FXD COMP 33K OHM $581 / 4 \mathrm{~W}$ |  |
| Al1a48 | 0683-2235 | RifxD Comp 22 K OHM $581 / 4 \mathrm{~W}$ |  |
| A11R49 | 0683-2235 | RifxD COMP 22K OHM 58 1/4W |  |
| AllR50 | 0683-3335 | RifxD COMP 33K OHM 58 1/4W |  |
| Allasi | 0683-3025 | R: FXD COMP 3000 DHM $581 / 4 \mathrm{M}$ |  |
| A11852 | 0683-3335 | R3FXD COMP 33K OHM 58 1/4M |  |
| A11853 | 0683-2235 | R:FXD CONF 22K OHM $581 / 4 \mathrm{~N}$ |  |
| A11R54 | 0683-2235 | R: FXD COWP 22X OHM 58 1/4W |  |
| A11R55 | 0683-3335 | R:FXD COMP 33K OHM 58 //4W |  |
| A11R56 | 0683-3025 | R: FXD COMP 3000 OHM $581 / 4 \mathrm{H}$ |  |
| ${ }^{1} 11257$ | 0683-3335 | Ri FXD COMP 33K OHM $581 / 4 \mathrm{~N}$ |  |
| AllR58 | 0683-2235 | RaFXD COMP 22K OHM $581 / 4 \mathrm{~W}$ |  |
| Allas9 | 0683-2235 | Ri FXD COMP 22K OHM 58 1/4W |  |
| A11R60 | 0683-3335 | RiFXD COMP 33K OHM 58 1/4H |  |
| ${ }^{\text {All } 11661}$ | 0683-3025 | R2FXD COMP 3000 OHM 58 1/4M |  |
| ${ }^{111262}$ | $0683-3025$ $0683-3335$ | R2FXO COMP 3000 OHM 58 1/4W |  |
| A11R64 | 0683-2235 | R: FXD COMP 22K OHM 58 1/4H |  |
| 111865 | 0683-2235 |  |  |
| AllR66 AllR67 | -0683-3335 | R1FXD COMP 33K OHM 58, $1 / 4 \mathrm{H}$ |  |
| AllR68 | 0683-6835 | RIFXO COMP 685 OHM 58 1/4M |  |
| AllR69 | 0686-4735 | R3FXD COW 47 K OHM 58 1/2W |  |
| Allvi | 1970-0009 | electron tubesindicator 10 digit |  |
| A12 |  | same as ali, use prefix al2 |  |
| A13 |  | SAME AS A11, USE PREFIX A 13 |  |
| A14 |  | SAME AS A11, USE PREFIX A14 |  |
| A15 |  | sAME AS AII, USE PREFIX A1S |  |
| Anc |  | same as all, use prefix als |  |
|  |  | - |  |



Table 5-1. Reference Designation Index (Cont'd)


| $\begin{aligned} & \text { Refrence } \\ & \text { Destration } \end{aligned}$ | - Part No. | Description \# | Note |
| :---: | :---: | :---: | :---: |
|  |  | $\begin{aligned} & \text { A16 5000-3800 (CONT'D) } \\ & \text { A17 5000-5002 } \\ & 8000-623 \end{aligned}$ | $\begin{aligned} & A-L \\ & M-X \end{aligned}$ |
| A16R46 | 0683-3305 | Kz FXD COMP 33 OHM $581 / 4 \mathrm{M}$ |  |
| A16R47 | $0683-1635$ | R2FXD COMP 16K OHM $58.1 / 4 \mathrm{H}$ |  |
| A16R48 | 0683-1035 | R: FXD COMP 10 K OHM $581 / 4{ }^{\text {d }}$ |  |
| A16R49 Al6R50 | $0683-5625$ $0686-5625$ | R2FXD COMP 5600 OHm 58 l 1/4W |  |
| Al6R50 | 0686-5625 | R: FXD COMP 5600 OHM $581 / 2 \mathrm{~W}$ |  |
| A16R51 | 0683-1635 | R:FXD COMP 16K OHM 58 1/4M |  |
| A16R52 | 0683-1025 | R: FXD COMP 1000 OHM $581 / 4 \mathrm{~W}$ |  |
| ${ }^{16853}$ | $0683-4735$ | RifxD COMP 47K OHM $581 / 4 \mathrm{H}$ |  |
| A16R54 Al6R55 | $\begin{aligned} & 0683-1535 \\ & 0683-4725 \end{aligned}$ |  |  |
| A16R56 | 0683-1835 | RifXD COMP 18K OHM 58 1/4M |  |
| Al6R57 | 0686-4725 | R: FXD COMP 4700 OHM $581 / 2 \mathrm{~W}$ |  |
| A16R58 | 0683-4335 | R: FXD COMP 43 K OHM 58 1/4M |  |
| ${ }_{\text {Al }} \begin{aligned} & 16 R 600\end{aligned}$ | $0686-3325$ $0683-4335$ | Refxd Comp 3300 OHM $581 / 2 \mathrm{~W}$ |  |
| Al6R61 | 0683-4335 | RifXD COMP 43K OHM 58 1/4W |  |
| A16R63 | 0757-0954 | RzFXD FLM 18K OHM 28 1/8w |  |
| A16R64 A16R65 | -0757-0954 |  |  |
| A16R66 | 0757-0952 | R:FXD FLM 15K OHM 28 1/8W |  |
| A16R67 | 0683-3335 | RifxD Comp 33K OHM 5R 1/4W |  |
| Al6R68 | 0683-1835 | RiFXD COMP 18K OHM 58 1/4W |  |
| A16R69 | 0683-4725 | R:EXD COMP 4.7 K 5\% ${ }^{1 / 4 \mathrm{~W}}$ | A-F |
| Al6R70 | -0683-2725 |  | G-x |
| A16R71 | 0683-1015 | R:FXD COMP 100 OHM 58 1/4M |  |
| A16R72 | 0683-4725 | R:FXD COMP 4700 OHM $581 / 4 \mathrm{~W}$ | A-K |
| A16R73 | 0683-2725 | R 2 FXD COMP 2700 OHM $581 / 4 \mathrm{~W}$ | L-x |
| A16R74 | -0689-2725 |  |  |
| Al6R75 | 0683-2235 | R:FXD COMP 22K OHM 58 1/4W |  |
| A16R 76 | 0683-3335 | R:FXD COMP 33K OHK 58 1/4H | A-g |
| A16R77 | $0683-2735$ $0757-0943$ |  | $\mathrm{H}-\mathrm{x}$ |
| A16R78 | 0683-1635 | RiFXD COMP 16K OHM 58 1/4W |  |
| A16R79 | 0683-1635 | R:FXD COMP 16K OHM 58 1/4M |  |
| Al6R80 | 0683-1235 | R: FXD COMP 12K OHM 58 1/4H |  |
|  | $0683-1535$ $0683-4735$ | RifxD COMP 15K OHM $581 / 4 \mathrm{~N}$ |  |
| A16Re3 | 0683-4325 | R: R FXD COMP 4300 OHM $581 / 4 \mathrm{H}$ |  |
| A16R84 | 0683-2235 | R:FXD COMP 22K OHM $5811 / 4 \mathrm{~W}$ |  |
| A16R85 | 6683-4725 |  |  |
| A16R86 | $\begin{aligned} & 0683-2725 \\ & 2100-0369 \end{aligned}$ | R:FXD CONP 2700 OHM 58 1/4W R:VAR WH 200 OHM $102 \mathrm{LIN} 1 / 4 \mathrm{~W}$ | G-x |
| A17 | 5030.6002 | GATE COATROL |  |
|  |  | ant cluthol | A-L |
|  | 5080-6224 | GATE CONTROL | M-X |
| Al7C 1 | 0140-0194 | CifxD MICA 110 PF 58 |  |
| Alice | $0140-0194$ | Cifxd mica 110 PF 58 |  |
| Allic | 0140-0200 | C: FXD MICA 390 PF 58 |  |
| All Alich | $0140-0200$ $9.150-0121$ | C:FXX MICA 390 PF 58 C:FXD CER 0.1 UF +80-208 SOVOCN |  |

Table 5-1. Reference Designation Index (Cont'd)


Pable 5-1. Reference Designation Index (Cont'd)


Table 5-1. Reference Designation Index (Cont'd)





Table 5-1. Reference Designation Index (Cont'd)

Table 5-1. Reference Decignation Index (Cont'd)

|  | - Part No. | Deceripition \# | Nole |
| :---: | :---: | :---: | :---: |
|  |  | A22 5000-8010 | F-X |
| A22 | 8000-5610 | LOEIC CARD | F-X |
| $\begin{aligned} & \text { A22CR1- } \\ & \text { A22CRO } \end{aligned}$ | 1901-0041 | DICOE:SILICON 50 VOLTS MORKIMG |  |
| a22CR9 A22CR10 | $\begin{aligned} & 1901-0081 \\ & 1901-00 \mathrm{~A} \end{aligned}$ | UICOEBSILICON 50 VOLTS WORKIMG Dlcofisilitan 50 valis morimg |  |
| ${ }^{\text {A22 CR12 }}$ | 1901-0081 | DIODEISILICOM SO VOLIS WORKIMG |  |
| A22CR13 $A_{2} 2$ CR15 | $1901-0081$ $1901-0081$ | LIODE $\operatorname{sisilicom}$ so volis morimg |  |
| ${ }^{\text {a } 2226816}$ | 1901-0081 | DIDOEISILICOM 50 volts monkimg |  |
| ${ }^{\text {a } 22 C R 17}$ | 1901-0081 | DIDOEZSILICOM SO VOLTS WOXIMC |  |
| ${ }^{\text {a } 226818}$ | 1901-0081 | DICOE PSILICOW 30 Voliss moaximg |  |
| ${ }^{\text {A22CR23 }}$ | 1901-0041 | OLOOE a SILICOM 50 VOLTS mokrimg |  |
| A22CR25 | 1901-0081 | dicoersilicom so vols workimg |  |
| A22CR27 | 1901-0041 | didoersilicom so volis moakimg |  |
| ${ }^{\text {A220, } 28}$ | 1901-0081 | dLDoe isilicom so volis moaking |  |
| ${ }^{\text {A220, }} 3$ | 1901-0041 |  |  |
| A220 A2CR37 | 1901-0081 | DIDOE asilicon so volis morkimg DIODE ISILICOW so wotis working |  |
| ${ }^{\text {a22CR38 }}$ | 1910-0016 | didot igermaniun rooma at 0.85V gopiV |  |
|  | 1910-0016 | dicoeigermanium looma at o.ssV gopiv |  |
| ${ }^{122 C R 47}$ | 1901-0081 | didotrsilicom so volts wokkimg |  |
| ${ }_{\text {aracrsa }}$ | 1901-0081 | dLOOEsSILICON 50 volis mokkime |  |
| $\begin{aligned} & 128 \\ & 82 \end{aligned}$ | 1850-0114 | transistorigermaniun pmp |  |
| A22R1 | 0683-1835 | kifxD comp lek anm 58 1/4M |  |
|  | $0683-3335$ $0683-1535$ | K3FXD COMP 33 K OHM $581 / 4 \mathrm{M}$ RifXD COMP 15K 0HM 58 1/4Y |  |
| ${ }^{122284}$ | 0683-1635 | R2FXD com lek own 58114 H |  |
| ${ }^{\text {A2225 }}$ | 0683-3335 |  |  |
| A22R6 | 0683-1535 | RaFXD Cow 15 K OHM $581 / 4 \mathrm{~W}$ |  |
| ${ }^{422217}$ | 0683-1835 | Rifxo comp $10 \times \mathrm{mm} 581 / 4 \mathrm{~N}$ |  |
| A2288 A22as | $0683-3335$ $0683-1535$ |  |  |
| A22R10 | 0683-1835 |  |  |
| A22R11 | 068 3-3335 | R:FXD cow 33 K OWM $581 / 4 \mathrm{~W}$ |  |
| A22R12 | 0683-1535 | R3FXD Comp 15k OHM 58 1/4W |  |
| 422 R 13 | 0757-0946 | R3FXD FLM $8.2 \mathrm{~K} \mathrm{Omm} 281 / 8 \mathrm{M}$ |  |
|  | 0757-0950 | RifxD FLM 12 K OHM $281 / 8 \mathrm{BM}$ |  |
| A22R15 A22R 26 | $\begin{aligned} & 0757-0944 \\ & 0683-1835 \end{aligned}$ |  |  |
| A22017 | 0683-5625 | Rifxo comp 5600 |  |
| A22R18 | $0683-1035$ | RiFXD COM 10 K OHM $581 / 4 \mathrm{~W}$ |  |
| A22R A2 2 20 20 | $0683-1835$ $0683-5625$ |  |  |



| Mecrence | ()Part No. | Description \# | Note |
| :---: | :---: | :---: | :---: |
| A23 |  | A23 5090-3771 |  |
|  |  | 5050-5874 | -L |
|  |  | 5080-6203 | M-X |
|  | 5080-3771 | ac a Ohms delay gate | A-H* |
|  | 5050-5874 | ac a ohms delay gate | J-L* |
|  | 5060-8206 | ac \& Ohms delay gate | M-x |
| $123{ }^{1}$ | 0180-0196 | c: FXD ELECT 56 UF 15VdCh il |  |
|  | 0140-0194 | C: FXD MICA 110 PF 58 |  |
| A23C3 A23C4 | $0140-0200$ $0150-0121$ |  |  |
| ${ }^{\text {A } 23 C 5}$ | 0140-0200 | C: FXX MICA 390 PF 58 |  |
| ${ }^{123 C 6}$ | 0140-0194 | cafxd mica 110 PF 58 |  |
| $\begin{aligned} & A 23 C 7 \\ & A 23 C B \end{aligned}$ | $\begin{aligned} & 0140-0194 \\ & 0180-0701 \end{aligned}$ $0180-0291$ | C: FXD MICA 110 PF 58 <br> C: FXD ELECT LUF 10235 VDCH |  |
| $\begin{aligned} & \text { A23CR1- } \\ & \text { A23CR4 }^{233} \end{aligned}$ | 1910-0016 | UICOE : GERMANIUM looma at 0.85V gopiv |  |
| A23CR5 | $\begin{aligned} & \text { 1910-0010 } \\ & 1901-0081 \end{aligned}$ | diodesgermanium looma at o.b5V gopiv didoes silicon so volts morking | A-H |
| A23CR6 | 1910-0016 | UIODEEGERMANIUM 100MA AT O.85V GOPIV' | J-L $M-X$ |
|  | 1910-0016 | DI ODE EGERMANIUM 100MA AT 0.85V GOPIV | A-H |
|  | 1901-0081 | DIO OEISILICON 50 VOLTS MORKING | J-L |
|  | 1910-0016 | oldoer germanium 100ma at 0.85V gopiv | M-X |
| A23CR 7 | 1910-0016 | OIODE EGERMANIUM 100 Ma AT 0.85V GOPIV | A-H |
|  | 1910-0016 | DIODE EGERMANIUM LOOMA AI 0.85 V SOPIV |  |
| A23Cr8 | 1910-0016 | DIODE :GERMANIUM IOOMA AT O.85V GOPIV |  |
| A23CR9 A23CR10 | $\begin{aligned} & 1901-0061 \\ & 1901-0081 \end{aligned}$ | DIODE:SILICON <br> DIDDE:SILICON 50 VOLTS WORKING |  |
| A2301 | 1851-0024 | transistor:germanium npn |  |
| A2302 | 1850-0111 | TR ANSI STOR: GERMANIUM PNP | A-L |
| $\begin{aligned} & A 2303 \\ & A 2364 \end{aligned}$ | - | TRANSISTORI SILICON PNP |  |
|  | 1850-0113 | TRANSISTOR : GERMANIUM PNP |  |
|  | 1851-0006 | transistori 2ni69a NPN |  |
| $\begin{aligned} & A 2306 \\ & \text { A2307 } \end{aligned}$ | $1850-0111$ $1850-011$ | TRANSISTOR:GERMANIUM PNP TRANSI STOR: GERMANIUA PNP |  |
|  |  |  |  |
| A23R1 | 0683-3335 | R: FXD COMP 33K OHM 58 1/4N |  |
|  | 0683-2435 | R:FXD COMP 24K OHM 58 1/4W | $J-X$ |
| A23 | 0683-4735 | R:FXD COMP 47K OHM $581 / 4 \mathrm{M}$ | A-H |
|  | $0683-4335$ | R:FXD COMP 43K OHM $581 / 4 \mathrm{~W}$ | $J-\mathrm{x}$ |
| A23R 3 | 0686-5135 | R:FXD COMP 51K DHM 58 1/2W |  |
|  |  | *5060-6206 mar REPLACE 5060-3771 OR 5060-5874. |  |

\# See introduction to this section for ordering information


Table 5-1. Reference Destopation Index (Cont'd)

| Dencreetion | © Fart No. | Description \# | Note |
| :---: | :---: | :---: | :---: |
|  |  | A28 $058214-0014$ $05232-0007$ | ${ }_{\text {A-8 }}^{\text {T-X }}$ |
| A23 | 06214-5014 | InPUT AMPLIFIER | A-8 |
| $\mathrm{arcc}_{2}$ | 0180-0039 | Cifxo elect loouf 12vocm |  |
| ${ }^{2} 20 C^{2}$ | 0140-0198 | C2FXO Mica 200 pf 58 |  |
| ${ }^{\text {a } 26 C 3}$ | 018000063 | C: FXD ELECT S00UF -108+1008 3VOCW |  |
| ${ }_{\text {a } 20.0}$ | 0180-0050 | C 3 FXD ELECT 40 UF +75-108 SOVOCW |  |
| A2SCR1 | 1902-0199 | didotabreakdown s.8/10.0V 100MM |  |
| A26L1 | 9140-0027 | COIL 3 FXD RF 35 UH |  |
| 42601 | 1854-0003 | transistorimp silicon |  |
| $\begin{aligned} & A 2602 \\ & A_{2603} \end{aligned}$ | $\begin{aligned} & 1850-0037 \\ & 1850-0037 \end{aligned}$ | TRANSISTOR:GERMANIUM TRANSI STOR : GERMANIUM |  |
| A26R1 | 0683-6835 | R F FXD Comp bek own 58 1/4M |  |
|  | 0683-1845 | RiFXD COMP 180K OMM $581 / 4 \mathrm{M}$ R:FXD COMP 33K OHM $581 / 4 M$ |  |
| A26R4 | 0693-1545 | RiFXD COMP 150R OHM 58 1/4W |  |
| a26RS 42686 | $0683-2235$ $0683-3935$ |  |  |
| 42607 | 0683-2725 | Rifxo comp 2700 OHm $581 / 4 \mathrm{M}$ |  |
| A26R8 | 0683-6225 | R3FXD COMP 6200 OHM $581 / 4 \mathrm{M}$ |  |
| ${ }^{\text {a } 26089}$ | 0683-6815 | RiFXD Comp $680 \mathrm{OHM} 581 / 4 \mathrm{M}$ |  |
| A26R10 A26R 11 | $0683-1515$ $0683-1035$ |  |  |
| $\begin{aligned} & \text { A26R12 } \\ & \text { A26A } 13 \end{aligned}$ | $\begin{aligned} & 0683-1025 \\ & 0683-4735 \end{aligned}$ | Rifio comp 1000 OMM 58 1/4M RaFXD COM 47K OHK 58 1/4N |  |
| A2S | 06232-4007 | IMPUT AMPLIFIER | T-X |
| $\mathrm{arcc}_{1}$ | 0180-0039 | Cifxo elect loour l2vocm |  |
| ${ }^{\text {asect }}$ | 0180-0124 | CiFXO ELECT 200uF ovoch |  |
| ${ }_{\text {A20, }}$ | 0180-0104 | CiFXD ELECT 200UF 15 SVOCN |  |
| A2acs | 015000121 |  |  |
| A26C6 | $0140-0177$ | Ci FXD MiCA 400 PF 18.208 |  |
| A26CR1 | 1910-0011 | didoesgermanium sha at iv |  |
| A2601 | 1854-0003 | TRANSISTOR:MPN SILICOM |  |
| 42602 42603 | 1853-0909 | TRANSISTOA SILIICOM PNP TRANSISTOR SILICOM PMP |  |
| ${ }_{4}^{4} 2604$ | 1053-0009 | TRANSISTOR:SILICOM PMP |  |
| A26R1 | 0603-2735 |  |  |
| A26a 2 | 0603-1025 | RiFFX comp 1000 omm 58 l 1/4M. |  |
|  | 0603-2735 | R, FXO COMP 27K OMM $581 / 4 M$ |  |
|  | 0613-6225 | ReFXD COw 6200 OHm 58114 M |  |
| A2CR6 | 0683-1025 | Riffo cow 1000 OHM 58 1/4W |  |

Table 5-1. Reference Designation Index (Cont'd)


Table 5-1. Reference Dealgation Index (Cont'd)



Table 5-1. Reference Designation Index (Cont'd)


Table 5-1. Roference Dealemation Index (Cont'd)


Table 5-1. Reference Designation Index (Cont'd)



Table 5-1. Reference Deaignation Index (Cont'd)

| Deecreman | - Part No. | Descripition \# | Note |
| :---: | :---: | :---: | :---: |
|  |  | A33 s000-3me (COWT'D) |  |
| A33AIC8 | 0160-0166 | Cifxd hy 0.1 Uf 108200 VOCm |  |
| A33aicrs | 1910-0025 | diodesge lisiv ons |  |
| A33A1CR6 A33AICR7 | 1901-0081 $1901-0081$ | didotesillicom so valts morxing UICOE ESILICOM 50 VOLTS WORKING |  |
| A33AICR9 | 1901-0081 | DLOOErSILICOM 50 VoLts working |  |
| A33A1L1 | 9140-0174 | COILIFXO RF 220 me 58 |  |
| A33A1L2 | 9140-0075 | COIL:FXD RF 270 UF | : |
| A33A103 | 1850-0111 | transistorigermanilum pmp |  |
| A33A104 | 1853-0308 | transistonisilicon pmp |  |
| A33A105 | 1850-0032 |  |  |
| A33A106 | 1850-0032 | TRANSISTORigermanium Pmp 2 ma 04 |  |
| A33A1R15 | 0757-0280 | Asfid met flm ik owm is 1/8M |  |
| A33A1R16 A3SALR17 | $0757-1102$ $0757-0198$ | Rz FXD MET FLM 180 OUM 18 1/8N |  |
| A33Ainis | 0757-0200 | R: FXD MET FLM 9.62 KOHM 18 1/EM |  |
| A33A1R19 | 0757-0816 | KifXD MEI FLM 681 OHM is $1 / 2 \mathrm{~W}$ |  |
| A33A1R20 | 0757-1060 | RZFXD MET FLM 1960 WH 18 1/2W |  |
| A33A1R21 A3SA182 | 0757-0444 | R:FXD MET FLM 12 . 1 K OHM $181 / 8 \mathrm{M}$ |  |
|  | $0757-0276$ | RBFXD MET FLM 1.7ex OHM IS I/SW |  |
|  | O696-3130 $0696-3132$ |  |  |
| A33A1R25 | 0698-3134 | RSFXD MET FLM $1.33 \mathrm{~K} 0 \mathrm{HM} 181 / 4 \mathrm{M}$ |  |
| A33A1R26 | 0698-0035 | RiFXD MET FLM 2.61 K OHM 18 1/8w |  |
| A33A1R27 | 2100-0371 | Rivar WH IK OHM 108 LIM 1/4M |  |
| A33A1R28 | 0757-0731 | RiFXD MET FLM 025 OMm 18 1/4W |  |
| ${ }^{333121 R 32}$ | 2100-1433 | Ri VaR MH 100 OHM 58314 M |  |
| A33A1R33 | NRFR | RiFXO CARBOM FLM 5-40 OHM SELECTED in test. | : |
| A33A1R34 A33A1R35 | $\begin{array}{r} 0757-0458 \\ 0757-0438 \end{array}$ | RifXD MET FLM Sl.1K OHM 18 I/SM RiFXD MET FLM 5.11 K OHM 18 L/en |  |
| A3 3 A1t 2 A $33 A 1 W 1$ | 9130-0028 <br> 5950-0001 | pransformer JUMPER WIRE |  |
| A33A2 | 5060-3830 | Bimary PC |  |
| A33A2C1 | 0140-0192 | Cafxo mica 68 Pf 58 |  |
| A33A2C2 | 0140-0192 | cifxo mica de pf 58 |  |
| A33A2CR1 | 1901-0081 | didotisilicom so volis morkinc |  |
| A33A2CR2 $\mathrm{A}^{\mathrm{A} 33 \mathrm{~A} 2 \mathrm{CR}} \mathrm{B}$ A33A2CR4 | $\begin{aligned} & 1901-0081 \\ & 1910-0025 \\ & 1910-9025 \end{aligned}$ | DICOE ISILICOM so valis morkinc didoeetge limiv ans DIOOEIGE LSWIV GNS |  |
| A33A201 | 1850-0075 | transistorigermaniom pnp |  |
|  |  | $\begin{aligned} &:: \text { REPLACES C6 IN CERTAIN APPLICATIONS } \\ & \text { :: SUBSTITUTED FOR WI WHEN L2 IS USED } \end{aligned}$ |  |

Table 5-1. Reference Designation Index (Cont'd)


Table 5-1. Reference Designation Index (Cont'd)

\# Bee introduction to this eection for ordoring tinformation

| Deifrema | OPat No. | Description \# | Note |
| :---: | :---: | :---: | :---: |
|  |  | MAIN CHASSIS (CONT'O) |  |
| cR2 | 1901-0000 | UIOOE:SILICON |  |
| CR3 ${ }_{\text {CR20 }}$ | $1901-0060$ $1901-0081$ | DIDEESILICON |  |
| CR20 | $1901-0081$ $1901-0081$ |  | G-x $H-x$ |
| $\begin{aligned} & F_{1} \\ & F_{2} \end{aligned}$ | $\begin{aligned} & 2110-0006 \\ & 2110-0007 \end{aligned}$ | fuseicartridge zamp l25v slow blow FUSEICARTRIDGE 1 AMP 250V SLOW BLIO KEPL竍ES FI FOR 23OV OPERATION. |  |
| FLI | $9110-0103$ $9100-2477$ | filteriline b wire r.sa filteriline 3 WIRE 1.5A | A-t |
| J1 | 1251-0119 | connafemale 37 cuntacts |  |
| 32 | $1251-0087$ $1250-0118$ | COMMECTORZFEMALE 50-PIN Minat |  |
| ${ }^{54}$ | 1250-0118 | COMWEC TOR : BMC |  |
| J6 | 1250-0118 | COMNEC TOR : BMC |  |
| J9 | 1250-0118 | CUMNEC TOR : BNC. |  |
| J31 | 1251-0349 | cumaguarded chassis 3 pin male |  |
| 4 | 9110-0067 | Chowes 35 mh 2.5A |  |
| 01 | $\begin{aligned} & 1850-0132 \\ & 1853-0011 \end{aligned}$ | transistoragermanium pnp TRANSISTOR:SILICON PNP | A-J $\mathrm{k}-\mathrm{x}$ |
| 02 | 1850-0132 | TRANSIS SOR : GERMANIUM PNP | A-J |
| -03 | $1850-0064$ $1853-0008$ |  | $\mathrm{G}_{\mathrm{i}}$-x |
| R1 | 0813-0007 | R:FXD WW 10K OHM 1085 S |  |
| R2 | 0816-0014 | RiFXO WM 1250 OHM 108 10w |  |
| R3 | 0692-1025 | R:FXD COMP 1K OHM 58.2 LN | A-J |
| R4 | - 0686 -6825 |  | k-x |
| RS | 0686-4745 | RIFXD COW 470k OHM 58 1/2W |  |
| R6 | 0603-1025 | KifxD COMP 1000 OHM 58 $1 / 4 \mathrm{H}$ |  |
| R7 | 0683-1025 | R2FXD COMP 1000 OHM $581 / 4 \mathrm{M}$ |  |
| R88 | - $0683-6835$ |  |  |
| R11 | 0683-1015 | H2FXO COMP 100 OHM $581 / 4 W^{\prime}$ | $\mathrm{H}-\mathrm{x}$ |
| $\mathrm{R12}$ | 0683-4715 | Rifxo Comp 470 OHM $581 / 4 \mathrm{~W}$ | H-x |
| R202 | 0686-1135 | H2FXD COMP 11K OHM 58 1/2N |  |
| R203 | NSR ${ }_{\text {O6-4335 }}$ | R: FXD COMP 43K OHM 58 1/2w (PART OF S5) | , |
| S1 | 3100-1402 | SwItchzrotary a pos 3 SECt |  |
| S2 | 3100-0711 | Smitchzmotary 12 pole 3 on 4 pos |  |
| 53 54 5 | 310000464 $3101-0004$ | SMITCH2ROTARY 6 POLE O POS |  |
| 55 | 3100-0466 | SMITCHRROTARY W/2SOK OHM RESISTOR |  |
| S6 | 3101-0005 | Smitchitog dpot jan astizn |  |
| 57 | 3101-0001 | switchatogele spst | ' |
| S10 S11 | $\begin{aligned} & 301-0001 \\ & 3101-0033 \end{aligned}$ | SWITCH: TOGGLE SPST SMITCHISLIDE DPDT |  |

\# See introduction to thin section for ordertas information

Table 5-1. Reference Dealemation Index (Cont'd)


\# See introduction to this secition for ordering information

Table D-1. Referanoe Denienation Index (Cont'of










## TABLI S-3. St Of MANUPACTURERS


tacli s-s.
COOA LIST of manupactunces (coñinued)
 <br> \title{
TABLE 3.3. <br> \title{
TABLE 3.3. <br> ćODE LIST OP MANUPACTURGIL (Continud)
}

# MANUAL SUPPLEMENT 

Model HP-2401C<br>Infegrating Digital Volimeter<br>Opfion 21

## l

### 21.1 OENERAL DEBCRIPTION

The HP-2401C-21 Integrating Digital Voltmeter provides positive true recorder outputs in 8-4-2-1 binary code instead of the 4-2'-2-1 code provided by the standard HP-2401C recorder outputs. (See Tables 2-4 and 21-1.) Except for this difference in coding, the specifications in Section 1.7 apply without change to the HP-2401C-21.

### 21.2 INSTALLATION AND OPERATION

Install, operate, and program the HP-2401C-21 as specified in Section II of this manual.

### 21.3 THEORY OF OPERATION

The theory of operation of the HP-2401C-21 is the same as that of the standard HP-2401C except as noted in the following paragraphs.

### 21.3.1 Prinfer Coupling Logic A22 (Figure 21-1)

The logic and circuitry shdwn in Figure 21-1 converts decimal and function inputs to 8-4-2-1 BCD outputs for recording. The decimal $10^{-\mathrm{n}}$ and function numbers from this assembly are identical to those from a standard printer coupling logic asssembly, but they are in 8-4-2-1 code instead of 4-2'-2-1 code.

### 21.3.2 Reversible Decade Counfors All-A15 and A46 (Figure 21-2)

The decade counter shown in Figure 21-2 differs from that shown in Figure 4-17 only in the arrangemed ofinedback. The waveforms associated with forward and backward couligig of HP-2401C-21 decades are shown in the circuit diagram, Figure 2 H 2.

The decades always count up during frequency measurements and during. the first phase of voltage measurements. Up counting is enabled when the count down line is clamped to ground (positive true) and the count up line is near. -35 v . Both of these signals are provided by Counter Control Logic on A16. These states close the down count AND gates and open the up count AND gates. Positive triggersare coupled from the collectors of odd-numbered transistors (Q1, Q3, Q5, Q7) to succeding stages. Each trigger advances the count by one. When the count is advanced from nine to zero, the turn on of Q7 generates a trigger that increases by one the count in the
next decade, and so on through all six counting units. The up count progression is as follows:


At the forward count of eight, conduction through Q8 and CR20 inhibits triggering of Q3-Q4 by Q1, assuring that Q3-Q4 and Q5-Q6 remain in zero state (Q3 and Q5 on) when the count of ten resets Q1-Q2 to zero state. The resetting of Q1-Q2 to zero state also resets Q7-Q8 to zero state through forward count AND diode CR13 and OR diode CR21.
Down counting is commanded by the Counter Control Logic on A16 when the polarity of the input voltage reverses. This is enabled by the positive-true state of the count $\overline{u p}$ line, which closes the up count AND gates, and the negative-true state (near -35v) of the count down line, which opens the down count AND gates. Positive triggers are then coupled from the collectors of even-numbered transistors to succeeding stages. The count progression is exactly the reverse of the up count progression, which is summarized above.

Starting from the zero state:
a. The first reverse count trigger sets binary Q1-Q2, triggering binaries Q3-Q4, Q5-Q6, and Q7-Q8 to set state through rever se count AND diodes CR14, CR16, and CR18. Turn-on of Q8 triggers binaries Q3-Q4 and Q5-Q6 back to zero state, leaving Q2 and Q8 on, representing a nine count.
b. The next trigger sets Q1-Q2 to zero state, reducing the count to eight.
c. The third trigger sets Q2, Q4, and Q6 on, which resets Q7-Q8 to zero state, establishing the count of seven.

The remaining triggers continue subtraction as indicated so long as the reverse count is enabled. Each time a trigger sets the decade from zero to nine during leverse counting, the turn on of Q8 triggers the next decade through reverse count AND diode CR22, reducing the count of the next decade by one.

### 21.4 MAINTENANCE

Figures 4-17, 4-23, and 4-24 are superseded by Figures 21-1 and 21-2 in this section; performance checks 15 and 16 of Table 4-3 are replaced by checks 21.1 and 21.2 in Table 21-2. Otherwise, the maintenance instructions in Section IV of this manual are directly applicable without change to the HP-2401C-21.

Table 21-1 Function Coding

| Data | Function | Logic | 8 | 4 | 2 | 1 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | Period (W/30) |  | 0 | 0 | 0 | 0 |
| 1 | +VDC |  | 0 | 0 | 0 | 1 |
| 2 | -VDC |  | 0 | 0 | 1 | 0 |
| 3 | KC |  | 0 | 0 | 1 | 1 |
| 4 | K $\Omega$ (W/HP-2410B) |  | 0 | 1 | 0 | 0 |
| 5 | $\mathrm{M} \Omega \quad$ (W/HP-2410B) |  | 0 | 1 | 0 | 1 |
| 6 | Spare |  | 0 | 1 | 1 | 0 |
| 7 | Spare |  | 0 | 1 | 1 | 1 |
| 8 | Time |  | 1 | 0 | ${ }^{2}$ | 0 |
| 9 | Overload - |  | 1 | 0 | 0 | 1 |
|  | VAC (W/HP-2410B) |  | 1 | 0 | 1 | 1 |

### 21.5 PARTS LIST

The Parts List in Section V of this manual applies to the HP 2401C-21 except as indicated in Tables 21.-3 and 21-4.

Table 21-2. In-Cabinet Performance Checks
Perform checks 1 through 14 and 17 through 24 as specified in Table 4-3 and Section 4.2.
21.1 RECORDING OUTPUTS - BCD FUNCTION

1 digit.
4-line 8-4-2-1 code.
" 0 " state level, -35 to -24.5 V ; " 1 " state level, -2.5 to 0 V .
Source impedance, 33K.
a. Determine and record dc function levels at the following pins of J2:

*W/dc input sufficient to produce OVERLOAD indication.
b. The source impedance is determined by fixed value 33 K resistors, which can be seen in the assembly A22 circuit diagram in Figure 21-1.
21.2 RECORDING OUTPUTS - BCD DECIMAL POINT

Specifications same as for 21-1.
a. Set HP-2401C FUNCTION switch to VOLT, other controls as specified below; determine and record dc decimal levels at the following pins of J2; short-circuit HI, LO, and GUARD terminals to assure all zeros reading.

|  |  |  | J2 Pin: | 27 | 26 | 2 | 1 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Range | Sample Period | Decimal Position | Code: | 8 | 4 | 2 | 1 |  |
| 1000 V | .01 Sec | $000000 . \mathrm{V}$ |  | $\overline{0}$ | 0 | 0 | 0 | $\left(10^{-0}\right)$ |
| 1000 V | 0.1 Sec | 00000.0 V |  | 0 | 0 | 0 | 1 | (10-1) |
| 100 V | 0.1 Sec | 0000.00 V |  | 0 | 0 | 1 | 0 | $\left(10^{-2}\right)$ |
| 10 V | 0.1 Sec | 000.000 V |  | 0 | 0 | 1 |  | $\left(10^{-3}\right)$ |
| 1 V | 0.1 Sec | 00.0000 V |  | 0 | 1 | 0 | 0 | $\left(10^{-4}\right)$ |
| 0.1 V | 0.1 Sec | 0000.00 MV |  | 0 | 1 | 0 | 1 | (10-5) |
| 0.1 V | 1.0 Sec | 000.000 MV |  | 0 | 1 |  | 0 | $\left(10^{-6}\right)$ |
| 0.1 V | 1.0 Sec | 00.0000 MV |  | 0 | 1 | 1 | 1* | $\left(10^{-7}\right)$ |

**W/HP-2411A at +10 gain ( 10 MV full scale), FUNCTION at EXT SEL, Card A30 installed.
b. Disconnect short from HI, LO, and GUARD terminals. Set HP-2401C FUNCTION switch to FREQ, ATTENUATION control just clockwise from switched CHECK position, other controls as specified below. Use DC Null Voltmeter to check decimal levels at the following pins of J 2.

|  |  |  | J2 Pin: | 27 | 26 | 2 | 1 |
| :--- | :--- | :--- | ---: | :--- | :--- | :--- | :--- |
| Sample Period | Decimal Position |  | Code: | 8 | 4 | 2 | 1 |
| 01 Sec | 00000.0 KC |  |  |  |  |  |  |
| 0.1 Sec |  |  | 0 | $\frac{0}{0}$ | 0 | $\frac{1}{1}$ | $\left(10^{-1}\right)$ |
| 1.0 Sec | 0000.00 KC |  | 0 | 0 | 1 | 0 | $\left(0^{-2}\right)$ |
| STOP | 000.000 KC |  | 0 | 0 | 1 | 1 | $\left(10^{-3}\right)$ |
|  | 000000 |  | 1 | 0 | 1 | 1 | $\left(10^{-0}\right)$ |

c. The source impedances are determined by fixed value 33 K resistors, which can be seen in the assembly A22 circuit diagram in Figure 21-1.

HP. 240IC PERFORMANCE CHECK TEST CARD
SER $\qquad$ - _ oate $\qquad$


Table 21-3. Reference Designation Index


Table 21-3. Reference Designation Index (Cont'd)




Table 21-3. Reference Designation Index (Cont'd)

| $\begin{aligned} & \text { Reference } \\ & \text { Designation } \end{aligned}$ | (1)Part No. | Description | Nofe |
| :---: | :---: | :---: | :---: |
|  |  |  |  |
| A22R60 A22R61 | 0683-3335 0683-2045 |  |  |
| A22R62 | 0683-1335 | R: FXD COMP 13K $0 \mathrm{HM} 581 / 4 \mathrm{~W}$ |  |
| ${ }^{\text {A22R63 }}$ | 0683-3335 | R: FXD Comp 33K OHM $581 / 4 \mathrm{~W}$ |  |
| A22R64 | 0683-2035 | R:FXD COMP 20K-OHM $581 / 4 \mathrm{~W}$ |  |
| A22R65 | 0683-2035 | R:FXD COMP 20K OHM 5x 1/4W |  |
| A22R66 | 0683-3.335 | R: FXD COMP 33K OHM 58 1/4 ${ }^{\text {d }}$ |  |
| ${ }_{\text {A22R67 }}$ | 0683-2045 | R: FXD COMP 200K. OHM 5x 1/4 |  |
| A22R68 | 0683-1335 | R:FXD COMP 13K OHM $581 / 4 \mathrm{~N}$ |  |
| A46 |  | Same as all, use prefix a4b |  |

Table 21-4. Replaceable Parts



Stock No. 5060-5611 (For Serial Prolix 537 and above)
A22 Printer Couplings



Stock No. 5060-5066
(A11-A15, A46) Reversible +8-4-2-1 Decade Counter for Option 21


# MANUAL SUPPLEMENT <br> MODEL HR-2401C Integrating Digital Volimeter Option 29 

## 29.1 - GENERAL DESCRIPTION

The HP-2401C-29 Integrating Digital Voltmeter is capable of frequency measurement to 1.2 megahertz. This option is available with 8-4-2-1 positivetrue or negative-true BCD output. The specifications in Section 1.7 of this manual apply without change to the HP-2401C-29.

### 29.2 INSTALLATION AND OPRRATION

Install, operate, and program the HP-2401C-29 as specified in Section II of this manual.

### 29.3 THEORY OF OPERATION

The theory of operation of the HP-2401C-29 is the same as that of the standard HP-2401C, except as noted in the following paragraphs.

### 29.3.1 1 MHz Input Amplifier and Trigger Assemblies A26 and A27 (Pigure 29-1, Standard on Serial Prafix 735 and Above)

The Input-Amplifier (A26) and Schmitt Trigger (A27) assemblies used in the HP-2401C-29 incorporate circuit constants and transistors which are selected to achieve amplification and switching of signals with frequencies up to 1.2 megahertz. Otherwise these circuits, shown in Figure 29-1. are identical to those used in the standard HP-2401C.

### 29.3.2 I Megahertz Gate Assembly A3s (Figure 29-2)

In the HP-2401C-29, a special Ymegahertz gate assembly. A38 performs the counter input gating functions which are performed by circuitry on A19 in the standard instrument. To minimize degradation of the input signal and reduce noise susceptibility of the instrument, the gate assembly is located close to the 1 megahertz counting/display decade. A11.

As lindicated in Figure 29-2, frequency pulses are received from Schmitt Trigger A27(6). Whenever the FREQ function is selected. the negative-true state (near $-35 v$ ) of the freq line opens AND gate CR1-CR2 to the frequency input pulses. At the same time, the positive-true state (near ground) of the volt line closes AND gate CR4-CR5 to volt pulses which are received from Counter Control Assembly A16.

Selection of the VOLT function reverses the states that are applied to A38. The negative-true state of the volt line opens AND gate CR4-CR5 and the positive-true state of the freq line closes AND gate CR1-CR2.

Inverted frequency pulses from $Q 1$ or volt pulses from $Q 2$ are coupled through counter driver Q3 to counter decade A11. The output from Q is differentiated
by C4-R11-R12 to produce the positive spike that is required for triggering the counting decade.

### 29.3.3 Reversible 1 MHz +4-2'-2-1 Decade Counter All (Figure 29-3)

The transistors and circuit constants of decade counter A11 are selected to achieve the fast switching that is required for counting signal frequencies to 1.2 megahertz. The base-emitter junctions of the transistors are protected from reverse bias punch-through by diodes CR25 and CR35-CR41. Otherwise decade A11 is identical to decades A12-A15 and A46.

### 29.3.4 Reversible 8-4-2-1 Decade Counfer (Figure 29-4)

Except for the circuit constants and transistors (which bre selected for fast switching) and diodes CR25 and CR35-CR41 (which protect the transistors from reverse bias punch-through), the decade counter A11 used in HP-2401C29/21 and 29/35 instruments is the same as the decade counter described in Sections 21 and 35 of this manual:

The BCD output logic (negative-true or positive-true) supplied from the basic $8-4-2-1$ decade is determined by the connection of shorting links. The circuit in Figure 29-4 shows the connections used for negative-true BCD output, wherein the " 1 " state is near $-35 v$ and the " 0 " state is near ground. As shown, the shorting links are connected between $-1,-2,-4$, and -8 terminals and the BCD outputs of the decade. Positive-true BCD output is provided from this basic decade by connecting the shorting links from the $+1,+2,+4$, and +8 terminals to the BCD outputs. Positive-true output reverses the states previously mentioned: " 1 " state is near ground and " 0 " state is near. -3.5 v .

### 29.4 MAINTENANCE

Figures 29-1 through 29-4 show parts placement and circuit configurations of A11. A26, A27, and A38 for HP-2401C-29, 29/21, and 29/35 instruments. See Figure 29-5 for location of A38, R12, and R13 added for Option 29. Figure 29-6 shows interconnections of the HP-2401C-29 where they differ from those of the standard HP-2401C. Except for the foregoing, the maintenance information in Section IV (and Section 21 or 35 if applicable) of this manual applies without change to all versions of the HP-2401C-29. Assemblies A26 and A27 described in this section are standard on instruments with serial prefix 735 and above.

### 29.5 PARTS LIST

The Parts List in Section V of this manual applies to the various versions of the HP 2401C-29 except as indicated in Tables 29-1 and 29-2.
$-$
Table 29-1. Reference Designation Index


See introduction to this rection for ordering information


Table 80-1. Redorence Deolemantion inder (Cont'A)

Table 80-1. Reforence Desigmation Index (Cont'd)


| Demmention | - Part No. | Descripition \# | Nele |
| :---: | :---: | :---: | :---: |
|  |  | OpT1ON 22/21, $2: / 38$ A11 gopa-cich sepocin |  |
| A26 | 05232-6007 | input Amplifier | A-S |
| ${ }^{\text {A } 27}$ | 05232-6006 | SCMMITT TRIGGER | A-S |
| A388 | $5060-5700$ $5060-5644$ | 1 IMHZ GATE ASSEMBLY |  |
|  |  |  |  |
| ${ }_{\text {chi }}$ | -1901-0025 | C:FXD CER 0.1 UP $+80-201$ SOVDCH DIODE:SILICON 100 MV 100MA | A-S |
| CR4- |  |  |  |
| CR11 | 1901-0025 | DIODE: SILICON 100 MV 100MA |  |
| R12 | 0683-4715 | R:FXD COMP 470 OHM $511 / 4 \mathrm{~N}$ | M-x |
| ¢ 213 | $0683-4715$ $1251-0135$ | R:FXD COMP 470 Otm St $1 / 4 \mathrm{H}$ CONNECTOR:BOOY 15 PIN |  |
|  |  |  |  |
| A11 | $\begin{aligned} & 6000-6965 \\ & 6000-6006 \end{aligned}$ | 1 miz Reveremele decade counter 1 MHZ REVEREMELE DECADE COUNTEA |  |
| Allal | NSR | hendout block assy |  |
| $\begin{aligned} & \text { Alici- } \\ & \text { Allico } \end{aligned}$ | 0160-2101 | CiFXD MICA 2TPF 28 300VOCH |  |
| Allc Alics | $0140-0191$ $0160-2101$ | CiFXD MICA CiFXD PF SICA 27PF 28 300VDCM |  |
| Alics | 0140-0195 | CifxD MICA 130 PF 58300 VOCM |  |
| Alicto | 0160-2232 | Cifxd Mica 33 PF 283300 VDCW |  |
| Allicil | 0160-2232 | C2FXO MICA 33 PF 28 300VDCM |  |
| ${ }^{\text {Alicil }}$ | 0140-0195 | C: FXD MICA 130 MF 58300 VOCN |  |
| A11C13 | 0160-2232 | CiFID MICA 33 PF 28 300VDCH |  |
| AllC Al | 0160-2232 | C: FXD MICA 33 PF 28 300VOCW |  |
| Allic15 $\begin{aligned} & \text { All } \\ & \text { All }\end{aligned}$ | $0160-2232$ $0160-2232$ | C2FXO MICA Ci |  |
|  |  |  |  |
| AllC17 <br> AllCle | $\begin{aligned} & 0160-2232 \\ & 0160-2232 \end{aligned}$ | C\& FXO MICA 33 PF 28 300VOCW <br> CaFXD MICA 33 PF 28 300VDCW |  |
| $\begin{aligned} & \text { AlICR1- } \\ & \text { AllCRE } \end{aligned}$ | 1901-0025 | DICOEFSILICON 100WV 100ma |  |
| Alicra- Alicata | 1901-0081 | OLDOE:SILICOM SO VOLTS MORKIMG |  |
| Allicre2s | 1901-0143 | DICOESSILICON |  |
| Allce34 | 1901-0081 | DICOE:SILICON 50 VOLTS WORKING |  |
| AllCR35- <br> AlICR41 | 1901-0143 | OLCOE:SILICOM |  |
| $\begin{aligned} & \text { A1101- } \\ & \text { Al108 } \end{aligned}$ | 1853-0004 | TRANSISTOR:SILICON PNP |  |
| Alint | 0603-3945 | R2FXD COMP 390K OHM $581 / 4 \mathrm{M}$ |  |
| AllR2 AllR3 | 0683-563b 0683-5635 |  |  |
| Aling | 0683-1045 | R:FXD Comp look ohms 58 1/4M |  |
| Al1as All | $0683-3945$ $0683-5635$ |  |  |

Table 29-1. Reference Designation Index (Cont'd)

|  | - Part No. | Descripition \# | Note |
| :---: | :---: | :---: | :---: |
|  |  | OPTION 20121, 20135 <br> A11 $\qquad$ (conTP) |  |
| A1187 | 0683-5635 | RiFxo comp 56 K Dums $581 / 4 \mathrm{M}$ |  |
| ${ }^{\text {allit }}$ | 0683-1045 | R, FXO COMP 100K OHMS $581 / 4 \mathrm{M}$ |  |
| A1189 | 06033-3943 | R2FXO COMP 390K OHH $5811 / 4 \mathrm{M}$ |  |
| Al1R10 Allill | $0683-5635$ $0683-5635$ |  |  |
| A11R12 | 0683-1045 | ki FXD Comp look oums 58114 M |  |
| Allikis | 0683-3945 | RiFXD COMP 390K OHM $581 / 4 \mathrm{H}$ |  |
| allal4 | 0683-5635 | RifxD Comp sck onms $581 / 4 \mathrm{M}$ |  |
| Allats | 0683-5635 | RiFXD COMP 56K OHMS 58 1/4W | / |
| A11a 16 | 0683-1045 | R, FXD COMP 100 K OHMS $581 / 4 \mathrm{M}$ |  |
| Al1a 17 | 0683-1035 | R, FXD COM 10 K OHM $581 / 4 \mathrm{M}$ | A-G |
|  | 0683-2235 | RifxD COMP 22K OHM $58.1 / 4 \mathrm{M}$ | H-x |
| Allkie ${ }_{\text {alin }}$ | -063-1835 | Rifiol R |  |
| Alliz20 | 0683-2235 | RiFXD Comp 22k Owm 58 1/4W |  |
| A11R21 | $0683-2235$ | RiFXD COMP 22K OHM 58 1/4M |  |
| A11R22 | 0683-2235 | R:FXD COMP 22K OHM 58 1/4M |  |
| A11R23 | 0603-1035 | Rifxo com lisk OHM 58 1/4M |  |
| A11024 | 0633-6835 | aifxo comp bek 0 WM 58 1/4W | A-6, |
|  | 0683-3935 | RifxD conp 39x Owm 58 1/4M | H-x |
| AllR2S | 0683-1835 | RiFXD COM 18K OMM $581 / 4 \mathrm{~N}$ | A- |
| A11R26 | $0633-2235$ $0633-1225$ |  | A-6. |
| A11027 | 0686-5625 | R 3 FXD COWP 5600 OHM $581 / 2 \mathrm{~W}$ |  |
| A11R28 | 0686-5025 | R: FXD COMP 5600 OHM $581 / 2 \mathrm{~N}$ |  |
| A11829 | 0686-5625 |  |  |
| Al1R30 | 0680-5625 | R:FXD COMP 5600 OHM $581 / 2 \mathrm{~W}$ |  |
| Alir3i | $\begin{aligned} & 0683-6835 \\ & 0683-4735 \end{aligned}$ | RiFXD COMP 6aK OHM 58 1/4W RifxD COMP 47K OHM 58 1/4M |  |
| A11R32 | 0686-5625 | RifxD COMP S600 OHM $581 / 2 \mathrm{~W}$ |  |
| ${ }^{\text {Al }} 11833$ | 0686-5625 | R 2 FXD COMP 5600 OHM $581 / 2 \mathrm{~W}$ |  |
| A11034 | 0683-6835 | RiFXD COMP 68K OHM 58 1/4W | A-s, |
| A11035 | $0683-4735$ $0663-6835$ | K2FXD Rif | H- |
| A11836 | 0686-5629 | Rafxo COMP 5600 OHM $581 / 2 \mathrm{~W}$ |  |
| A11837 | 0686-5625 | R2FXD COMP 56000 OHM $581 / 2 \mathrm{~W}$ |  |
| AllR38 | 0683-6835 <br> 0683-5635 |  | ${ }_{\text {A. }}^{\text {A. }}$ |
| $\begin{aligned} & \text { Al1R 39- } \\ & \text { A11R50 } \end{aligned}$ | 0683-5635 | RifxD COMP 56K DHMS $581 / 4 \mathrm{H}$ |  |
| AllRs All All | $0683-3025$ $0683-5635$ | Rifxo comp RiFXD comp S6K |  |
| Alless | 0683-5635 | RiFXD COMP S6K OHNS 58 1/4W |  |
| Al1R54 | 0683-5635 | RIFXD COMP S6K OHMS 58 1/4M |  |
| Allass | 0683-5635 | Refxo Cowp 56k OHMS 58 1/4M |  |
| Al1 1856 Alin5 | $0683-3025$ |  |  |
| Allinse | $0683-5635$ $0683-5635$ |  |  |
| A11R59 | $0683-5635$ | RiFXD COMP 56K OHMS $581 / 4 \mathrm{~W}$ |  |
| AllR60 | 0683-5635 | R:FXD COMP S6K OHMS 58 1/4M |  |



Table 29-2. Replaceable Parts

| (\%) Put No. | Decorticica \% | Mth. | Mis. Pert No. | 70 |
| :---: | :---: | :---: | :---: | :---: |
|  | OPTION 20 |  |  |  |
| 0140-0014 | c: fxd mica 56 PF 108 | 00853 | RCM 15 S S60K |  |
| $0140-0191$ | C:FXD MICA 56 PF 51 | 28480 | 0140-0191 | 6 |
| 0140-0195 | C:FXD MICA 130 PF SI 300VDCw | 04062 | DM1sF131J 300V | 3 |
| 0140-0201 | C:FXD MICA 12 PF 51 | 28380 | 0140-0195 | 1 |
| 0160-0356 | C:FXD mica 18 PF 51 | 28480 | 0160-0336 | 2 |
| 0160-2101 | C: FXD MICA 27 PF 21 300VOCW | 72136 | RDM1 SE270G3C | 4 |
| 0160-2232 | C: PXD MICA 33 PF 21 300VDCW | 72136 | RDMISES30G3C | 6 |
| $0683-1035$ $0683-1045$ | R:FXD COMP 10k 10 HM $351 / 4 \mathrm{H}$ | 01121 | CB 1035 | 2 |
| $0683-1045$ $0633-1235$ | R: FXD Comp look oim Si 1/4W | 01121 | CB 1045 | 4 |
|  |  | 03121 | CB 1235 | 2 |
| 0683-1535 | R:FXD COMP 15k orm 58 1/4W | 01121 | С® 1535 | 3 |
| 0683-1835 | R:FXD Comp lek anm Si 1/4W | 01121 | св 1835 | 3 |
| 0683-2235 | R:FXD COMP 22K Orat si $1 / 4 \mathrm{~W}$ | 01121 | CB 2235 | s |
| 0683-2735 | R:FXD COMP 27 K ome $51 / 4 \mathrm{WW}$ | 01121 | CB 2735 | 3 |
| 0683-3025 | R:FXD Comp 3k orm Silitw | 01121 | CB 3025 | 7 |
| 0683-3035 | R:FXD Comp 30k orm si $1 / 4 \mathrm{~W}$ | 01121 | С® 3035 | 2 |
| 0683-3935 | R:FXD Cown 39k orm Si $1 / 4 \mathrm{~W}$ | 01121 | CB 3935 | 3 |
| 0683-3945 | R:PXD COMP 390K OHm Si $1 / 4 \mathrm{~W}$ | 01121 | CB 3945 | 4 |
| 0683-4735 | R:FXD Comp 47 K orm $581 / 4 \mathrm{~W}$ | 01121 | CB 4735 | 1 |
| 0683-5635 | R:FXD COMP S6K otm St $1 / 4 \mathrm{~W}$ | 01121 | св 5635 | 33 |
| $0683-6825$ $0683-6835$ | R:FXD COMP 6.8K OHM 5S $1 / 4 \mathrm{~W}$ R:FXD COMP 6ek otm 5s $1 / 4 \%$ | 01121 | $\begin{array}{ll}\mathrm{CB} & 6825 \\ C B 6835\end{array}$ | 1 |
| 06856-4735 |  | (01121 | C8 6835 | $?$ |
| 0686-5625 | R:FXD COMP 5.6 K Otem $5 \mathrm{Si} 1 / 2 \mathrm{~W}$ | 01121 | EB S625 | 9 |
| 0689-2725 | R:FXD comp 2.7K Otm St ik | 01121 | C8 2725 | 1 |
| 0757-0947 | R:PXD FLM 9.1K OMM $251 / 8 \mathrm{~W}$ | 28480 | 0757-0947 |  |
| 0757-0949 | R:FXD FLM 11K OTM $2121 / 8 \mathrm{H}$ | 28480 | 0757-0943 | 1 |
| 0757-0958 | R:FXD FLM 27 K OtM $231 / \mathrm{BW}$ | 28480 | 0757-0947 | 1 |
| 1853-0008 | TRANSISTOR:SILICON PNP | 01295 | 2N3250 | 3 |
| 1901-0025 | DIODE:SILICON 100mA Loov | 284801 | 1901-0025 | 8 |
| 1901-0081 | DIODE:SILICON SOVOCW | 28480 | 1901-0081 | 13 |
| 1901-0143 | DIODE:SILICON | 28480 | 1901-0143 | 8 |
| 1970-0009 | ELEETRON TUBE: INDICATOR 10 DIGIT | 83594 | 05991 | 1 |
| 5060-5647 | IMHa Reversible decade counter | 04404 | 5060-5647 | 1 |
| 5060-5700 | IMHz GATE ASSEmbly | 04404 | 5060-5700 | 1 |
| 5080-0615 | TRANSISTOR:MATCHED PAIR | 04404 | 3080-0615 | 8 |
|  | OPtion zewz |  |  |  |
| 0140-0014 | C: FXD MICA 56 Pr 101 | 00853 | reitilsesbok | 4 |
| 0140-0191 | C:FPD MICA S6 PF St | 28480 | 0140-0191 | 1 |
| $0140-0194$ $0140-0195$ | C:FXD MICA 110 PF Si | 28480 | 0140-0194 | 40 |
| 01400195 $0140-0201$ | C:FXD MICA 130 PF St 300 VDCW | 04062 28480 | 0115F131.1300V | 41 |
|  |  |  |  |  |
| 01400219 | C:FXD MICA 180 PF 21 | 28480 | 0140-0219 | s |
| 0150-0121 | C:FXD CER 0.1 UF +30-201 SOVDCW | 56283 | SCSOB15-CML | 1 |
| 0160-0356 | c: FRD MICA 18 PF Si | 28480 | 0160-0356 | 2 |
| $0160-2101$ $0160-2232$ | C:FXD MICA 27 PF 21 300VDCW | 12136 | rdmi Se 2 Jors 3 C | 1 |
| 0160-2232 | C:FXD MICA 33 PF 2l 300 VDCW | 12136 | RDHISE33063C | 8 |
| 0683-1035 | R:FXD COMP 10K OHM ST $1 / 4 \mathrm{~W}$ | 01121 | CB 1035 | , |
| 0683-1045 | R:FXD COMP lonk orm se $1 / 4 \mathrm{~W}$ | 01121 | CB 10345 |  |
| 0683-1335 | R:FXD COMP 13 K OHM $51 / 1 / 4 \mathrm{H}$ | 01121 | CB 1335 | , |
| 068341535 | R:FXD COMP 15K OHM 53 1/4W | 01121 |  | 11 |
| n693-1835 | R:FXD COMP 18K OHM 5\% $1 / 4 \mathrm{~W}$ | 01121 | CB 1985 | $1 \cdot$ |


|  | 1e 29-2. Replaceable Parts (Cont'd) |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| © Part No. | Decertpition \# | Mfr. | Mfr. Part No. | TQ |
|  | OPTIOW 20/21 (CONT'D) |  |  |  |
| 0683-2035 | R:FXD COMP 20K OHM $581 / 4 \mathrm{~W}$ | 01121 | CB 2035 |  |
| 0683-2045 | R:FXD COMP 200K OHM $581 / 4 \mathrm{~W}$ | 01121 | CB 2045 | 6 |
| 0683-2235 | R:FXD COMP 22K OHM 58 $1 / 4 \mathrm{~W}$ | 01121 | CB 2235 | 79 |
| 0683-2435 | R:FXD COMP 24K OHM 5i $1 / 4 \mathrm{~W}$ | 01121 | CB 2435 | 1 |
| 0683-2735 | R:FXD COMP 27K OHM 58 $1 / 4 \mathrm{~W}$ | 01121 | CB 2735 | 40 |
| $0683-3025$ $0683-3335$ | R:FXD COMP 3 K OHM 58 \% $1 / 4 \mathrm{~W}$ | 01121 | CB 3025 | 37 |
| 0683-3335 | R:FXD COMP 33 KK OMM 58 $1 / 4 \mathrm{~W}$ | 01121 | CB 3335 |  |
| $0683-3935$ $0683-3945$ |  | 01121 | CB 3935 | 2 2 2 |
| n683-4715 |  | 01121 01121 | CB 3945 <br> CB | 24 2 |
| 0683-4725 | R:Fxo comp 4.7K orm 58 1/4N | 01121 | CB 4725 | 1. |
| 2683-4735 | R:FXD COMP 47 K OHM $581 / 4 \mathrm{~W}$ | 01121 | CB 4735 | $2{ }^{\text {a }}$ |
| 0683-5625 | R:FXD COMP 5.6 K OHM $581 / 4 \mathrm{~W}$ | 01121 | CB 5625 | 44 |
| 0683-5635 | R:FXD COMP 56K OHM 58 1/4W | 01121 | СВ 5635 | 73 |
| n683-6825 | R:FXD COMP 6.8K OHM 58 $1 / 4 \mathrm{~W}$ | 01121 | CB 6825 | 1 |
| n683-6835 |  | 01121 | CB 6835 $C B 8225$ | 37 |
| n683-8225 n683-9135 |  | (01121 | C8 88225 <br> CB <br> 135 | 1 |
| 7683-4735 | R:FXD COMP 47 K OHM $581 / 2 \mathrm{~W}$ | 01121 | EB 4735 | 6 |
| 0686-5625 | R:FXD COMP 5.6 K OHM $581 / 2 \mathrm{~W}$ | 01121 | EB 5625 | 9 |
| 0689-2725 $0757-0944$ |  | 01121 28480 | GB 2725 $0757-0944$ | 1 |
| 0757-0946 | R:FXD FLM 8. 2 K OHM $281 / 8 \mathrm{~W}$ | 28480 | 0757-0946 | 1 |
| 0757-0947 | R:FXD FLM 9.1K OHM $281 / 8 \mathrm{H}$ | 28480 | 0757-9747 | 1 |
| 0757-0949 | R:FXD FLM lik OHM 28 1/8W | 28480 | 0757-0949 | 1 |
| 0757-0950 | R:FXD FLM 8. 2 K OHM $281 / 8 \mathrm{~W}$ | 28480 | 0757-0950 | 1 |
| 0757-0958 | R:FXD FLM 27 K OHM 28 1/8W | 28480 | 0757-0958 | 1 |
| $1251-0135$ $1850-0111$ | CONNECTOR:BODY 15 PIN | 28480 01295 | 1251-01.35 | 6 |
| 1850-0184 | TRANSISTOR:GERMANIUM PNP | 02735 | 38339 | 40 |
| 1853-0008 | TRANSISTOR:SILICON PNP | 01295 | 2N3250 | 11 |
| 1901-0025 | DIODE:SILICON IOOMA 100 V | 28480 | 1901-0025 | 48 |
| 19n1-0081 | DIODE:SILICON 50VOCW | 28480 | 1901-0081 | 79 |
| 1901-0143 | DIODE:SILICON | 28480 | 1901-0143 | 8 |
| 1910-0016 | DIODE:GERMANIUM 100MA AT 0.85 V 60PIV | 28480 | 1910-0016 | 2 |
| $1970-0009$ $5060-5066$ | ELECTRON TUBE: INDICATOR 10 digit REVERSIBLE DECADE COUNTER | 83594 04404 | $\begin{aligned} & \text { B5991 } \\ & 5060-5066 \end{aligned}$ | 6 5 |
| 5n60-5611 | PRINTER LOGIC | 04404 | 5060-5611 |  |
| 5n6n-5645 | Imha reversible decade counter | 04404 | 5060-5645 | 1 |
| 5n6n-570n | IMHZ GATE ASSEMbLY | 04404 | 5060-5700 | 1 |
| 5080-6555 | network: diode resistor | 04404 | 5080-6555 | 1 |
|  | OPTION 29/30 |  | : |  |
| 014n-0014 | C: FXD MICA 56PF 103 | 00853 | RCM15E560K |  |
| $\begin{aligned} & 0140-0191 \\ & 0140-0194 \end{aligned}$ | C:FXD MICA 56PF 53 | 28480 | 0140-0191 | 1 |
| 0140-0195 | C:FXD MICA 130PF 5 5? 300VOCW | 28480 04062 | 0140-0194 | 40 |
| 0140-0219 | C:FXD MICA 180PF 23 | 28480 | -140-0219 | 46 |
|  |  |  |  |  |




Stock No. 05232-6007 (Serial Prefix 637 and below)

## (A26) Inpat Amplifier for Option 29



Stock No. 05232-6006 (Serial Prefix 637 and below)
(A27) Trigger for Option 29



## Stock No. 5060-5700

(A38) 1 Megaherty Gate for Option 29


Figure 29-2. 1 Megaherty Gate (A38) for Option 29




8tock No. 5060-5647
(A11) Revers Ible $1 \mathrm{MHz}+4-2$-2-1 Decade Counter for Option 29


- (1)
, 分. chassis chouno
uniess ot menemise morcatio






Stock No. 5060-5046
(A11) Reversible 1MHz 8-4-2-1 Decade Counter for Option 29/21 or 29/35



Figure 29-5. - Wottom Internal View of HP 2401C-20


## MANUAL SUPPLEMENT

MODIL HP-2401C Integrating Digifal Volimeter<br>Option 30

### 30.1 GENERAL DESCRIPTION

The HP-2401C-30 Integrating Digital Voltmeter incorporates logic for perlod measurement in addition to all capabilities of the standard instrument. The six-digit display of the HP-2401C-30 provides direct readout of period, in milliseconds, with the decimal point properly placed. Period measurement specifications of Option 30 are presented in Section 1.7 of this manual.

### 30.2 INSTALLATION AND. OPERATION

Install, operate, and program the HP-2401C-30 as specified in Section II of this manual.

### 30.3 THEORY OF OPERATION

Period is measured by reversing the signal routing used when measuring frequency. In the $\mathrm{HP}-2401 \mathrm{C}-30$ this reversal is accomplished by period logic assembly A40 when the FUNCTION switch, S2, is set to PERIOD position, or when period measurement is programmed with the FUNCTION switch set to EXT SEL position. (See Figures 30-1 and 30-2.)

### 30.3.1 Frequency Measurement

When the FUNCTION switch is set to FREQ position, the false state (near - 15 volts) of the period input logic line to pin 5 of A40 enables AND transistors Q5 and Q8. Through logic amplifiers Q1 and Q2 this establishes the frequency measurement connections whereby cycles of an unknown signal are counted by decade counters A11-A15 and A46 for a known sample period, which is derived by decade dividers A1-A5 from the 100 kHz time base outpat of A6.

### 30.3.2 Period Measurement

When the FUNCTION switch is set to PERIOD position, the true state (near ground) of the period input logic line enables A40 AND transistors Q6 and Q7 through logic amplifier Q1. This switches the known 10 kHz output from decade divider A1 to the decade counters and switches the unknown signal to the circuits that start and stop the gate period. The number of 100 kHz pulses ( 100 microsecond intervals) counted during the gate period yields a measurement of the period's duration. The decimal point is placed so that the measurement is direct reading in milliseconds.
The selection of SAMPLE PERIOD determines whether the unknown signal is divided by 1,10 , or 100 . Division of the unknown signal improves the resolution of measurement because the number of counts of the known signal is multiplied by 10 or 100 . The averaging of 10 periods in this manner yields 10 mi crosecond resolution. Averaging of 100 periods gives 1 microsecond resolution.

### 30.3.3. Ofher Functions

The remainder of the period logic on A40 controls display lamps of units indicator assembly A24 and the frequency logic line input to printer coupling logic assembly A22. The selection of either PERIOD or FREQ measurement FUNCTION applies a true state to the FREQ logic lines, assuring that frequency count AND transistor A19Q11 of counter input logic assembly A19 is - opened.

### 30.3.4 Volf Measurement

Selection of VOLT measurement FUNCTION has the same effect upon the A40 circuits as the selection of FREQ except that the FREQ logic line is left false. The time base is derived for voltage measurements, but frequency count AND transistor A19Q11 is inhibited and voltage count AND transistor A19Q10 is enabled.

### 30.4 MAINTENANCE

Except as specified in the following paragraphs, service the HP-2401C-30 per the instructions in Section IV of this manual.

### 30.4.1 In-Cabinef Performance Checks

The In-Cabinet Performance Checks for the HP-2401 C-30 are specified in Table 30-1. Apy notations to check 30.1, etc. refer to that table only.

### 30.4.2 Location of $\dot{A} 4$ and Components

Figure 30-2 shows the parts location on A40 and Figure 30-3 shows the location of A40 in the HP-2401C-30.

### 30.4.3 Troubleshooting

Trouble in period logic assembly A40 can prevent counting by the decades when any FUNCTION is selected. (See Figures $30-1$ and $30-2$.) Figure 30-4 shows connections of the HP-2401C-30 where these differ from those of the standard HP-2401C. The other components involved in period measurement are checked adequately by following the troubleshooting instructions in Section 4.4 of this manual.
1.

Table 30-1. In-Cabinet Performance Checke (Sheet 1 of 2)
Perform checks 1 through 24 as specified in Table 4-3 of this manual per instructions in Section 4.2.

## "30.1 PERIOD MEASUREMENT RANGES

1, 10 , and 100 periods, $5 \mathrm{~Hz}(200 \mathrm{~ms})$ to $10 \mathrm{kHz}(1 \mathrm{~ms})$ - sine wave input*.
a. Set HP-2401C-30 Power switch to ON, other controls as follows:

| FUNCTION: | PERIOD. |
| :--- | :--- |
| SAMPLE PERIOD: | .01.SEC. |
| SAMPLING RATE: | Fully clockwise. |
| ATTENUATION: | Fully clockwise. |
| 100 KC STD (rear panel): | INT. |

b. Connect output of portable oscillator to HP-2401C-30 FREQ INPUT and to input of oscilloscope with a BNC 'T" connector. Set oscillator to provide $5 \mathrm{~Hz} 0.28 \mathrm{v} \mathrm{p}-\mathrm{p}$ output.
c. Check and record reading on the HP-2401C-30, which should be approximately
d. Set oscillator for reading of exactly 200.0 MILLISEC on the HP-2401C-30. Set SAMPLE PERIOD switch to 11 SEC position and check and record reading, which should be $200.00 \pm$ the setting error in the last ( $10 \mu \mathrm{~s}$ ) digit.
e. Set oscillator for reading of exactly 200.00 MILLISEC on the HP-2401C. Set SAMPLING PERIOD switch to 1 SEC position and check and record reading, which should be 200.000 MILLISEC $\pm$ the setting error in the last ( $1 \mu \mathrm{~s}$ ) digit.
30.2 PERIOD MEASÚURMENT ACCURACY *
$\pm 1$ count $\pm$ time base accuracy $\pm$ trigger error number of periods averaged
a. Turn on frequency standard and connect its SELECTED FREQ OUTPUT to the HP-2401C-30 FREQ INPUT and oscilloscope as indicated below. Select 10 Hz output.

b. Set HP-2401C-30 Power switch to ON, other controls as follows:

```
FUNCTION:
SAMPLE PERIOD:
PERIOD.
.01 SEC.
Fully clockwise.
Fully clockwise.
INT.
ATTENUATION:
100 KC STD (rear panel):
```


## -

c. After required warmup of frequency standard, set $500 \Omega$ potentiometer for maximum p-p amplitude of signal to HPL2401C-30 FREQ INPUT. Then record period measurement displayed. This should be within the range of $100 \pm 0.1$ MILLISEC.

[^1]Table 30-1. In-Cabinet Performance Check (Sheet 2 of 2 )
30.2 d. Slowly reduce signal amplitude tapped from the $500 \Omega$ potentiometer to the point where individual period measurement readouts on the HP-2401C-30 are as low as 00099.6 or as high as 00100.4 MILLISEC. Determine and record p-p amplitude of signal to FREQ INPUT of the HP-2401C-30. Amplitude should be no greater than 0.28 v p-p ( 0.1 v rms ).
e. Set SAMPLE PERIOD switch to . 1 SEC and record the most erroneous period measurement of the next ten. No readout should be lower than 0099.96 MILLISEC or higher than 0100.04 MILLISEC.
f. Repeat step e, above, at 1 SEC SAMPLE PERIOD. No readout should be lower than 099.996 MILLISEC or higher than 100.004 MyLLISEC.
30.3 EXTERNAL PROGRAMMING - PERIOD FUNCTION

Period measurement is a programmable function of the HP-2401C-30; the requirements of check 20, Table 4-3, apply.
a. Prepare for period measurement as specified in check 30.1 , except set the FUNCTION switch to EXT SEL.
b. Record lighted HP-2401C-30 units display, which should be VOLTS.
c. Connect a jumper between pins Z and f of J 1 and record lighted HP-2401C-30 units display, which should be MILLISEC.

### 30.5 PARTS LIST

The Parts List in Section V of this manual applies to the HP 2401C-30 except as indicated in Tables 30-2 and 30-3.

HP-2401C
$\qquad$ - $\qquad$ DATE $\qquad$

|  | DESCRIPTION | CHECK RESULTS |
| :---: | :---: | :---: |
| 30.1 | PERIOD MEASUREMENT RANGES | , |
|  | Period |  |
|  | 1 | $\int \mathrm{ms}$ |
|  |  | (Approx. 200.0 ms ) |
|  | 10 | $\square \mathrm{ms}$ |
|  |  | (200.0? ms) |
|  | 100 | $\square \mathrm{ms}$ |
|  |  | (200.00? ms) |
| 30.2 | PERIOD MEASUREMENT ACCURACY |  |
|  | 1 period reading, maximum amplitude input | $\longrightarrow \mathrm{ms}$ |
|  |  | $(100.0 \pm 0.1 \mathrm{~ms})$ |
|  | Input voltage producing specified trigger error | $\longrightarrow v \mathrm{p}-\mathrm{p}$ |
|  |  | (0.28v p-p, max.) |
|  | 10 period reading with apecified trigger error | $\int \mathrm{ms}$ |
|  |  | $(100.00 \pm 0.04 \mathrm{~ms})$ |
|  | 100 period reading with speclfied trigger error | $\square$ ms $(100.000 \pm 0.004 \mathrm{~ms})$ |
| 30.3 | EXTERNAL PROGRAMMING - PERIOD FUNCTION |  |
|  | Program | - |
|  | Function <br> Volts |  |
|  |  | (VOLTS) |
|  | J1-Z to 1 Period | (MILLISEC) |

Table 30-2. Reference Designation'Index


Table 30-2. Referencie Designation Index (Cont'd)





Stök No. 5060-2506 (Serlal Profix 501 thru 605)


Stock No. 5060-5870 (Serial Prefix 010 and above)
(A40) Period Logic for Option 30


Figure 30-2. Period Logic (A40) for Option 30


Figure 30-3. Bottom Internal View of HP 2401C - $\mathbf{3 0}$


-     - $-\cdots$


Figure 30-4. Interconnections for Option 30

Section 30


Figure 30-4. Interconnections for Option 30 (Sheet 2 of 2)

# MANUAL SUPPLEMENT 

## MODAR HP-2401C <br> Infegrating Dighal Velimoter

Option 31

### 31.1 ORNERAL DESCRIPTION

The HP-2401C-31 Integrating Digital Voltmeter incorporates automatic 8 e lection of the appropriate input voltage range in addition to all capabilities of the standard instrument. The autoranging circuitry utilizes the full overrange capability of the standard HP-2401C, upranging at $310 \%$ of full scale. It downranges at $30 \%$ of full scale.
Operation of the autoranger is rapid - only $\mathbf{6} \mathrm{ms}$ per range change. 'The autoranger proceeds automatically in the correct direction. Thus even if the appropriate range for a new input signal is at the opposite extreme from that required for the previous reading, the measurement usually commences in 34 mis. (This includes the normal encode delay of 9.7 ms when the correct range is reached.) However, if the autoranger has downranged from 1000 V to 1 V range, notse may force one or two uprangings, resulting in as much. as 50 ms delay before the sample period begins. The HP-2401C-31 can therefore be used at high sampling rates with varying input signals, and permits rapid scanning rates when employed in multi-channel systems with widely varying signal levels. However, the maximum sampling rate is limited by the sample period and the time required to reach the correct range.
When used with a HP-2411A Guarded Data Amplifier, the HP-2401C-31 automatically selects the appropriate amplifier gain. It thereby provides six automatically selected ranges from 10 mV to 1000 v full scale.
The HP-2401C-31 also provides range selection commands for a HP-2410B AC/Ohms Converter. (HP-2410B-17 for AC/Ohms Converters with serial prefixes earlier than 514-.) However, autoranging ac voltage measurement extends only to the $1 v$ range; ac voltage measurements on the 0.1 v range must be selected manually or by specific programming. The autorange logic is such that the record command outputs from the instrument are not necesarily identical to the counter gate time.

### 31.2 INSTALLATION AND OPERATION

For dc voltage measurement, install, operate, and program the HP-2401C31 as specified in Section II of this manual. The following paragraphs briefly describe how to set controls for autoraning ac and resistance measurements using the HP-2410B AC/Ohms Converter and measurements down to 10 millivolts full scale using the HP-2411A Guarded Data Amplifier. Also briefly discussed is the autoranger's response to various situations during the operating cycle of the HP-2401C-31.

### 31.2.1 Autoranging wish MP-24108

For autoranging resistance or ac voltage measurements using a HP-2410B AC/Ohms Converter with a HP-2401C-31, set controls exactly as specified in Section 2.5.3, except for the BP-2410B RANGE awitch. Instead of setting the HP-2410B RANGE awitch to a specific range, set it to AUTO position. This programs autoranging operation of the HP-2401C-31 regardless of the HP2410B FUNCTION selected and autoranging resistance or voltage measurements will be automatically completed on the range that yields the best resolution and accuracy.

The logic in the HP-2401C-31 cannot select the 0.1 iv measurement range $\alpha$ the HP-2410B. Ac voltage measurements on the $0.1 v$ ac range must be aclected manual ly by means of the HP-2410B RANGE pwitch or by epecific programming.

### 31.2.2 Auforanging with HP-2411A

For autoranging dc valtage measurement down to 10 millivolts ( 0.01 v ) full scale ( 30 millivolts overrange), using the HP-2411A Guaided Data Amplifier with the HP-2401C-31, eot controls exactly as epecified in Section 2.5. $\frac{1}{2}$ except for the HP-2401C-31 FUNCTION aritch and the HP-2411A MODE selector. Instead of eetting the HP-2401C-31 FUNCTION switch to EXT SEL, set it to AUTO RANGE positicn; use EXT SEL poaition opy if autoranging measurements with the HP-2411A are to be programmed externally. Instead of eetting the HP-2411A MODE selector to the desired mode, eat it to EXT SEL.
31.2.3 Respense Characteristics of the MP-2401C-31

## Upranging

The HP-2401C-31 always responds to an input that exceeds $310 \%$ of full scale by upranging. During the deplay pariod, the autoranger switches directly to 1000 V range; this is easentially the same as the response of the etandard HP-2401C to an overload input, but the OVERLOAD indicator does not light when AUTO RANGE function is selected. Following the encode command, the HP-2401C-31 upranges one range at a time instead of aldpping to the 100 of range.

## Downranging

The HP-2401C-31, responds to an input that is less than $30 \%$ of full scale only during the encode delay interval that follow the encode pulse and pre only during the encode d

## Deadgn Objectures

These reaponse characteristics are designed to achieve the following:
a. Madmum protection of the instrument from overloading.
b. Minimum delay between the encode command and the etart of a valid meacurement.

### 31.3 TMEORY OF OPREATION

### 31.3.1. General

During autorange operation of the HP-240IC-31 the autorange logic melecta the appropriat voltage range in responce to dover and under range inpat eignils from Auto Range Rate Detector A10. The eclection of range and
+1 or +10 gain are routed through PROGRAM CONTROL receptacle J1 to the HP-2410B or the HP-2411A, controlling their operation as well when either is used with the HP-2401G-31.
As shown in Figurd 31-5, Auto Range Rate Detector A10 consists of two frequency-to-voltage converters (fvc's) and high and low rate level detec--torm. The high and low rate outputs from A10 are applied to the Range Gates on Ascembly A44, as indicated in Figure 31-6. During the encode delay period, low or high rate pulses are passed to the count one-shot on Range Coritrol Assembly A45. This one-shot prochices a delayed trigger for the Range Counter on Ascombly Ass. The range counter counts up or down, depending upon the logic line imput that it receives from the up/down flipflop on A45. The range counters count down in response to low rate pulses because the down etate of the up/down flip-flop is 'not changed. High rate pulces trigger the up/down ilip-1lop to up etate, so that the range counters count up in reeponse to high rate pulces. The tates of the range counter binaries are decoded and amplifted to program range aelection Down count program progreasively lower ranges and up counts program progressively higher ranges. The details of the autorange logic are discussed in the dehigher ranges. The details of the autoran
scriptions that etart with Section 31.3 .3 .

### 31.3.2 Autorange Refe Defector A10 (Figure 31-7)

NOTE
Unless otherwise stated, incomplete designations (C7, A1, T1, CR4, etc.) which appear in the following discussions (Sections 31.3.2 through 31.3.5) identify components of the circuit assembly (A10, A43, A44, or A45) being described.

The auto range rate detector examines the combined channel pulse train output of the voltmeter vfc to determine if the pulse rate (input voltage) 1s low or high. If the vic output is less than 30 kHz (1.e., the input sig nal is less than $30 \%$ a full acale), the low rate detector produces an output. When the ofc output is 310 kHz or greater (i.e., the input signal is at least $310 \%$ of full scale), the high rate detector produces an output. Between these extremes, no output is produced by either detector.

The output from either detector is essentially the same, a train opositivegoing $2 \mu \mathrm{~s}$ pulses at 5.5 ms intervals. (The quoted duration and apacing are approdimate.) The auto range rate detector also provides an overload reset pulce for the HP-2411A Guarded Data Amplifier.

Hish Rate Detector
As ahown in Figure 31-7, the vic pulses are received at pin 1 , A A10 and coupled to the high rate detector via C7. The high rate detector output from the collector $\alpha$ Q1 is produced anly when current can flow through the number 2 winding a T1. The switching of current flow between the number 1 and 2 windings of T1 is determined by the voltage levels at the cathodes of CR3 and CR4.

The voltage at the cathode of CR4, set by potentiometer R3, determines the high rate detector switchover point. The voltage at the cathode of CR3 is
determined by the frequency of the pulse input to pin 1 and the forward voltage
drop across CR18. The puises that are coupled through C7 and CR2 charge C2 drop across CR18. The puises that are coupled through C7 and CR2 charge C2 age across $\mathbf{C 2}$ increases for low input frequencles and decreases for high input frequencies.
With input pulse frequencles below 310 kHz , the voltage across C 2 is such, that the cathode ot CR3 is slightly more negative than the cathode of CR4. (Under these conditions the voltage difference is, essentially determined by a forward drop across CR18. Y CR4 is cut off, closing the path for regenerative feedback between collector and base $\alpha$ Q1, which is a blocking oscillator.
When the input pulse frequency reaches 310 kHz , the voltage across C 2 reaches a level where the cathode of CR3 becomes more positive than the cathode of CR4. This cuts off CR3 and enables conquction through CR4, opening the re-

At this point, when current is switched from $T 1$ winding no. 1 to no. 2 , thermal noise valtage developed across R5 is amplified and inverted by Q1 and coupled back to winding no. 2. The feedback, now in phase, quickly saturates the Current through 0 , generating a posittve-going pulse at the callector o Q1 ates and no longer provides the couping action, disconnecting the regenerauve path. Conduction through Q1 then decreases, returning to the unsaturated condition in approximately $2 \mu \mathrm{~s}$. After a time delay that is essentially determined by the time constant of R5 and C3, the comparison circult is ready to cycle again. This action continues as long as the overload remains, producing a train of positive-going pilses from the collector of Q1.

## Low Rate Detector

- The opergtion of the low rate detector is similar to that $\alpha$ the high rate detector, except that the actuon is reversed. At thput pulse above 30 kHz the valtage developed across CR19 keeps the CR10 cathode more positlve than the CR9 cathode. Below 30 kHz the C10 valtage falls to the point at which the CR10 cathode is more negative than the CR9 cathode, connecting regeneration that drives $Q_{2}$ to saturation. The interval between positive pulses from the low rate output is determined by the time constant of R13 and C11.

Delay Between Rate Detector Pulses
R5 and R13 are factory selected to provide approximately 5.5 ms between rate detector output pulses. This delay allows time for a range change before the next high/1ow rate detector cutput pulse is generated. However, this does not delay the first high or low rate pulse, which is generated within 2 few hundred microseconds after the input frequency reaches 310 or 30 Khz. This is possible because C2 and C10 are partially charged by CR18

HP-2411A Reset Output
The reset pulse for the HP-2411A is generated by inverting amplifier Q3, which ampifies the internal reset pulse from the reset bus.

### 31.3.5 Range Gate A44 (Figures 31-6 and 31-9)

The logic on Range Gate Assembly A44 determines the response of the autoranger to pulses from A10. The low and high rate range gates are AND transistors Q1 and Q2. These gates are inhibited by any of several positive true in-
puts that may be applied through OR gates $\mathrm{CR} 3-\mathrm{CR8}$

Display Period Logic
During the display period, Q1 and Q2 are inhibited (cut off) by the positive true state of the display holdoff signal from A18. This same state opens overload AND gate C5-R13 through logic amplifier Q3 and OR diode CR15. High rate pulses from A10 can then trigger flip-flop A45Q9-Q10 to overload state through over by the range gates during the display period, switches the attenuator dirmectly to 1000 y range, protecting the instrum ent from overload ERLOAD Andicator is inhiblted through OR diode A1OCR16 by the positive true state of the autorange logic line when AUTO RANGE FUNCTION is selected.

Logic When AU'TO RANGE Is Not Selected
The non-selection of AUTO RANGE function has the same effect upon operation of the range gates as the true state of the holdoff input from A18. In this inQ7 from the false state of the autorange logic line. Also, if the FUNCTION switch is not set to AUTO RANGE position, the OVERLOAD indicator is ight by the overload state of filp-flop A45 $29-Q 10$. The overioad state of A45Q9-Q10 cuts off A10Q4 through OR diode A10CR15 so that the OVERLOAD indicator is not lighted when there is no overload.

Encode Delay Period Logic
After the reset (encode) pulse, AND transistors Q1 and Q2 are no longer inhibited by the holdoff input from A18, which is false. But Q1 and Q2 A23 during resistance or ac voltage measurements with the HP- 2410 B .

The encode delay starts at the end of the ac/ohms delay gate, or immedrately if resistance or ac voltage measurements are not being made. During this period, low rate pulses from A10 are gated through AND transistor Q1 while count flip-flop A45Q13-Q14 is in count down state.This continues untll a high rate pulse is generated, the correct range is reached, or the next sample period starts.
A45Q13-Q14 is initially set to count dome state by the reset pulse that starts the encode delay period. Any high rate pulse from AND transistor $\mathbf{Q 2}$ triggers A45Q13-Q14 to count up state, which inhibits low rate pulses from AND ransistor Q1. This prevents upranging in response to low rate pulses. Thereafter, high rate pulses from A10 are gated through $\mathbf{Q} 2$ until the correct range is reached,

Low or high rate pulses are coupled to count one-shot A45Q5-Q7 through OR gate CR1-CR2. The remaining logic on assembly A44 derives the lowest and gate CR1-CR2. The remaining logic on assembly A44 derives the lowest and
highest range signals that inhibit AND transistor Q1 or Q2 when the autoranger is at elther end of its response range.

Sample Poriod Logtc
During the aample period, the poaltive-true atate of the rocord command line from A17 inhlbita low rato AND transistor Q1 through OR diode CR4 This logic arrangoment allowa ouly uprangting during the sample perlod.

### 31.3.4 Range Coniral A4S (FIgures 31-6 and 31-10)

- The logic on Range Control Asambly A40 stores the control staten of the autoranging ayatom, except for the range control states. The princlpal control memorien are up/down flip-flop Q1s-Q14 and overload flip-flop Q0-Q10. Also on thie board are the count one-shot and the record flip-flop.
Up/Down Contral Filpw Flon
- FMp-flop Q1S-Q14 is presot to count down atate, by oach encode pulse from A7 or A18. This atato places the count down end count up lines near ground and negative Sov, reapectivoly. Thereafter, a high rato pulee from © A4Q2 down and count up linen. The contral atates from thile flip-flop determine whether the autoranger switches to lower or higher ranges in reaponse to the pulces that are phesed by the range gatos on A44.


## Overlond Flip-FIop

Flip-llop CO O10
Fup-flop CO-Q10 14 preaet to overload atpte by each encode pulae. It remains in this atate (Q9 on, Q10 cut off) untly a high rate pulse from AND gate A4AC5-R13 triggers it to overlond atate. This can occur only during the dieplay interval or when the FUNCTION awitch is not mot to AUTO or Q11, pwitching the input altenuator to 1000 v range. When logic invert logic line la falee, the faleo etate from CO aleo IIghts. the OVERLOAD in dicator on A24, through logic inverter A1004. If C9-010 OV in arcator on A21, through logic invertor A10G. II Q9-Q10 is in overload countera, setting them to the etates that keep the attenuator ewitched to tooov range: Theroafter the autoranger is switched to lower ranges if the 1000 y range is too high.

Count One-Ehot
Count one-ahot Qb-Cl delaya range triggers that are applied to the range counter. Each range pulee from A44 triggera the one-shot to ita unatable
, cotate. The positive-golng tralling edge of the one-ahot output from the Ch collector triggers the range counter at the one ahot returns to its atable atato. The delay allowe time for a revereal of up/down logic atate to metlector of ©S is applied to the reset bues. Each poaitive pulse from the col-

## Record Flip-Figp

Record aip-flop QS-Q4 provides + and-record commande that algnal an external recorder or data proceasing dovice that data is ready to be recordod or usod. This slip-flop is triggered to record etate (QS cut off and $\alpha$ on) at the ond $\alpha$ the eample period by the poaltive-golng tralling odge of the trecord command aignal from A17. Each count pulee from
the count one-chot triggers the ilip-flop to record mtate. Thic logic proventa lacuance of a record command when a aample period is not completod becauce of upranging. A record command la leaued only 18 the recotting of A17Q1-Gi is not blanked by a negative phise from ar al the count onethot. The outpute from the record Mp-riop are coupled to the record command outpute via emitter followers Q1 and Q4.
31.3.5 Range Counter A43 (Fijures 31-6 and 31-9)

Flip-ilapa 1 through 9 and rolated diode AND gatei make up a three-etage revorulble countor. with a digtal range from 0 through 7 , of which only 0 throigh 0 is used. Filp-ilopi 1 through 3 are identified A, B, and C in flop outmutia, conduction through an even-numbered tranetetor ( OH as OS ) flop outputa, conduction through an even-numbered tranadetor ( $\mathrm{CD}, \mathrm{QA}$, © $)$ repredtente 0 . Throuch an odd-numbered tranaletor (Q1, QS, Q3) conduc the counter 10, oummarized in Table's1-1.

Table 31-1. Range "Counter A4safummary


* To HP-2411A Guarded Data Amplifier
** To HP-2410B AC/Ohms Converter.

Up/Down Counting
During up counting, triggers are coupled from the collectors of odd-numbered tranalitors to aucceeding atages. Down counting is inhibited by the poaltive true etate $\alpha$ the count up line, which is applied to the cathodes of AND diodes CR29 and CR3S through R29 and R36. Down counting occurs when up counting is inhibited by the poaitive true atate of the count down

## Coupling al Countior Outpute

Coupling of the range selected by the range counter to external circuite is anabled by the true atate $\alpha$ the autorange logic line through logic inverter a. The inverted auput irom this line also serves as one of the inputs to HP-2410B control AND trandetor Q15.

## Control of the HP-2410B

## AND transiator Q15 is enabled if:

a. The SAMPLING RATE control is in STOP position (used when the HP-2401C-31 is operated as part of a data acquisition system).
b. Autorange is programmed.
c. ACF or ACN is programmed.
d. A sample period is not in progress.

1
When each fample period ends, Q15 is enabled and the overload flip-flop Is set via OR gate CR44-CR45. The HP-2401C-31 is switched to the 1000 v range, and the HP-2410B. is set to the 1000 v range via J1, pin e, the overload signal output.
The encode pulse for the next measurement sets the Range Counter Ascembly, A43, to 1000 v and resets the overload flip-flop via A45CR11. This alows the HP-2401C-31 to witch to the 1v range (ac is programmed), and because the range counter is at 1000 v , the $\mathrm{HP}-2410 \mathrm{~B}$ remains on the 1000 v range. If this is not the proper range, downranging occure ae deacribed previously.
If the HP-2401C-31 is operated in the automatic re-cycle mode (SAMPLING RATE control not at the STOP position) or when ohms function is program med, Q15 is inhibited and operation is the same as for dc voltages.
31.4 MAINTENANCE

Except as specified in the following paragraphs, service the HP-2401C31 per the instructions in Section IV of this manual.

### 31.4.1 In-Cabinef Performance Checks

The in-cabinet performance checks for the HP-2401C-31 are specified in Table 31.2. The test setup is shown in Figure 31-1. Except where other wise specified, any notations to check 31.1, etc., refer to that table only.

### 31.4.2 Troubleshooting

Trouble in A10, A43, A44, or A45 can prevent autoranging. Trouble in ${ }^{*}$ A10, A44, or A45 can prevent normal overload protection of the HP-2401C11. (See Figures 31-4 through 31-6.) The other components involved in he operation of the HP-2401C-31 are checked adequately by following the roubleshooting instructions in Section 4.4 of this manual
The locations of assemblies A10 and A43 through A45 are indicated in Figures 31-2 and 31-3. Figure 31-3 also shows the approximate locations of CR201 through CR205. Figures 31-7 through 31-10 show the location of components on these assemblies and the assembly circuits. Figure 31-11 hows conriections to A17 and A18 for HP-2401C-31. Figure 31-12 shows interconnections of the HP-2401C-31.

### 31.4.3 Callbrefion of Refe Defoction

## Calibrate rate detection whenever the HP-2401C-31 uprange or downrange change point is incorrect. (See, performance check 31. 1. Table 31-2.) proceed as follows:

a. With FUNCTION switch set to VOLT, perform steps 1 through 5 of Section 4.7.3, but adjust A10R3 where adjustment of A10R2 is spec ified. (See Figure $31-2$ for location of rate detection adjustments.)
b. Set HP-2401C - $\mathbf{3 1}$ controls as follows:

| FUNCTION: | AUTORANGE. |
| :--- | :--- |
| SAMPLING RATE: | FULLYCLOCKWISE. |
| SAMPLE PERIOD: | .01 SEC. |

c. Set input voltage to $28.5 \%$ of any full scale range but the 0.1 V range. For example, set input voltage to 28.5 V . which is 28.5 N of the 100 V range:
d. Adjust A10R11 clockwise until the decimal jumps one place to the right on the digital display of the HP-2401C -31.
e. Verify correct calibration per performance check 31.1. Table 31-2.

### 31.5 PARTS LIST

The Parts List in Section V of this manual applies to the HP 2401C-31 except as indicated in Tables 31-3 and 31-4.

| 31.1 | autoranging - range change po Upranges at $310 \%$ of full scale. | ONTS <br> Downranges at $30 \%$ of full scale. |
| :---: | :---: | :---: |
|  | a. Set HP-2401C-31 Power switch FUNCTION: <br> RANGE: <br> SAMPLE PERIOD: <br> SAMPLE RATE: <br> 100 KC 8TD (Rear Panel): <br> STORE/DISPLAY (Rear Panel): | to ON, other controle as followe: AUTORANGE. <br> 1V. <br> 1 SEC. <br> Fully clockwise. <br> ENT. <br> DISPLAY. |

b. Connect the - and +OUTPUT terminale of the dc atandard to the HI and LO terminals $\alpha$ the 31. Jumper the GUARD terminal to the 20 terminal.
c. Turn on the dc atandard and eet it for 0.3V output. The HP-2401C-31 display readout abould approdmate -300.000 MILLVOLT8.
d. During manourement, while counting is vietble, alowly increase output from the de standard untll the decimal point on the 31 Jumpe one poaltion to the right. Record the next meagurement, which should be $-312.5 \pm 7.50$ MilLIVOLTS.
e. Siowly decreace output from the de atandard until the decimal point on the 31 jumps one poilton to the left. Record the next meacourement, which should be $-285 \pm 10.00$
MLLVOLTS.
31.2 EXTERNAL PROGRAMMING - AUTORANGE FUNCTION

Autoranging is a progirammable function of the HP2401C-31: the requiremente of
check 20, Table $4-3$ apply. check 20, Table 4-3 apply.
a. Repeat check 31.1, but with FUNCTION set to EXT $8 E L$ and pins $Z$ and $V$ of PROCRAM CONTROL receptacle J1 connected. The reault of this chock should be ident cal to those of 31.1. Record a yes on the test card if reculta are the same.
31.3 AUTORANGING - RANGE EELECT TME 6 milliseconds, madmum, for each range change; 34 milliseconde, madmum, from encode command to etart of meacurement.
a. Make connections illuatrated in Figure 31-1; set DC Standard for 800 output.
b. With the HP-2401C-31 on and operating, set controls as followe:

## FUNCTION:

AUTORANGE.
RANGE:
8AMPLE PERIOD: 1 8EC
BAMPLING RATE:
100 KC 8TD (rear panel):
STORE/DISPLAY (rear panel):
STOP
INT.
STORE
c. Set Oscilloscope as follows

| Trigger Level: | greater than 0 |
| :--- | :--- |
| Trigger Slope: | greater than 0 |
| Vertical Sensitivity: | $2 V / \mathrm{cm}$ (use probe 10X) |
| Sweep Time: | $\mathbf{1 m s} / \mathrm{cm}$ |

greater than 0
$2 \mathrm{~V} / \mathrm{cm}$ (use probe 10 X )
Vertical Sensitiv
$1 \mathrm{~ms} / \mathrm{cm}$
d. Set switch 81 at $0 V$ position, making sure 82 is open. Press RESET pushbutton on HP-2401C-s1 front panel. The oscilloscope should display the following waveform:

e. Set switch 81 at . $4 V$ position. Set oscilloscope sweep time at $5 \mathrm{~ms} / \mathbf{c m}$.
f. Clone switch $\mathbf{8 2}$. Record the time interval displayed on the oscilloscope (see above waveform). This time interval (upranging time) shall be no greater than 10 ms
g. Open awitch $\mathbf{5 2}$ and press the front panel RESET pushbutton. Record the time interval displayed on the oscilloscope. This time interval (downranging time) shall be no greater than 15 ms .
h. Repeat steps $f$ and $g$ for each of the other positions of switch S1. Record the upranging and downranging times for each position. These times shall be as follows:

| Switch S1 Setting | Upranging <br> Time (Max.) | Downranging <br> Time (Max. |
| :---: | :---: | :---: |
| OV | 10 ms | 10 ms |
| 4V | 10 ms | 15 ms |
| 4V | 16 ms | 21 ms |
| 40 V | 22 ms | 27 ms |
| 400V | 27 ms | 33 ms |



Figure 31-1. Setup for Check of Range Select Time

HP.2401C
$\qquad$ DATE $\qquad$



Table 31-3. Reforence Desigration Index


Table 31-3. Reference Designation Index (Cont'd)





| $\begin{aligned} & \text { Reforence } \\ & \text { Dealinatlon } \end{aligned}$ | Parl No. | Desectipition \# | Nol |
| :---: | :---: | :---: | :---: |
|  |  |  |  |
| A44R7 A 4 R | $0083-3935$ $0683-6825$ |  |  |
| A44R9 | 0683-3935 | R1FXD COMP 39 KOHM S8 $1 / 4 \mathrm{M}$ |  |
| A44R 10 | O6833-3935 | RiFXO COMP 390 OHM $981 / 4{ }^{\text {a }}$ |  |
|  | 0683-2245 | RIFXD COMP 220k OHN $581 / 4 \mathrm{M}$ |  |
| A44R12 | 0603-1035 | RIFXD COMP 10K OHM $581 / 4{ }^{\text {d }}$ |  |
| atarnis | $0683-3935$ $0683-1535$ |  |  |
| 44815 46416 | 0683-3335 | Rifxo comp 33 K OWM $5811 / 4$ |  |
| A44R16 | 0683-3335 | RIFXO COMP 33K OWN $981 / 4 \mathrm{H}$ |  |
| 444R17 | 0683-1045 | Rifxo comp look owns $581 / 4 \mathrm{H}$ |  |
| A44R18 | 0683-5629 | R2FXO COMF $56000 \mathrm{OHM} 581 / 4 \mathrm{M}$ |  |
| A44n20 | O683-1625 $0683-2035$ |  |  |
| A44R21 | 0683-3925 | Rifxo cow 3900 OHM $581 / 41 /$ |  |
| A44R22 | 0603-1239 | Rifxo Conp 12 K Omm $58.1 / 4 \mathrm{~W}$ |  |
| 144R23 | 0603-1535 | RIFXD CONP 15K OHM 58 1/9M |  |
| A44R24 | 0603-3335 | R F FXD Comp 33K OHM $581 / 4{ }^{\text {d }}$ |  |
| A4tras | $0683-3335$ | Rifxo comp 3ik onk $981 / 4{ }^{\text {a }}$ |  |
|  | 068 3-3335 | hifxo conp 33\% OHM 58 1/4W |  |
| 444R27 | 0603-5629 | nifxo Comp 5600 DHM 58 1/4M |  |
|  | $0603-3325$ $0666-1035$ |  |  |
| 444, 30 | 0683-3335 |  |  |
| atar 31 | 0683-3335 | RIFXD COMP 33K OHN $581 / 4 \mathrm{H}$ |  |
| ${ }^{444 R 32}$ | 0603-1035 | Rifxo comp lok onm 58 1/4M |  |
| ${ }^{4} 448.33$ | 0603-1525 | K2FXO COMP $15000 \mathrm{OHM} 581 / 4 \mathrm{M}$ |  |
|  | 06033-3225 | RIFXO CONP $33000 \mathrm{OHM} 581 / 4 \mathrm{H}$ |  |
|  | - $\begin{aligned} & 0683-3335 \\ & 0683-3359\end{aligned}$ | (ex |  |
| A44R 37 | 0683-2225 | Rifxo comp 2.2 X OHM $581 / 4 \mathrm{M}$ |  |
|  | -0603-1035 |  |  |
| ats | 6000-3031 |  |  |
| A4SCI | 0140-0200 | Cifxo mica 390 PF 58 |  |
|  | 0140-0200 $0160-0153$ | CiFXO MICA 390 PF 58, |  |
| A4SC3 A4SC4 | $0160-0153$ $0160-0168$ |  |  |
| A4SCS A 4 SC6 | $0160-0161$ $0170-0040$ | CifxD MY 0.01 UF 108200 VOCK |  |
| A4SC6 | 0170-0040 | cifxi ar . 047 UF 108200 VOCH |  |
| ${ }^{\text {A4S5C7 }}$ | 0160-0157 | CiFxo MY 0.0047 UF 108 200VDCW |  |
| Assc9 | - $0160-0150$ | CIFXO MY 0.0039 UFF 108 200VOCW |  |
| 445 Sc 10 | 0140-0200 | Cifxo mica 390 pf 98 |  |
| a4scil | 0160-0153 | Cifxo Mr 1000 PF 108200 VOCH |  |
| a4sc 12 | 0170-0040 | cifxo ar . 047 UF 108200 VOCH |  |
| ${ }_{4}^{45 C 13}$ | 0160-0161 | cifxo wr 0.01 UF 108200 COCH |  |
|  | ( $0160-0161$ |  |  |




|  | Table 31-4. Replaceable Parts | (Cont'd) |  |  |
| :---: | :---: | :---: | :---: | :---: |
| - Part No. | Decripteo " | Mrs. | Mtr. Pert No. | 70 |
|  | OPTION 31 |  |  |  |
| 0683-9125 | Rifxo canp 9100 Onm $581 / 4 \mathrm{H}$ | 01122 | CE 9125 |  |
| 0686-1035 |  | 01121 | EE 1035 | 2 |
| - 0686 -1049 |  | (ent 0121 | E8 1045 |  |
| 0686-4325 | R PFXD COMP 4300 OHm $581 / 2 \mathrm{~W}$ | 01121 | E8 4325 |  |
| $0686-5125$ | C3FXD COMP 3.1K Onm 58 1/2N | 01121 | E8 5125 |  |
| 0686-5625 | Rifxo whe 5600 Onm $581 / 2 \mathrm{~W}$ | 0122 | E8 5625 |  |
| - 066667525 | Rifxo comp 7500 OHm 58 l 1/2W | 01121 | E8 7525 |  |
| (0699-1815 | R2Fxo compler | (12121 |  |  |
| 0698-0024 | RifXD MEI FLM 2.01 K OHm $181 / 2 \mathrm{~W}$ | 28480 | 0694-0024 |  |
| 0690-3276 | R iFXO MEI FLM Sek OHM 18 1/2W | 19701 | WFic rob |  |
| 0698-3419 |  | 28400 | 0090-3419 |  |
| 0727-0751 | RiFXD DEPC 1000 OHm $181 / 2 \mathrm{M}$ | 20480 | 0727-0751 |  |
| 0727-0765 | R:FXD CARBON FLM 2.6 K OHM $181 / 2 \mathrm{~W}$ | 28480 | 0727-0765 |  |
| 0727-0792 | RiFXD CAREUN FLM 31.6 K OHM $181 / 2 \mathrm{M}$ | 28480 | 0727-0792 |  |
| 0727-0830 |  | 19701 | *TC |  |
| 0727-0940 |  | 19701 |  |  |
| (1) |  | $\begin{aligned} & 28480 \\ & 26400 \end{aligned}$ | $\begin{aligned} & 0757-3159 \\ & 0750-0004 \end{aligned}$ |  |
| 1251-0332 | comuspc 24 cowich is | 28480 | 1251-0332 |  |
| $1850-0332$ $1050-0030$ | Transi storicermeitun Pmo | 02735 | 2 m 04 | 2 |
| 1850-0940 | Trans siorackriniun Pmp | 20420 | ${ }_{2} 1650-0040$ |  |
| 1850-0128 | transistoripmp cermaniun | 01295 | ${ }_{2} 2 \mathrm{~N} 390 \mathrm{C}$ | $\stackrel{1}{6}$ |
| 1050-0145 | transistoascermanium mup | 03500 | 2 m 1926 |  |
| 1050-0184 | transistoraceame ium mup | 02735 | 313398 |  |
| 1051-0024 | tachsistoraceamin ilum mpm | 01295 | 2 m 38 A a |  |
| (1651-0031 |  | (1225 | $\stackrel{\text { 2n100s }}{201605 A}$ | $\frac{1}{3}$ |
| 1901-0025 | DICOEISILICOM L00w 100 ma | 28480 | 1901-0025 |  |
| 1901-0061 | dicoer silicum | 03077 | 1 Me |  |
| 1901-0081 | didoe asilicom so volis morxime | 26480 | 1901-0081 | 9 |
| 1902-0022 | DICOE MEEAXOUMMS 2.67 TV | 26480 | 1802-0022 | 2 |
| 1910-0016 | diooticeamanium looma at 0.est bopiv | 28480 | 1910-0016 |  |
| 2100-0369 | Rivar mem 200 unm 108 lim 1/4w | 28480 | 2100-0369 |  |
| 3060-2577 | TRMMSFUMMER PPULSE | 28400 | 5060-2577 |  |
| 3060-3604 | anmee care | 04404 | 5060-3604 |  |
| 5060-3793 | anmee cumiter | 04404 | 5060-37.0s |  |
| 5060-3831 | ramce comrail | 04404 | 5060-3631 |  |
| 5060-5021 | automame rate de tection |  | 5060-5021 |  |
| 5030-5078 | AUTORAME RATE DETECTOM | 08404 | \$490-9076 | I |
| 9100-1221 |  | 28400 | 41408122 | 2 |
| (1140-0053 |  | $\begin{aligned} & 99846 \\ & 26400 \end{aligned}$ | $\begin{aligned} & 3100-15-102 \\ & 9140-0210 \end{aligned}$ | 1 |
|  |  |  |  | , |



* SUPPLIED WITH HP 24100 ACHOMS COMVERTE * SEE IMSET OW FIGURE 4-3 FOR LOCATION OF OI ON SERIAL PREFIX SIO- AND EARLIER

Figure 31-2. Top Internal View of HP 2401C-31


Figure 31-3. Bottom Internal View of HP 2401C-31
$\cdots$


$$
\begin{aligned}
& \rightarrow-\text { inconasion flem } \rightarrow \text {-accoutlin. }
\end{aligned}
$$










Stock No. 5060-5021 (Serial Prefix 501 thru 605)


Stock No. 5060-5878 (Serial Prefix 610 and above)
(A10) Autorange Rate Detector for Option 31


Figure 31-7. Autorange Rate Detector (A10) for Option 31


Stock No. 5060-3785
(A43) Range Counter for Option 31


"



Stock No. 5060-3831
(A45) Range Control for Option 31



Figure 31-11. A17 and A18 Connections for Option 31


Figure 31-12. Interqonnections for Option 31 (Sheet 1 of 3 ).



Figure 31-12. Interconnections for Option 31 (Sheet 2 of 3)

2401C


# MANUAL SUPPLEMENT <br> MODA MP-24OIC Integrafing Diglial Velimetor Option 35 

### 35.1 GENERAL DESCRIPTION

The HP-2401C-35 Integrating Digital Voltmeter provides negative true recorder outputs in 8-4-2-1 binary code instead of the positive true 4-2'-2-1 code provided by the gtandard HP-2401C recorder cutputs. (See Tables 2-4 and 35-1.) Except for this difference in coding, the Specifications in Section 1.7 of this manual apply without change to the HP-2401C-35.

### 35.2 INSTALLATION AND OPERATION

Install, operate, and program the HP-2401C-35 as specified in Section II of this manual.

### 35.2 THIORY OF OPERATION

## 6 The theory of operation of the HP-2401C-35 is the same as that of the

 standard HP-2401C except as noted in the following paragraphs:35.3.1 Prinfor Coupling Legic A22 (Pigure 35-1)

The logic and circuitry shown in Figure 35-1 converts decimal and function inputs to negative true 8-4-2-1 BCD outputs for recording. The decimal 10-n and function numbers from this assembly are identical to those from a standard printer coupling logic assembly, but they are in -8-4-2-1 code instead of 4-2'-2-1 code. Logic inverters Q17 through Q20 produce the negative true function outputs in response to positive true inputs from the function-to-BCD matrix.

### 35.3.2 Change to Counter Control A16 (Pigures 4-18 and 35-1)

Diodes CR8 and CR9, which connect A16 (H) and (J) to J2 (15) and (16), replace diodes A16CR6 and A16CR5. A16CR5 and A16CR6 are replaced by A16W1 and A16W2 as shown on Figure 35-1.

### 35.3.3 Reversible Decade Coumters All-A1S and A46 (Pigure 35-2)

The decade counter shown in Figure 35-2 differs from that shown in Figure 4-17 only in the arrangement of feedback and the transitars from which the BCD outputs are taken. The negative true outpute are taken from the collectors of the odd numbered transistors (Q1, © , Q5, ©7): The waveforms associated with forward and backward counting of the HP-2401C-35 decades are shown in the circuit diagram, Figure 35-2.

The decades always count up during frequency measurements and daring the first phase of voltage measurements. Up counting is enabled when the count down line is clamped to ground (positive true) and the count $\overline{\mathrm{ip}}$ line is near ' $-35 v$. Both of these signals are provided by Counter Control Logic on A16.

These atates close the down count AND gates and open the up count AND gates. Ponitive triggers are coupled from the collectors of odd-numbered tranaintors (Q1, 3, 5, 7) to aucceeding atages. Each trigger advances the count by one. When the count is advanced from nine to tero, the turn-on of 87 generates a trigger that increases by one the count in the next decade, and so on through all oix counting units. The up count progression is:

| Up Count | Odd-Numbered Tranaistors Off | BCD Output Table |
| :---: | :---: | :---: |
| 0 | None |  |
| 1 | Q1 | 1 |
| 2 | Q3 | 2 |
| 3 | Q1, 9 | $1+2$ |
| 4 | 85 | 4 |
| 5 | Q1, 8 | $1+4$ |
| 6 | 93, 45 | $2+4$ |
| 7 | Q1, Q3, Q5 | $1+2+4$ |
| 8 | 91 | 8 |
| ${ }^{9}$ | Q1, 01 | $1+8$ |
| 10 | None | 0 + Trigger to Next Decade |

At the forward count of 8, conduction through Q8 and CR20 inhibits triggering $O$ QB-Qt by Q1, ascuring that $95-Q 4$ and $85-Q 8$ remain in zoro
 resetting $\alpha$ Q1-Q4 to zero atate also resete © 7 -Q8 to zerg atate through forward count AND dode CR1s and CR dode CR21.

Down counting is commanded by the Counter Control Logic on A16 when the polarity of the input voltage reverces. This is enabled by the posi-tive-true state $\alpha$ the couint $\overline{u p}$ line, which closes the up count AND gates and the nepativo-true atate (bear -35v) of the count down line, which opens the down count AND gatea. Poaitive triggers are then coupled from the collectores of even-numbered tranalators to meceeding etages. The count progreacion is axactly the reverse of the up count progrenaton, which is cummarised abote. starting from the zero atate, the firmt reverce count trigger ecte binary Q1-98, triggering binaries ©s-Q1, Q5-ه3, and Q7-Q8 to ect atate through reverce count AND diodes, CR14, CR16, CR18. Turn
 Q1 and Cl off,regresenting a 9 count. The next trigeger seta Q1-92 to zero matate, reducing the count to 8. The third trigger sets Q1, ©3, and Q6 off, which rescte ©ip-a8 to zero atate, eatablishing the count of 7 . The remaining triggers contimue mubtraction is indicated 50 long an the reverse count is enabled. Each time a trigger sets the decade from 0 to 9 during reverce counting, the turn on of 88 triggers the neat decade through reverse count AND diode CR22, reducing the count of the neat decade by 1.

### 35.4 MAINTENANCE

Figures 4-17, 4-23, 4-24 and 4-34, sheet 2, are replaced by Figurea 35-1 through 35-3. Performance checks 35.1 and 35.2 in Table 35-2 replace checks 15 and 16 in Table 4-3. Shorting linke $W 1$ and $W 2$ replace CR5 and CR6 on Counter Control assembly A16. Otherwise, Section IV instructione of thit manual apply without change to the HP-2401C-35.

Table 35-1. Function Codes

| Data | Function |  | 8 | 4 |  | 1 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | Period (W/30) |  | 0 | 0 | 0 | 0 |
| 1 | +VDC |  | 0 | 0 | 0 | 1 |
| 2 | -VDC |  | 0 | 0 | 1 | 0 |
| 3 | KC |  | 0 | 0 | 1 | 1 |
| 4 | Kת (W/HP-2410B) |  | 0 | 1 | 0 | 0 |
| 5 | M $\Omega$ (W/HP-2410B) |  | 0 | 1 | 0 | 1 |
| 6 | Spare |  | 0 | 1 | 1 | 0 |
| 7 | Spare |  | 0 | 1 | 1 | 1. |
| 8 | Time OVERLOAD |  | 1 | 0 | 0 | 0 |
| 9 |  |  | 1 | 0 | 0 | 1 |
|  | $\begin{aligned} & \text { OVERLOAD } \\ & \text { VAC (W/HP-2410B) } \end{aligned}$ |  | 1 | 0 | 1 | 1 |
| BCD Output Levels: |  | "1" State |  |  |  |  |
|  |  | -35 to -24V |  |  |  |  |
|  |  |  | Function <br> Decimal Point |  |  |  |
|  | - | "0" State | Data Function |  |  |  |
|  |  | -5 to -1V |  | ctí | P |  |

### 35.5 PARTS LIST

The Parts List in Section V of this manual applies to the HP 2401C-35 except as indicated in Tables 35-3 and 35-4.

Table 35-2. In-Cabinet Performance Checks
Perform checks 1 through 14 and 17 through 24 as specified in Table 4-3 and Section 4.2.
35.1 RECORDNG OUTPUTS - BCD FUNCTION

1 digit.
4-line 8-4-2-1 code.
"1" atate level, -35 to -24.5V; "0" state level, -2. 5 to $0 V$.
Source impedance, 33K.
a. Determine and record de function levels at the following pins of J :

| Contral Setting | Function | J2 Pin Code | $\begin{aligned} & 41 \\ & 8 \end{aligned}$ | $\begin{aligned} & 40 \\ & 4 \end{aligned}$ | ${ }^{16}$ | 15 1 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VOLTS, ${ }^{\text {NT }}+1 \mathrm{IV}$ | +VDC |  | 0 | 0 | 0 | 1 |
| VOLT8, ${ }^{\text {NTT-1V }}$ | -VDC |  | 0 | 0 | 1 | 0 |
| FREQ | KC |  | 0 | 0 | 1 | 1 |
| EXT 8EL, 1V | K月 (W/HP-2410B) | - | 0 | 1 | 0 | 0 |
| EXT SEL, 1V | M ${ }^{\text {a }}$ (W/HP-2410B) |  | 0 | 1 | 0 | 1 |
| VOLT8, IV* | OVERLOAD |  | 1 | 0 | 0 | 1 |
| EXTT 8EL, IV | VAC (W/HP-2410B) |  | 1 | 0 | 1 | 1 |

*W/de input aufficient to produce OVERLOAD indication.
b. The source impedance is determined by fixed value 33 K resistors, which can be seen in the assembly A22 circuit diagram, Figure 35-1.

### 35.2 RECORDNG OUTPUTS - BCD DECDMAL PONT

Spectications same as for 35.1.
a. Set HP-2401C FUNCTION switch to VOLT, other controls as epecified below; determine and record de decimal levele at the following pine of J2; short-circuit HI, LO, and GUARD terminale to ataure all zeros reading.

**W/EP-2A11A at +10 gain (10 MV full ecale), FUNCTION at EXTT SEL, Card A30 inetalled.
b. Disconnect short from HI, LO, and GUARD terminals. Set HP-2401C FUNCTION ewitch to FREQ, ATTENUATION control just clockwie from mwitched CHECX position, other controls as epecified below. Use DC Null Voltmeter to check dectmal levels at the following pins of J2:

| Sample Period | Decimal Poodtion | J2 Pin Code | $\begin{aligned} & 27 \\ & \underline{8} \end{aligned}$ | 26 4 | 2 <br> 2 | 1 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| . 018 sec | 00000. 0KC | , | 0 | 0 | 0 |  | $\left(10^{-1}\right)$ |
| 0.18 sec | 0000.00KC |  | 0 | 0 | 1 |  | (10-2) |
| 1.0 sec | 000.000KC |  | 0 | 0 | 1 |  | $\left(10^{-3}\right)$ |
| STOP | 000000 |  | 1 | 0 | 1 |  |  |

c. The source impenance is determined by fixed value sisk reaistors, which can be seen in the ansembly A22 circuit diagram, Figure 35-1.


Table 35-3. Reference Designation Index (Cont'd)


Tubjo sib-3. Reforemice Dasignultion Inder (Cont'd)


Table 36-3. Reforence Dealgation Index (Cont'd)


Table 35-3. Reforence Denimatica Fiodex (Cont'd)


Table 35-3. Refereace Dantmation Buiex (Coad'd)


Table 35-3. Refereace Deatgration Index (Coat'd)

| 5 man | Pret No. | Deceitaina \% | Nate |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { az2nez } \\ & \text { A22Re3 } \\ & \text { A22Rc4 } \\ & \text { an } \end{aligned}$ | $\begin{aligned} & 0757-0955 \\ & 063-3335 \\ & 063-2045 \end{aligned}$ | crions <br> ase <br> R8 FKD FLM 20n OHM 28 1/3M A: FXD COM 33x ONW 58 1/4M asFxO COW 200W OMM 58 1/4W same AB A11, Une mentix am |  |

Tabe 38-4. Repisconile Parts


is




Stock No. 5060-5644
(A11-A15) Reversible -8-4-2-1 Decade Counter for Option 35



Figure 35-3. Interconnection Changes for Option 35

# MANUAL SUPPLEMENT <br> mODM MP-2401C Intogrefing Digitel Veltmotor <br> <br> Option 146 

 <br> <br> Option 146}

### 146.1 GENERAL DEBCRIPTION

The HP-2401C-146 Integrating Digital Voltmeter permits connecting command signals to a computer (such as the HP Model 2116 Computer) by a single connector. This is accomplished by internal wiring changes.

### 146.2 INSTALLATION AND OPERATION

Installation and operation of the HP-2401C-146 is the same as for the standard HP-2401C except a signal at COUNTER RESET connector J4 on the rear panel will be routed to the computer via pin $n$ of PROGRAM CONTROL connector J1. The compiter in turn will control counter reset via J1 (c). Also, the +Record Command is routed to the Computer via $J(r)$ as well as to pin 23 of BCD OUTPUT connector J2.

### 146.3 TMEORY OF OPIRATION

Theory of operation of the HP-2401C-146 is the same as for the standard HP-2401C except external programming signals are routed as explained in Section 146.2.

### 146.4. MANMTENANCE

Figure 146-1 shows the connections to A17, which differ from the standard HP-2401C. Figure 146-2 abows changes in interconnections for the HP-2401C-146. Otherwise, the maintenince instructions in section IV of this manual are directly applicable witiout. change to the BP-2401C-146.
146.5 Pants list

The Parts List in Section V of this manual applies to the HP-2401C-146 except as indicated in Tables 146-1 and 146-2.

Table 140-1. Reformece Deatoration buiex

| Lnem | OPution | Deacrixion \# | Note |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { C14 } \\ & 080 \end{aligned}$ | $\begin{aligned} & \text { 0160-0161 } \\ & \text { ase3-1025 } \end{aligned}$ | cricion hes <br> a0D THE FOLLONIMG TO TABLE 5-1 TO make the tacle applicasle to the hp 2401C-146 <br> CEFXD MY 0.01 UF 108200 VOCH <br> RBFXO COMP 1000 OHM 5\% 1/4W |  |

Table 140-2. Repiacenble Parte

| - Put No. | Decertation \% | ME. | Mif. Pat No. | T0 |
| :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { 0160-0161 } \\ & 063-1025 \end{aligned}$ | Crmow im <br> CsFXD MV 0.01 uF 108200 VDCH ReFXD COM 1000 OM 58 1/4M | $\begin{aligned} & 28480 \\ & 01121 \end{aligned}$ | $\begin{aligned} & 0160-0161 \\ & \text { CB } 1025 \end{aligned}$ | 1 |



Figure 146-1. A17 and A18 Connections for Option 146


Figure 146-2. Interconnection Changes for Option 146



Tho romody is to replace CRA with a $1 \mathrm{~K}, \mathrm{n}, 0.25$ watt, Allon Bradicy resistor, stock number 0083-1025. This chango will be made on all 2401C Voltmetors, sorial number 526-00221, and abovg.
E.
$t$.


9



HEWLETT

## MODEL 2401C INTEGRATINO DIGITAL VOLTMETER

## Diaplay Docaden Ehowing counts during Reset Sorial. Prefixed Bolow 605

Some DY-2401C Voltmetern will mow orratic oounta during remet.
While remetting the dimplay decades, a binary, which im react to ita Zoro etate, will ocoanionally pane a puise to the following binary. The following binarien will acoopt this pulee an a counter pulse at the time the reset pulse in removed.

The reault is an oocamional count appearing when the display decaden ehould be renet to Zoro.

A eimple oure for thia in to gate off the up/down gates so that no pulise oan be transforrod during the roset poriod.

Pleame note that the following modification is broken down into 3 seotionm. Seotions 1 and 2 should be done with all 2401C's oxcopt M70 or combinations with the M70. Bections 1 and 3 chould be done with 2401C's having the M70.

1. A 16 6060-3809

| Add CRAO | Diodo | -hp- stook number | 1901-0081 |
| :--- | :--- | :--- | :--- |
| Dol R76 | Rosistor 33 K | -hp- stock number | $0683-3335$ |
| Add R76 | Rosistor 27 K | -hp- stock numbor | $0683-2735$ |



BOARD LAYOUT C8100-1569


# HP-2401C M146 INTMRORATIMO DIOITAL VOLTMETER <br> FAILURE TO GIVE THE BP-2116A COMPUTER <br> THE PROPER PRIMT COMAND 

Sorial Preifxea Below 739-

When uising the 2401C M146 with the RP-2116A Computer, the voltmeter may not ianue a print comand to the DisI oard in the computer. When thin problem ocours, the 2116A Computer $\quad 111$ appear to be at fault. The true mource of the problem has been traced to the 2401C M146, Voltmeter.

The print command from the atandard 2401C in normally 25 volte, however, when M146 in ingtalled, a parallel print comand in takon out on Jl pin $\bar{r}$. The print command on Jl $\overline{\mathrm{F}}$ in an input to the DVM program board in the 2116A. The DWM board has an 8 volt Zener Diode in merien with the print command which clampe the print comand at a maximum of 8 volte. The parallel print command on $J 2$ pin 23 is not large enough to trigger the DSI board in the 2116A Computer.

All 2401 C m 148 Voltmeters in the field should have the following modification installed:

Add: R20 Reaistor, fixed, 1000 ohme HP stock number 0683-1025

Add: Terminal, atand off HP stock number 0360-0018


# BP-2401C INTYORATINO DIGITAL VOLTMETER REPLACFIET OF THE AC LIME FILTMR <br> Berial Prelixen 736 and Below 

A new AC line filter hat been developed for une in the RP-2401C. The new line filter W111 Withatand a higher voltage in the line to ground inaulation teat.

The HP atock number for the preferred line filter 18:

0100-2477
Be aure to update the Table of Replaceable Parte Section in your Operating and Service Manual.

$\mathrm{LV} / \mathrm{tj} / \mathrm{wo}$

#  OECIMGATIOA OF TEE +12 NOLE PONR EUPPLI <br> Serial Prefixen 739 and Below 

Bone 2401C voltmetere have mown noine counta in excean of the mpecifications ( $\pm 2$ counta). This noise in cauced by oncillation of the +12 volt power mupply.

To correct this problem make the following modification:

1. Delete C13 10pf, hp stock number 0160-2197 NOTE: On unite below cerial number 735-02037, C13 does not exiet.
2. Add C13 91pf, hp ntock number 0160-2203. The capacitor mould be inatalled on connector zA34, ping 6 and 6.

In addition to the above change, if a field replacement of A34, A35, or A36 is made it may be necenasary to make the following change:
I 1. Add or remove C12, hp atock number 0140-0149 on connector XA34, pins 1 and 5.
NOTE: On units having the Paco power transiormer, the capacitor Cl2 will be on connector XA34 pine 1 and 6.

This change is necessary because Cl2 is selected in production test to compensate for parameter changes due to lead lengths and dressing of the cable harness.

Be sure and update the Table of Replaceable parts in the Operating and Service Manual.

LV/tj/wo

[^2]
## SERVICENOTE

## HP MODEL 2401C-M81

## LOCK-UP ON ONE RANGE

Serial Number 751-02187 and below

When operated at ambient temperatures above $50^{\circ} \mathrm{C}$, the HP 2401C-M31 autorange circuit tende to lock-up on one range. This problem has been traced to trangiators A10Q1 and A10Q2 on the Auto-range Rate Detector Aesembly A10 (HP 8tk. No. 5060-5878): Typically, these transistors have a lower beta and frequency response than this circuit requires.

To correct this problem, make the; following changes on A10: remove Q1 and Q2 (HP stock No. 1850-0048) and replace them with two HP Stk. No. 1850-0184 transistors. Change the Table of Replaceable Parts to reflect this modification.

Calibration of the Auto-range Rate Detector circuit is required after this change. To calibrate this circuit, use the procedures given in the HP2401C Operating and Service Manual (page M31-10, table 31.2, performance check M31.1),

# HP 2401C <br> INTEGRATING DIGITAL VOLTMETER 

NEGATIVE CHANNEL BOARD FAILURE
Serial Number 811-2508 and below

## PROBLEM DESCRIPTION

When operating the 2401C IDVM in a data acquisition system with a acanner such as the 2001A Input Scanner or 2011 Crosabar switch, switching transients may dentroy tranaletor 96 on the Negative Channel Board (A32). This problem has occurred when switching +750 V through the scanner to the voltmeter.

## PROBLEM SOLUTION

- Replace transistor Q6 with a direct replacement having a higher breabdown voltage.


## PROCEDURE

1. Remove A32 Negative Channel Board (Stock No. 5060-5001).
2. Remove transistor $\mathbf{Q 6}$ from Channel Board (Stock No. 1851-0091).
3. Install transistor Q6 (Stock No. 1851-0034).
4. Install A32 in 2401C IDVM.
5. Correct the Table of Replaceable Parts to reflect this change.
6. No adjustment or calibration of the instrument is necessary.

This change is incorporated in voltmeters with serial numbers 811-2569 and above.

Ray Nelson/jc/wo

Europe: 64 Route Det Acecies, Geneva. Bwtirertend. Cebte: "HEWPACKBA" Tel. (0221 42.e1.80 6/68-6
HP 2401C
INTEGRATING DIGITAL VOLTMETER
NEGATIVE CHANNEL BOARD FAILURE
Serial Number 811-2568 and below

## PROBLEM DESCRIPTION

When operating the 2401C DVM in a deta acquisition system with a scanner such as the 2901A Input Scanner or 2911 Crossbar Switch, switching transients may dentroy transistor 96 on the Negative Channel Board (A32). This problem has occurred when switching +750 V through the scanner to the voltmeter.

## PROBLEM SOLUTLON

Replece transistor 96 with a direct replacement having a higher breakdown voltage.

## PROCEDURE

1. Remove A32 Negative Channel Board (Stock No. 5060-5001).
2. Remove transistor $\mathbf{Q 6}$ from Channel Board (Stock No. 1851-0031).
3. Install transistor Q6 (Stock No. 1851-0034).
4. Install A32 in 2401 C IDVM.
5. Correct the Table of Replaceable Parts to reflect this change.
6. No adjustment or calibration of the instrument is necessary.

This change is incorporated in voltmeters with serial numbers 811-2569 and above.

Ray Nelson/jc/wo
Cuptomer Bervice - 331 Loma Avenue. Mountain Viw, Cathornle 84040. Tel. (418) pe8.9200


# HP MODEL 2401C-M31 DIGITAL VOLTMETER <br> Serial Numbers 1020A-02897 and Below 

RECOMMENDED TRANSISTOR REPLACEMENT
A44Q5

Hewlett-Packard Part Number 1854-0071 is the recommended replacement for transistor A4405 (HP Part Number 1851-0034). The new transistor has greater reliability but is recommended for replacement only if failure occurs.

Instruments with serial numbers 1020A-02898 above, have the 1854-0071 installed during manufacture.

Correct the Replaceable Parts List in your Operating and Service Manual.

DH/ep/WO


INTEGRATING DIGITAL VOLTMETÉR

## MANUAL. PIUNTED: June 1969

MANUAL, PART NUMBER: 02401-0028
SFIUAL. NUMBERS (OVERED): Serial numbers prefixed 501-through 811-
SHPPIEMENT DESCILIPTION: The purpoee of this supplement is to correct mamal errora, to describe differences between the instrument described in the manual and the instrument furnished, and to provide additional opera ting and service information, as required.

## DESCRIPTION

Serial numbers prefixed 1020A (Product Safety Improvements).
Starting with instruments having serial numbers prefixed 1020A, electrical parts changes were made to ac power input circuits as follows:

Page 1-8, ACCESSORIES FURNISHED, item 1. Change to read:
"1. Power Cord, Length 7-1/2 feet, plugs into rear connector. Stock No. 8120-1348."
Page 2-1, Paragraph 2.1.1. The line set switch now bears the nomenclature 8ELECTOR switch.
Page 2-4, Paragraph 2.4.1, last item. Change to read:
"POWER switch and~LINE (ac line) fuse: Controls ac power to the voltmeter. Logend 115 V 2 AT prescribes 2 -ampere fuse with normal time lag (slow-blow) for 115 -valt operation and legend 230 V 1 AT prescribes 1 -ampere fuse with normal time lag fgr 230 -vilit operation."
Page 2-5, Paragraph 2.4.2, last item. Change to read:
'SELECTOR swltch and ~LINE receptacle. Switch aets the instrument for operation from 115 or $2 \overline{30}$ line valtage. Legend for LiNE receptacle includes operating line voltage and tolerance ( $115 / 230 \mathrm{~V} \pm 10 \%$ ), line frequency range ( $48-66 \sim$, and maxdmum power consumption ( 150 VA MAX.).".
Page 4-87, Figure 4-34, sheet 3 of 3. In lower center of figure change LINE SET 811 sedtch to SELECTOR SII switch.

Page 5-43, Table 5-1. Change part numbers and descriptions as follows

| Ref. Des. | Part No. |
| :---: | :---: |
| Fl | 2110-0303 |
| F2 | 2110-0312 |
| FL1 | 9100-3115 |
| S7 | 3101-0030 |
| 810 | 3101-0030 |
| S11 | 3101-1234 |

## Deacription

Fuse: Cartridge 2A, 250V, slow-Elow Fuse: Cartridge 1A, 250V, slow-Elow Filter, Line, 6A Switch: Toggle SPST, 15A, 125VAC Switch: Toggle, 8PST, 15A, 125VAC 8witch: slide, DPDT

Pages 5-54 and 5-55. Delete entire listing for 2110-0006, 2110-0007, 3101-0001, 3101-0033, and 9100-2477. Add new listings as follows:

| Part No. | Description | Mir | Met Part |
| :---: | :---: | :---: | :---: |
| 2110-0303 | Fuse: Cartridge 2A | 71400 | MDX-2A |
| 2110-0312 | Fuge: Cartridre 1A | 71400 | MDL-1A |
| 3101-0030 | Switch: Togele, 8RST | 88140 | $890015988{ }^{\text {¢ }}$ |
| 3101-1234 | Switch: 8lide, DPDT | 82389 | 11A-1242 |
| 9100-3115 | Filter: Line |  | 11A-12. |


[^0]:    NOTE: THIS IS A SUMMARY OF DETAILED DESCRIPTION FROM LOGIC SYMBOLOGY. A PUBLICATION AVAILABLE THROUGH HEWLETT-PACKARD SALES AND SERVICE OFFICES

[^1]:    *Measurement of period up to 99999.9 MILLISEC is possible with pulse input specified for frequency measurement.

[^2]:    Cusfomer Bervice - sss Logue Avenue, Mountain Viow, Callfornla 94060. Tel. (415) 080 -9800
    : Europe: Of Route Des Acaclas, Geneva, Ew/izertand, Cable: "MEWPACKSA" rol. (028) 42.01.60

