Deterministic Latency

Both ends of the JESD204B link contain various clock domains distributed throughout each system. Data traversing from one clock domain to a different clock domain can lead to ambiguous delays in the JESD204B link. These ambiguities lead to non-repeatable latencies across the link from one power cycle or link reset to the next. The AD9083 supports JESD204B Subclass 0 and Subclass 1 operation. If deterministic latency is not a system requirement, Subclass 0 operation is recommended and the SYSREF signal may not be required. Even in Subclass 0 mode, the SYSREF signal can required in an application where multiple AD9083 devices must be synchronized with each other.

Subclass 0

If there is no requirement for multichip synchronization while operating in Subclass 0 mode, the SYSREF input can be left disconnected. In this mode, the relationship of the JESD204B clocks between the JESD204B transmitter and receiver are arbitrary but does not affect the ability of the receiver to capture and align the lanes within the link

Subclass 1

The JESD204B protocol organizes data samples into octets, frames, and multiframes, as described in the Transport Layer section of this data sheet. The LMFC is synchronous with the beginnings of these multiframes. In Subclass 1 operation, the SYSREF signal is used to synchronize the LMFCs for each device in a link or across multiple links (within the AD9083, SYSREF signal also synchronizes the internal sample dividers). The JESD204B receiver uses the multiframe boundaries and buffering to achieve consistent latency across lanes (or even multiple devices), and also to achieve a fixed latency between power cycles and link reset conditions. The AD9083 features sampled SYSREF modes for JESD204B Subclass 1 operation. See the Multichip Synchronization (MCS) section for details.

Multichip Synchronization

The AD9083 has a JESD204B Subclass 1 compatible SYSREF input, which provides flexible options for synchronizing the internal blocks of the AD9083. The SYSREF input is a source synchronous system reference signal used to align the AD9083 LMFCs that enables multichip synchronization between multiple AD9083s. The input clock divider, the signal processing tile, signal monitor block, and JESD204B link can be synchronized using the SYSREF input.

Sampled SYSREF Mode

In sampled SYSREF mode, SYSREF operates as a standard JESD204B Subclass 1 signal.

The following are some characteristics of sampled SYSREF synchronization:

- Synchronous sampling of SYSREF.
- Must meet setup/hold time requirements for reliable synchronization. This is increasingly difficult to achieve as the sample rate increases.
- SYSREF jitter must be much less than one sample clock period. A SYSREF coming from an ASIC or an FPGA may have significant jitter.

AD9083 SYSREF interface with an LVDS input.

The AD9083 SYSREF input is a differential input, which is specified to accept typically 700mVolts to a maximum of 1100mVolts with a common mode voltage of 0.5Volts. The SYSREF +/- input can be terminated by an internal 100ohmns resistor. It is necessary to ensure that this internal 100ohms termination resistor is removed by disabling the SYSREF termination. Register 0xD4C set to 0x05 disables the SYSREF termination.

See Figure x below,(AVDD = 1Volt.)

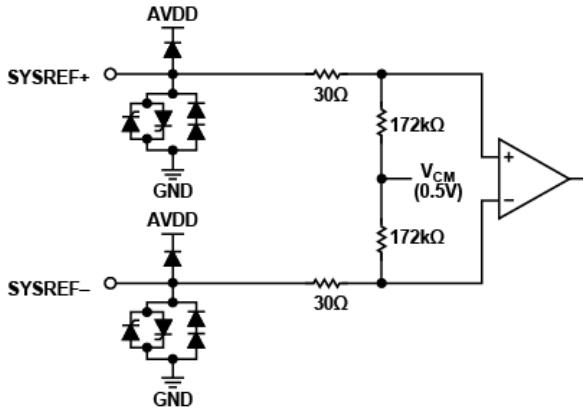

Figure. 1 AD9083 SYSREF input

LVDS signals are differential signals with a typical swing of 700mVolts on a common mode voltage of 1.2Volts. The AD9528 clock output in LVDS mode provides these signal levels, see Figure y.

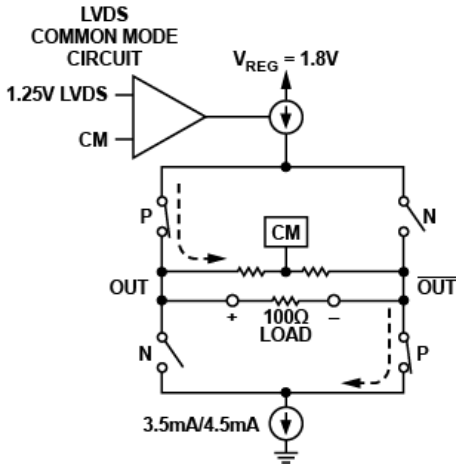

Figure. 2 AD9528 clock output in LVDS mode

A common mode level shift between the LVDS output and the AD9083 +/-SYSREF input is required to interface the AD9083 +/- SYSREF input to a standard LVDS differential input. Figure.z shows the LVDS to AD9083 SYSREF common mode level shift circuit recommended with an LVDS SYSREF source.

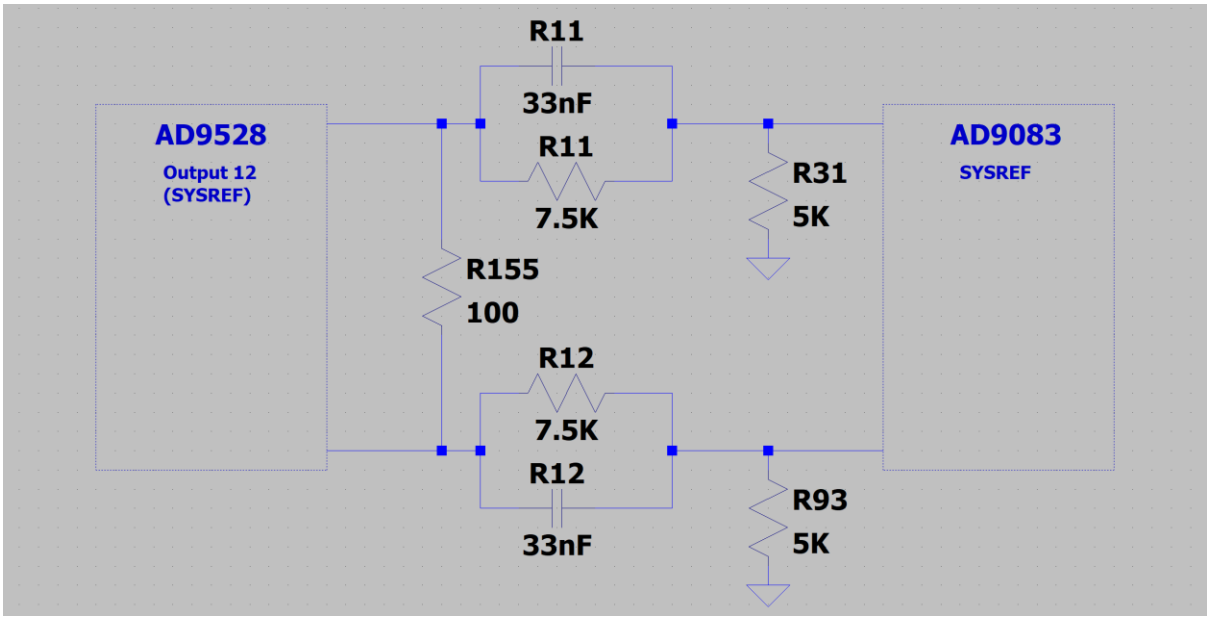

Figure 3. LVDS to AD9083 SYSREF common mode level shift circuit

SYSREF Registers writes

Table x. Subclass 1 Required Register Writes

R/W	Register	Bits	Value	Description
W	0xD4C	[7:0]	0x05	Disable SYSREF Termination
W	0x1C0	[7:0]	0x04	SYNC_CTRL1
W	0x1C4	[7:0]	0x01	DDC_SYNC_CTRL
W	0x28E	[7:5] [4:0]	0x1 N′	JTX_SUBCLASSV_CFG =1, JTX_NP_CFG
W	0x284	[7:0]	0x10	JTX_TPL_SYSREF_N_ SHOT
W	0x260	[7:0]	0xC0	JTX_CORE_CONFIG

In order to configure the AD9083 in JESD204B Subclass 1, program JTX_SUBCLASSV_CFG bits to 1 (Register 0x28E, [7:5] to 1).

Register 0xD4C set to 0x05 disables the SYSREF termination to allow the use of an external common mode level shift , see Figure z.

In resynchronization mode with the SYSREF_RESYNC_
MODE bit (Register 0x1C0, Bit 2 =1), the AD9083 aligns all internal clocks to the SYSREF signal (for Subclass 1 synchronization and deterministic latency). In the case of periodic SYSREF, after alignment is achieved, further periodic SYSREF inputs are automatically aligned to the internal clocks. A change in the SYSREF input phase initiates a re-alignment of the datapath clocks to the new SYSREF input phase.

The NCORESET_ALL_SYSREF bit field set to 0 (default) in Register 0x1C0, Bit 3 ensures that the NCOs only receive a reset pulse in response to a SYSREF pulse that has resynchronized the clocks.

Program the NCOs to continuous synchronization mode by programming DDC_SYNC_NEXT Bit[1]= 0 and DDC_SYNC_EN [0] = 1 in Register 0x1C4.

The DDCs are programmed to reset the NCOs in response to the periodic SYSREF pulse or the Nth SYSREF pulse received using Register 0x284 (JTX_TPL_SYSREF_N_SHOT).

JTX_SYSREF_FOR_RELINK bit 7 in Register 0x260 and JTX_SYSREF_FOR_STARTUP bit 6 in Register 0x260 should be programmed to 1. Enabling these bits ensures that the JESD link will output all 0's during the synchronization process until valid data is being sent.

Synchronisation status of the AD9083 can be checked by reading bits [3:1] of Register 0x27E.

SYSREF phase has been established, Register 0x27E bit [1] jtx_tpl_sysref_rcvd = 1.

Incoming SYSREF has been registered at the expected time from the previously established SYSREF , Register 0x27E bit [2] jtx_tpl_sysref_phase_err = 0.

LFMC phase (set with SYSREF) has been successfully transfered from the transport layer to the link layer, Register 0x27E bit [3] jtx_tpl_phase_established = 1.

SYSREF Related Functionality

The AD9083 supports resynchronization of internal clocks and NCOs, as well as across multiple AD9083 devices. The SYSREF and trigger signal inputs to the AD9083 are used to provide a synchronization triggering mechanism that supports

- Deterministic latency in JESD Subclass 1 mode.
- Multichip synchronization for NCO reset.

Multichip Synchronization and NCO Reset Options

There are two aspects of multichip synchronization:

- Aligning the clocks across multiple devices.
- Aligning the NCOs across multiple devices.

Aligning Clocks Across Multiple Devices

Aligning the clocks across multiple devices is provided by the SYSREF signal in resynchronization mode. The SYSREF signal is used to align all the clocks in the AD9083. When SYSREF is deterministically sampled by multiple devices, it implies that the clocks are aligned across multiple devices.

Aligning NCOs Across Multiple Devices

NCO reset is handled by the reset of the NCO accumulators in the AD9083 signal processing tiles. To ensure that the NCOs are reset deterministically across devices, it is important to use resynchronization mode.

An external controller (for example, a clock generator chip) generates periodic SYSREF pulses or a one-shot SYSREF pulse to the SYSREF input.

Key Features and Notes Regarding Resynchronization Mode

In SYSREF resynchronization mode, all clocks shut down and restart in-phase to the SYSREF pulse.

The JESD LMFC aligns at a deterministic phase/delay from the SYSREF pulse.

The NCOs reset at a deterministic time after the SYSREF pulse is received. The NCO reset occurs after the datapath clocks are aligned to the new SYSREF.

The latency numbers, such as SYSREF LMFC delay, SYSREF to NCO reset delay, and so on, depend on the configuration used.

The latency of the NCO reset from SYSREF is constant for all periodic SYSREF pulses. If the SYSREF period is altered, a resynchronization followed by an NCO reset is triggered.

The SYSREF period for any mode must be a multiple of the multiframe clock period. Additional restriction may be required due to decimation modes.

An LMFC settling period of 8 LMFCs is expected for the internal LMFC to stabilize after a SYSREF input initiates realignment.