A Mostly-Digital Variable-Rate Continuous-Time Delta-Sigma Modulator ADC

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***Abstract*—This paper presents a reconfigurable continuous-time delta-sigma modulator for analog-to-digital conversion that consists mostly of digital circuitry. It is a voltage-controlled ring oscillator based design with new digital background calibration and self-cancelling dither techniques applied to enhance performance. Unlike conventional delta-sigma modulators, it does not contain analog integrators, feedback DACs, comparators, or reference voltages, and does not require a low-jitter clock. Therefore, it uses less area than comparable conventional delta-sigma modulators, and the architecture is well-suited to IC processes optimized for fast digital circuitry. The prototype IC is implemented in 65 nm LP CMOS technology with power dissipation, output sample-rate, bandwidth, and peak SNDR ranges of 8–17 mW, 0.5–1.15 GHz, 3.9–18 MHz, and 67–78 dB, respectively, and an active area of 0.07 mm^2.**

***Index Terms*—Continuous-time delta-sigma modulator, delta-sigma ADC, VCO ADC.**

I. Introduction

In MANY analog-to-digital converter (ADC) applications such as wireless receiver handsets, the bandwidth of the analog signal of interest is narrow relative to practical ADC sample-rates. Delta-sigma ($\Delta\Sigma$) modulator ADCs are used almost exclusively in such applications because they offer exceptional efficiency and relax the analog filtering required prior to digitization [1]. Continuous-time $\Delta\Sigma$ modulator ADCs with clock rates above several hundred MHz have been shown to be particularly good in these respects [2]–[5].

Unfortunately, conventional analog $\Delta\Sigma$ modulators present significant design challenges when implemented in highly-scaled CMOS IC technology optimized for digital circuitry. They require analog comparators, high-accuracy analog integrators, high-linearity feedback DACs, and low-noise, low-impedance reference voltage sources. Continuous-time $\Delta\Sigma$ modulators with continuous-time feedback DACs additionally require low-jitter clock sources. These circuit blocks are increasingly difficult to design as CMOS technology is scaled below the 90 nm node because the scaling tends to worsen supply voltage limitations, device leakage, device nonlinearity, signal isolation, and $1/f$ noise.

An alternate type of $\Delta\Sigma$ modulator which does not require the above-mentioned analog blocks consists of a voltage-controlled ring oscillator (ring VCO) with its inverters sampled at the desired output sample-rate followed by digital circuitry [6]–[11]. Although the ring VCO inevitably introduces severe nonlinearity, the structure otherwise has the same functionality as a first-order continuous-time $\Delta\Sigma$ modulator. Unfortunately, the nonlinearity problem and the high spurious tone content of first-order $\Delta\Sigma$ modulator quantization noise has limited the deployment of such VCO-based $\Delta\Sigma$ modulators to date. The only previously published method of circumventing these problems is to use the VCO-based $\Delta\Sigma$ modulator as the last stage of an otherwise conventional analog $\Delta\Sigma$ modulator, but this solution requires all the high-performance analog blocks of a conventional analog $\Delta\Sigma$ modulator except comparators [12].

This paper presents a VCO-based $\Delta\Sigma$ modulator that incorporates two new techniques with which it avoids these problems: digital background correction of VCO nonlinearity, and self-cancelling dither [13]. The digital background calibration technique is an extension of a technique originally used to correct nonlinear distortion in pipelined ADCs [14], [15]. The self-cancelling dither technique eliminates the spurious tone problem by adding dither sequences prior to quantization and then cancelling them in the digital domain. Additionally, the $\Delta\Sigma$ modulator uses a new digital calibration technique that enables reconfigurability by automatically retuning the VCO's center frequency whenever the $\Delta\Sigma$ modulator's sample-rate is changed.

The new techniques enable the $\Delta\Sigma$ modulator to achieve high-performance data conversion without analog integrators, feedback DACs, comparators, reference voltages, or a low-jitter clock. Therefore, it uses less area than comparable conventional analog $\Delta\Sigma$ modulators, and the architecture is well-suited to highly-scaled CMOS technology optimized for fast digital circuitry.

The paper consists of four main sections. Section II describes the VCO-based $\Delta\Sigma$ modulator concept, and quantifies the VCO nonlinearity problem. Sections III and IV describe the $\Delta\Sigma$ modulator's new signal processing enhancements and key circuits, respectively. Section V presents measurement results.

II. VCO-Based $\Delta\Sigma$ Modulator Overview

A. Ideal Operation

An idealized VCO-based $\Delta\Sigma$ modulator with a continuous-time input voltage, $v(t)$, and a digital output signal, $y[n]$, is

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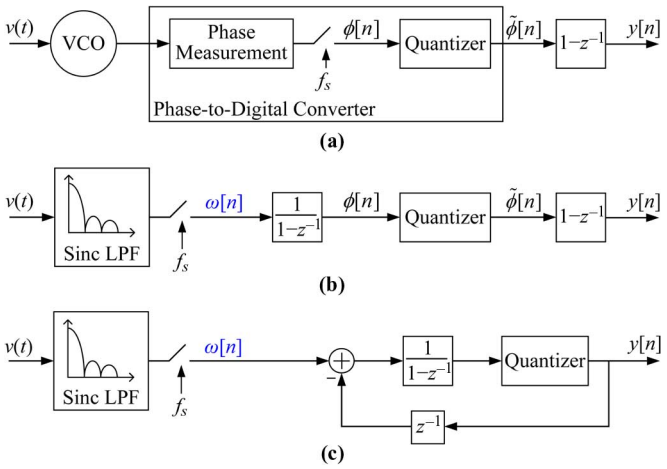

Fig. 1. Equivalent systems: (a) a generic VCO-based $\Delta\Sigma$ modulator, (b) the cascade of a continuous-time low-pass filter, sampler, quantizer, and digital differentiator, and (c) the cascade of a continuous-time low-pass filter, sampler and first-order $\Delta\Sigma$ modulator.

shown in Fig. 1(a). It consists of a VCO, a phase-to-digital converter, and a digital differentiator block with a transfer function of $1 - z^{-1}$. Ideally, the instantaneous frequency of the VCO is

$$f_{\mathrm{VCO}}(t) = f_s + \frac{K_{\mathrm{VCO}}}{2\pi} v(t) \tag{1}$$

where f_s is the center frequency of the VCO in Hz, and K_{VCO} is the VCO gain in radians per second per volt. The phase-to-digital converter quantizes the VCO phase, i.e., the time integral of the instantaneous frequency, and generates output samples of the result at times nT_s, $n = 0, 1, 2, \ldots$, where $T_s = 1/f_s$.

In a practical implementation the phase-to-digital converter would typically generate its output samples modulo one-cycle. It can be verified that provided

$$0.5 f_s < f_{\mathrm{VCO}}(t) < 1.5 f_s \tag{2}$$

for all t and another modulo one-cycle operation is performed after the digital differentiator, then the digital output signal is not affected by the modulo operations. Therefore, the modulo operations are not considered in the following to simplify the explanation.

Aside from an integer multiple of a cycle (which ultimately has no effect on $y[n]$ because of the modulo operations), the nth output sample of the phase to digital converter in radians is a quantized version of

$$\phi[n] = \int_0^{nT_s} K_{\mathrm{VCO}} v(\tau) d\tau. \tag{3}$$

Equivalently, (3) can be written as

$$\phi[n] = \sum_{k=1}^{n} \omega[k] \tag{4}$$

where

$$\omega[n] = \int_{(n-1)T_s}^{nT_s} K_{\mathrm{VCO}} v(\tau) d\tau. \tag{5}$$

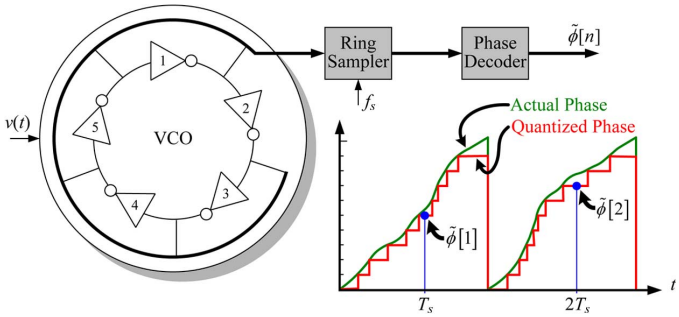

Fig. 2. Example of a ring VCO and phase-to-digital converter.

It follows that $\omega[n]$ could have been obtained by passing $v(t)$ through a low-pass continuous-time filter with transfer function

$$H_c(f) = K_{\mathrm{VCO}} e^{-j\pi T_s f} \frac{\sin(\pi T_s f)}{\pi f} \tag{6}$$

and sampling the output of the filter at a rate of f_s.

The system of Fig. 1(b) is, therefore, equivalent to that of Fig. 1(a). It obtains $\omega[n]$ by sampling a filtered version of the input signal as described above and implements (4) as a discrete-time integrator. The discrete-time integrator is followed by the same quantizer and digital differentiator as in Fig. 1(a) to obtain $y[n]$.

Given that the discrete-time integrator and differentiator both have integer-valued impulse responses, it can be verified that the system of Fig. 1(b), and, hence, the system of Fig. 1(a), is equivalent to the system of Fig. 1(c) [16]. Thus, the VCO-based $\Delta\Sigma$ modulator is equivalent to a conventional first-order continuous-time $\Delta\Sigma$ modulator, so it can be analyzed by applying well-known properties of the first-order $\Delta\Sigma$ modulator to the system of Fig. 1(c) [1]. In particular

$$y[n] = \omega[n] + e_{\Delta\Sigma}[n] \tag{7}$$

where $e_{\Delta\Sigma}[n]$ is first-order high-pass shaped quantization noise.

B. A Ring VCO Implementation

A practical topology with which to implement the VCO and phase-to-digital converter is shown in Fig. 2. In this example, the VCO is a ring oscillator that consists of five inverters, each with a transition delay that depends on the VCO input voltage, $v(t)$. The ring sampler consists of five flip-flops clocked at a rate of f_s, where the D input of each flip-flop is driven by the output of one of the VCO's inverters. At each rising edge of the clock signal, i.e., at times nT_s, the output of each flip-flop is set high if the corresponding VCO inverter output signal at that time is above the flip-flop's digital logic threshold of approximately half the supply voltage, and is set low otherwise.

A well-known property of ring oscillators is that at any given time during oscillation, exactly one of the VCO's inverters is in a state of either *positive transition* or *negative transition*, i.e., a state in which the inverter's input and output are both below or both above the digital logic thresholds of the flip-flops to which they are connected, respectively. For example, suppose Inverter 1 in Fig. 2 enters positive transition at time t_0. The inverter remains in positive transition until a time t_1 at which its output rises above the digital logic threshold of the flip-flop to

which it is connected. At this same instant, Inverter 2 enters negative transition. This process continues in a clockwise direction around the VCO such that Inverter $(1+(i \bmod 5))$ is in positive transition from time t_i to time t_{i+1} if i is even, and is in negative transition from time t_i to time t_{i+1} if i is odd for $i = 0, 1, 2, \ldots$, where $t_{i+1} > t_i$.

Therefore, each inverter goes once into positive transition and once into negative transition during each VCO period, and there are only 10 possible 5-bit values that the ring sampler can generate regardless of when it is sampled. The phase decoder maps each of the 10 values into a phase number, $\tilde{\phi}[n]$, in the range $\{0, 1, 2, \ldots, 9\}$ (the corresponding phase in radians is given by $2\pi\tilde{\phi}[n]/10$). Since each phase number corresponds to one of the inverters being in a state of transition and there are 10 such states per VCO period, $\tilde{\phi}[n]$ represents the phase of the VCO modulo one-cycle quantized to the nearest 10th of a cycle as depicted in Fig. 2.

Ideally, the VCO inverters are such that the ith transition delay is given by

$$t_{i+1} - t_i = \frac{1}{10}\left[T_s - K_d\overline{v}(t_i, t_{i+1})\right]. \tag{8}$$

where

$$\overline{v}(t_i, t_{i+1}) = \frac{1}{t_{i+1} - t_i}\int_{t_i}^{t_{i+1}} v(t)dt \tag{9}$$

is the average value of $v(t)$ over the time interval from t_i to t_{i+1}. This time interval represents a 10th of the corresponding VCO cycle as described above, so (8) implies that the VCO's *average* frequency during this time interval, i.e.,

$$\frac{1}{t_{i+1} - t_i}\int_{t_i}^{t_{i+1}} f_{\mathrm{VCO}}(t)dt \tag{10}$$

where $f_{\mathrm{VCO}}(t)$ is the VCO's *instantaneous* frequency at time t, can be written as

$$\frac{1}{10(t_{i+1} - t_i)}. \tag{11}$$

Substituting (8) into (11) and expanding the result as a power series yields

$$\frac{1}{t_{i+1} - t_i}\int_{t_i}^{t_{i+1}} f_{\mathrm{VCO}}(t)dt = \frac{1}{T_s}\sum_{n=0}^{\infty}\left(\frac{K_d}{T_s}\overline{v}(t_i, t_{i+1})\right)^n. \tag{12}$$

Provided that $v(t)$ does not change significantly between t_i and t_{i+1}, it follows that the VCO can be modeled as having an instantaneous frequency given by

$$f_{\mathrm{VCO}}(t) = f_s + \frac{K_{\mathrm{VCO}}}{2\pi}v(t) + \frac{1}{T_s}\sum_{n=2}^{\infty}\left(\frac{T_s K_{\mathrm{VCO}}}{2\pi}v(t)\right)^n \tag{13}$$

where $K_{\mathrm{VCO}} \equiv 2\pi K_d/T_s^2$.

C. The Nonlinearity Problem

A comparison of the instantaneous frequency of the ring VCO given by (13) to the ideal instantaneous frequency given by (1) indicates that the ring VCO introduces nonlinear distortion. Applying the reasoning of Section II-A leads to the conclusion that the distortion causes the input to the first-order $\Delta\Sigma$ modulator in the equivalent system of Fig. 1(c) to be

$$\omega[n] + \int_{(n-1)T_s}^{nT_s}\left[\frac{2\pi}{T_s}\sum_{i=2}^{\infty}\left(\frac{T_s K_{\mathrm{VCO}}}{2\pi}v(\tau)\right)^i\right]d\tau \tag{14}$$

instead of just $\omega[n]$. It follows from (5) and (7) that provided $v(t)$ does not change significantly over each sample interval, the output of the $\Delta\Sigma$ modulator is

$$y[n] = \omega[n] + e_{\Delta\Sigma}[n] + \sum_{i=2}^{\infty}\alpha_i\left(\omega[n]\right)^i \tag{15}$$

where

$$\alpha_i \cong \left(\frac{1}{2\pi}\right)^{i-1} \tag{16}$$

for $i = 2, 3, \ldots$, are nonlinear distortion coefficients.

It should be stressed that the nonlinearity is not the result of non-ideal circuit behavior. It is a systematic nonlinearity that occurs even with ideal circuit behavior. The problem is that the VCO's *period* changes linearly with $v(t)$, but to eliminate the nonlinear terms in (14) it would be necessary for the VCO's *frequency* to change linearly with $v(t)$. It is the reciprocal relationship between VCO's period and frequency that give rise to the nonlinear terms in (14). Of course, in practice the relationship between the inverter delays and the input voltage is not perfectly linear as assumed by (8). While this introduces additional significant nonlinearity it tends to be less severe than the reciprocal nonlinearity described above.

Transistor-level simulations of the VCO-based $\Delta\Sigma$ modulator described above with the 15-element VCO designed for the IC prototype presented in this paper support these findings and demonstrate the severity of the problem. For instance, the output of the simulated $\Delta\Sigma$ modulator with $f_s = 1.152$ GHz and a full-scale 250 KHz sinusoidal input signal has second, third, and fourth harmonics at -26 dBc, -47 dBc, and -64 dBc, respectively. When the simulated output sequence is corrected in the digital domain to cancel just the second-, third-, and fourth-order distortion terms using the techniques presented in the next section, the largest harmonic in the corrected sequence is less than -90 dBc.[1] This suggests that for the target specifications of the IC prototype presented in this paper it is only necessary to cancel the second-, third-, and fourth-order distortion terms.

III. Signal Processing Details

The prototype IC contains two identical $\Delta\Sigma$ modulators that each incorporate four of the basic VCO-based $\Delta\Sigma$ modulators described above as separate signal paths. They also contain additional components that implement the digital background calibration and self-cancelling dither techniques. The signal processing details of the $\Delta\Sigma$ modulator design and the reasons for

[1]It can be verified that the technique used to cancel the α_3 term in (15) introduces a fifth-order term that happens to largely cancel the α_5 term in (15) as a side-effect.

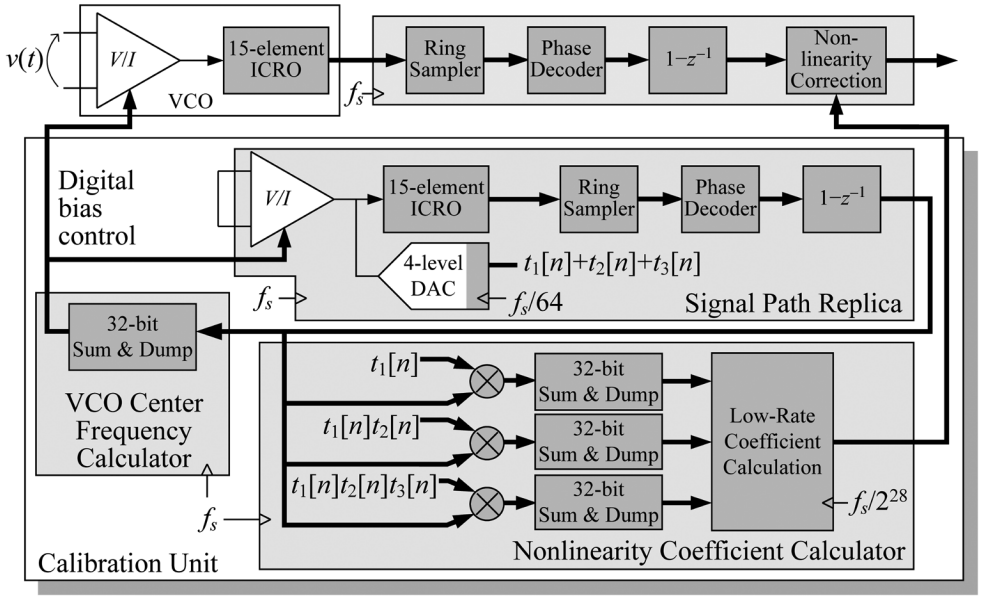

Fig. 3. The prototype IC's on-chip calibration unit shown with a single VCO-based $\Delta\Sigma$ modulator signal path for simplicity.

using four such signal paths in a single $\Delta\Sigma$ modulator are presented in this section.

A. Digital Background Calibration

Two types of digital background calibration are implemented in each $\Delta\Sigma$ modulator: 1) digital background cancellation of VCO-induced second-order and third-order distortion, and 2) digital background tuning of the VCO's center frequency to the $\Delta\Sigma$ modulator's sample rate, f_s. The former in combination with a pseudo-differential architecture to be explained shortly addresses the nonlinearity problem described in the previous section. The latter centers the input range of the $\Delta\Sigma$ modulator about the midscale input voltage. This maximizes the dynamic range, and enables reconfigurability by automatically retuning the VCO's center frequency whenever f_s is changed.

Fig. 3 shows a block diagram of a single VCO-based $\Delta\Sigma$ modulator signal path and the on-chip *calibration unit* shared by all the signal paths in both $\Delta\Sigma$ modulators. The signal path is similar to the VCO-based $\Delta\Sigma$ modulator described in Section II, except that its VCO is implemented as a voltage-to-current (V/I) converter followed by a 15-element current-controlled ring oscillator (ICRO), and it contains a *nonlinearity correction block* that cancels the distortion terms in (15). The calibration unit measures the VCO center frequency and nonlinear distortion of a *signal path replica*, and generates digital data used by the actual signal path to properly tune the VCO's center frequency and cancel nonlinear distortion. The calibration unit operates continuously in background, and periodically updates its output data with new measurement results.

The calibration unit's signal path replica is identical to the actual signal path except that it does not have a nonlinearity correction block, its differential input voltage is zero (i.e., it has a constant, midscale input signal), and a four-level current steering f_s/64-rate DAC adds a calibration sequence to the input of its ICRO. The calibration sequence is $t_1[n] + t_2[n] + t_3[n]$ where the $t_i[n]$ sequences are 2-level, independent, zero-mean, pseudo-random sequences.

VCO Center Frequency Calibration

The calibration unit's *VCO center frequency calculator* block adds each successive set of 2^{28} output samples from the signal path replica and scales the result by a constant, K, to create an $f_s/2^{28}$-rate digital sequence given by

$$\Delta I[m] = K \sum_{i=0}^{P-1} r[mP + i] \tag{17}$$

where $P = 2^{28}$, and $r[n]$ is the output of the signal path replica. The eight most significant bits (MSBs) of this sequence are used to adjust the output current of the V/I converter in the signal path replica. This forms a negative feedback loop with a bandwidth that depends on K. The feedback drives the VCO's output frequency to the point at which $r[n]$ has zero mean. The frequency to which the VCO converges is f_s, because the VCO's input voltage is zero and the calibration sequence has a mean of zero. The V/I converter in the signal path is also adjusted by the $\Delta I[m]$ sequence. To the extent that the signal path and signal path replica match, this causes the signal path's VCO to have a frequency very close to f_s when $v(t) = 0$.

The choice of K is not critical because settling error in the loop introduces only as a small common-mode error in the $\Delta\Sigma$ modulator. In the prototype IC, K was chosen to achieve one-step settling.

Nonlinearity Correction

The nonlinearity correction block in the signal path is a high-speed look-up table with mapping data updated periodically by the *nonlinearity coefficient calculator block* of the calibration

unit. The look-up table maps each 5-bit input sample, $y[n]$, into an output sample, $y[n]|_{\text{corrected}}$, such that

$$y[n]|_{\text{corrected}} = y[n] - \tilde{\alpha}_2 (y[n])^2 - \tilde{\alpha}_3 \left(y[n] - \tilde{\alpha}_2 (y[n])^2\right)^3 \tag{18}$$

where $\tilde{\alpha}_2$, and $\tilde{\alpha}_3$ are measurements of the α_2 and α_3 coefficients in (15), respectively. It can be verified that if $\tilde{\alpha}_i = \alpha_i$, for $i = 2$ and 3, then $y[n]|_{\text{corrected}}$ does not contain any VCO-induced second-order or third-order distortion terms.

Applying (18) to obtain $y[n]|_{\text{corrected}}$ also has some side effects. A positive side effect is that it adds a fifth-order term that happens to nearly cancel the portion of the fifth-order distortion corresponding to α_5 given by (16). Negative side effects are that it adds higher-order distortion terms and cross terms that include $(e_{\Delta\Sigma}[n])^i$ for $i = 2$, 3, 4, 5, and 6. Fortunately, these terms are sufficiently small that they do not significantly degrade the simulated or measured performance of the $\Delta\Sigma$ modulator. The cross terms containing $(e_{\Delta\Sigma}[n])^i$ fold some of the $\Delta\Sigma$ quantization noise into the signal band but the folded noise is well below the overall signal band noise floor of the $\Delta\Sigma$ modulator. This is because the 15-element ring oscillator quantizes each phase estimate to within 1/30 of a VCO period so $e_{\Delta\Sigma}[n]$ is small relative to $\omega[n]$. Had a VCO with fewer ring elements been used, the folding of $\Delta\Sigma$ quantization noise into the signal band would not necessarily have been negligible.

Nonlinearity Coefficient Measurement

The purpose of the *nonlinearity coefficient calculator block* is to generate the 30 values of (18) that correspond to the 30 possible values of $y[n]$. While using the values of α_2 and α_3 given by (16) for $\tilde{\alpha}_2$ and $\tilde{\alpha}_3$, respectively, in (18) would result in cancellation of much of the nonlinear distortion, it would not address nonlinear distortion arising from non-ideal circuit behavior, and simulations suggest that this would limit the ADC's signal-to-noise-and-distortion ratio (SNDR) to between 60 dB and 65 dB.

Therefore, the calibration unit continuously measures α_2 and α_3 by correlating the output of the signal path replica against the three 2-level sequences: $t_1[n]$, $t_1[n] \times t_2[n]$, and $t_1[n] \times t_2[n] \times t_3[n]$, to obtain the three $f_s/2^{28}$-rate sequences given by

$$\gamma_1[m] = \frac{1}{P} \sum_{i=0}^{P-1} r[mP+i] t_1[mP+i], \tag{19}$$

$$\gamma_2[m] = \frac{1}{P} \sum_{i=0}^{P-1} r[mP+i] t_1[mP+i] t_2[mP+i], \tag{20}$$

and

$$\gamma_3[m] = \frac{1}{P} \sum_{i=0}^{P-1} r[mP+i] t_1[mP+i] t_2[mP+i] t_3[mP+i]. \tag{21}$$

where $P = 2^{28}$. It can be verified that when the signal path replica's VCO frequency is f_s,

$$\frac{\gamma_2}{2\gamma_1^2} \approx \alpha_2 \quad \text{and} \quad \frac{\gamma_3}{6\gamma_1^3} \approx \alpha_3. \tag{22}$$

Therefore, the nonlinearity coefficient calculator block calculates the 30 values of (18) with

$$\tilde{\alpha}_2 \triangleq \frac{\gamma_2}{2\gamma_1^2} \quad \text{and} \quad \tilde{\alpha}_3 \triangleq \frac{\gamma_3}{6\gamma_1^3}. \tag{23}$$

It does this and loads the 30 values into the nonlinearity correction block's look-up table once every $2^{28} T_s$ seconds.

The nonlinearity calibration technique described above is based on the same principle as that presented in [15], but one of its differences is that it measures the nonlinear distortion coefficients of a signal path replica instead of the actual signal path. The nonlinearity coefficients could have been measured directly from the output of the actual signal path, but if this had been done there would have been unwanted terms corresponding to $v(t)$ in the correlator output sequences, $\gamma_i[n]$. The variance of each such term is proportional to $1/P$, so for large enough values of P the terms can be neglected. However, P would have had to be much larger than 2^{28} for the terms to be negligible, so the time required to measure the nonlinear distortion coefficients would have been much longer than the $2^{28} T_s$ seconds required by the system described above. For example, when f_s is set to its maximum value of 1.152 GHz, the system described above requires 233 ms to measure the nonlinear distortion coefficients, whereas several tens of seconds would have been required had a signal path replica not been used.

The peak amplitude of the calibration signal also affects the time required to measure the nonlinear distortion coefficients. Each time the amplitude is doubled, P can be divided by four without reducing the variances of the measured nonlinear coefficient values. Therefore, it is desirable to have as large of a calibration sequence as possible in the signal path replica that does not cause the path to overload.

B. Pseudo-Differential Topology

The accuracy with which the nonlinear distortion terms can be cancelled depends on how well the actual signal path matches the signal path replica and also on bandwidth limitations of the signal path itself. For example, transistor-level simulations of the system shown in Fig. 3 indicate that the nonlinearity correction block only reduces the worst-case second-order distortion term from -28 dBc to -65 dBc, which is well below the target specification for this project.

This limitation is addressed in the $\Delta\Sigma$ modulator by combining two signal paths to form a single *pseudo-differential signal path* as shown in Fig. 4. The two signal paths differ from the signal path shown in Fig. 3 in that they share a single fully-differential V/I converter. Otherwise, the signal path blocks shown in Fig. 4 are the same as those shown in Fig. 3. The outputs of the two signal paths are differenced to form the output of the pseudo-differential signal path. The differencing operation causes the residual even-order distortion components in the outputs of the two nonlinearity correction blocks to cancel up to the matching accuracy of the two signal paths.

Both differential and pseudo-differential architectures have been used previously in VCO-based $\Delta\Sigma$ modulators [7], [9]–[11]. Each approach offers the benefit of cancelling much of the even-order nonlinearity. Unfortunately, simulation and

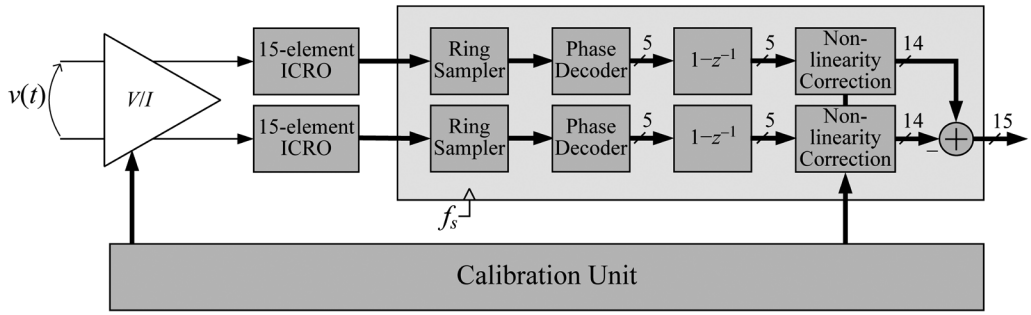

Fig. 4. A pseudo-differential signal path and the calibration unit.

measurement results indicate that the expected matching accuracy of the two signal paths is not sufficient to cancel the worst-case second-order distortion term below about −65 dBc. Furthermore, while the pseudo-differential architecture is better for low voltage operation than the differential architecture, it has the disadvantage that the strong second-order distortion introduced by each ICRO introduces a large error component proportional to the product of the difference and sum of the two ICRO input currents. Therefore, in the absence of second-order nonlinearity correction prior to differencing the two signal paths, any common-mode error on the two ICRO input lines would be converted to a differential-mode error signal. These problems are addressed by having the nonlinearity correction blocks in each signal path correct second-order distortion prior to the differencing operation.

The signal components in the output of the two signal paths have the same magnitudes and opposite signs, whereas the quantization noise and much of the circuit noise in the two outputs are uncorrelated. Therefore, the differencing operation increases the signal by 6 dB and increases the noise by approximately 3 dB, so the SNR of the pseudo-differential signal path is approximately 3 dB higher than that of each individual path.

C. Self-Cancelling Dither Technique

The quantization noise from first-order $\Delta\Sigma$ modulators is notoriously poorly behaved, particularly for low-amplitude input signals [1]. It often contains large spurious tones and can be strongly correlated to the input signal. In theory this problem can be solved by adding a dither sequence to the input of the $\Delta\Sigma$ modulator's quantizer. If the dither sequence is white and uniformly distributed over the quantization step size, it causes the quantizer to be well modeled as an additive source of white noise that is uncorrelated with the input signal [17]. The dither has the same variance and is subjected to the same noise transfer function as the quantization noise so it increases the noise floor of the $\Delta\Sigma$ modulator by no more than 3 dB.

Unfortunately, in a VCO-based $\Delta\Sigma$ modulator there is no physical node at which to add such a dither sequence, because the integration and quantization are implemented simultaneously by the VCO. Another option is to add the dither to the input of the $\Delta\Sigma$ modulator. This has the desired effect on the quantization noise, but severely degrades the signal-band SNR because the dither is not subjected to the $\Delta\Sigma$ modulator's high-pass noise transfer function. While high-pass shaping the dither prior to adding it to the input of the $\Delta\Sigma$ modulator would solve this problem, doing so tends to negate the positive effects of the dither on the quantization noise.

A self-cancelling dither technique is used in this work to circumvent these problems. The idea is to construct the $\Delta\Sigma$ modulator as the sum of two pseudo-differential signal paths each of the form shown in Fig. 4, but with a dither signal added to the input of one of the paths and subtracted from the input of the other path. The overall $\Delta\Sigma$ modulator output is the sum of the two pseudo-differential signal path outputs. The dither causes the quantization noise from each pseudo-differential signal path to be free of spurious tones and uncorrelated with the input signal and it also degrades the signal-band SNR of each pseudo-differential signal path output as described above. However, the dither components that cause the SNR degradation in the output sequences of the two pseudo-differential signal paths have equal magnitudes and opposite polarities, whereas the signal components in the two output sequences are identical, and the noise components in the two output sequences are uncorrelated. Therefore, when the two output sequences are added, the unwanted dither components cancel, the signal components add in amplitude, and the noise components add in power. This results in an SNR that is 3 dB higher than would be achieved by a single pseudo-differential signal path in which the unwanted dither component were somehow subtracted directly. It also doubles the circuit area and power dissipation, the implications of which are discussed shortly.

An advantage of the fine quantization performed by the 15-element ring oscillators is that low-amplitude dither sequences are effective. In this design, approximately 1 dB of dynamic range is used to accommodate the dither sequences.

An alternate approach to the self-cancelling dither technique described above is to add a common-mode dither signal to a single pseudo-differential signal path. The dither would then be cancelled by the pseudo-differential signal path's final differencing operation. The reason this approach was not used is that the second-order distortion correction performed by the nonlinearity correction blocks is not perfect, particularly at frequencies well above the signal band, so the residual second-order error would cause a small but potentially significant differential error term proportional to the product of the input and dither signals.

D. The Implemented $\Delta\Sigma$ Modulator Architecture

Fig. 5 shows a block diagram of the full $\Delta\Sigma$ modulator architecture incorporating the features described above. It consists of two of the pseudo-differential signal paths shown in

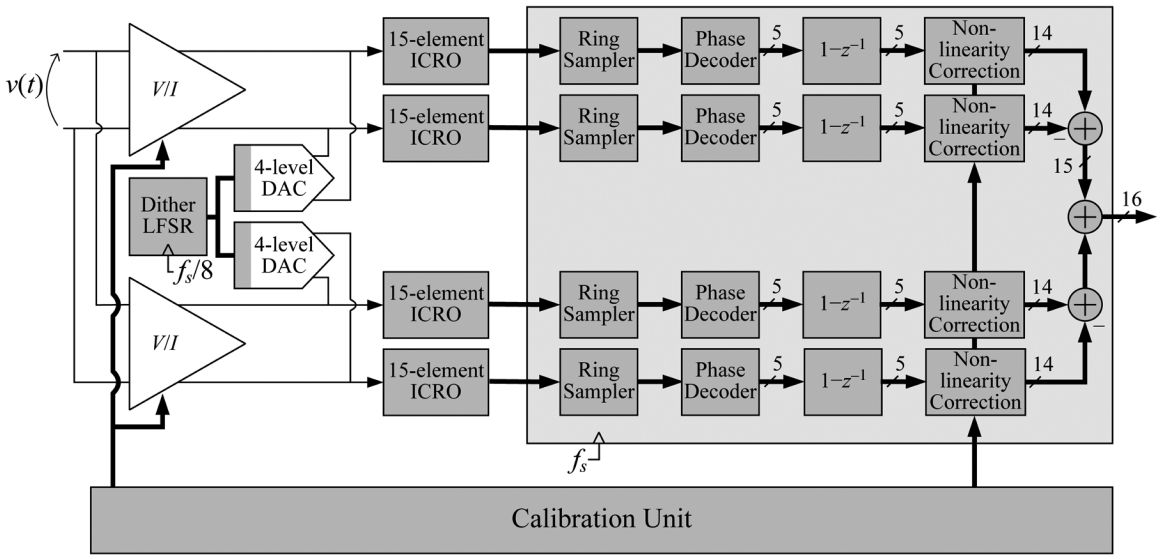

Fig. 5. High-level block diagram of the implemented VCO-based $\Delta\Sigma$ modulator.

Fig. 4, the calibration unit shown in Fig. 3, and a pair of 4-level DACs that add and subtract a pseudo-random dither sequence to and from the top and bottom pseudo-differential signal paths, respectively, The outputs of the two pseudo-differential signal paths are added to form the $\Delta\Sigma$ modulator output sequence.

The input to each dither DAC is a 4-level white pseudo-random sequence with a sample-rate of $f_s/8$. Each dither DAC converts this sequence into a differential current signal with a peak-to-peak range approximately equal to the quantization step-size referred to the inputs of the ICROs. Extensive system-level and circuit-level simulations and measurement results indicate that the dither whitens the noise injected by each ICRO's quantization process sufficiently to meet the target specifications of the $\Delta\Sigma$ modulator, despite having only four levels and an update rate of only $f_s/8$.

As described above, each pseudo-differential signal path has an SNR that is 3 dB higher than that of its two non-differential signal paths, and adding the outputs of the two pseudo-differential signal paths results in a 3 dB improvement in SNR relative to that which could be achieved by a single pseudo-differential signal path. Therefore, compared to a single non-differential signal path, the four signal paths in the $\Delta\Sigma$ modulator consume four times the power and circuit area, but they also result in an SNR improvement of 6 dB. A commonly-used figure of merit for $\Delta\Sigma$ modulators is

$$\mathrm{FOM} = \mathrm{SNDR} + 10\log_{10}\left(\frac{\text{signal bandwidth}}{\text{power dissipation}}\right) \qquad (24)$$

with SNDR in dB. To the extent that the SNDR is noise-limited it follows that the use of multiple signal paths does not degrade the FOM.

E. Quantization Noise, No-Overload Range, and the Number of Ring Elements

As described in Section II, well-known results for the first-order $\Delta\Sigma$ modulator can be applied to the VCO-based $\Delta\Sigma$ modulator [1]. The theoretical maximum signal-to-quantization-noise ratio, $\mathrm{SQNR}_{\max}$, is that of a conventional first-order $\Delta\Sigma$ modulator plus 6 dB to account for the four signal paths and minus 1 dB to account for the reduction in dynamic range required for dither. Hence,

$$\mathrm{SQNR}_{\max} = 20\log_{10}(2M) + 30\log_{10}\left(\frac{f_s}{2B_s}\right) + 1.59 \qquad (25)$$

where M is the number inverters in each ring oscillator (so the number of quantization steps is $2M$), and B_s is the signal bandwidth. The oversampling ratio is defined as $OSR = f_s/(2B_s)$. The no-overload range $\Delta\Sigma$ modulator is the range of input voltages for which (2) is satisfied, so it follows from (1) that the no-overload range is

$$|v(t)| < \frac{\pi f_s}{K_{\mathrm{VCO}}}. \qquad (26)$$

Unlike a conventional $\Delta\Sigma$ modulator, f_s and M in (25) cannot be chosen independently because $f_s = 1/(M\tau_{\mathrm{inv}})$ where τ_{inv} is the nominal delay of each VCO inverter when $v(t) = 0$. For a given inverter topology, τ_{inv} is determined by the speed of the CMOS process. Therefore, to increase f_s for a given design, it is necessary to reduce M proportionally. It follows from (25) that $\mathrm{SQNR}_{\max}$ increases by 3 dB each time f_s is doubled for any given τ_{inv} and B_s. However, increasing f_s has two negative side effects. First, it increases the quantization noise folding described in Section III-A because reducing M causes coarser quantization. Second, it increases the clock rate at which the digital circuitry following the ring oscillators must operate, which increases power consumption. The choice of 15-element ring oscillators for the IC presented in this paper represent was made on the basis of these considerations.

IV. Circuit Details

A. ICRO, Ring Sampler, and Phase Decoder

If the ring oscillator inverters have mismatched rise and fall times or signal-dependent amplitudes, the result is non-uniform

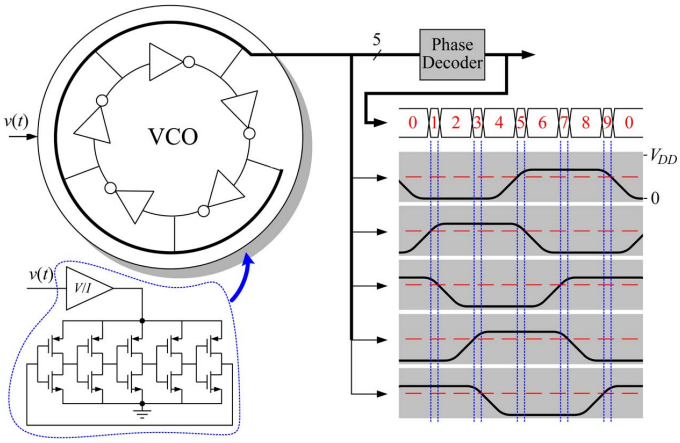

Fig. 6. Example of the signal-dependent non-uniform quantization problem.

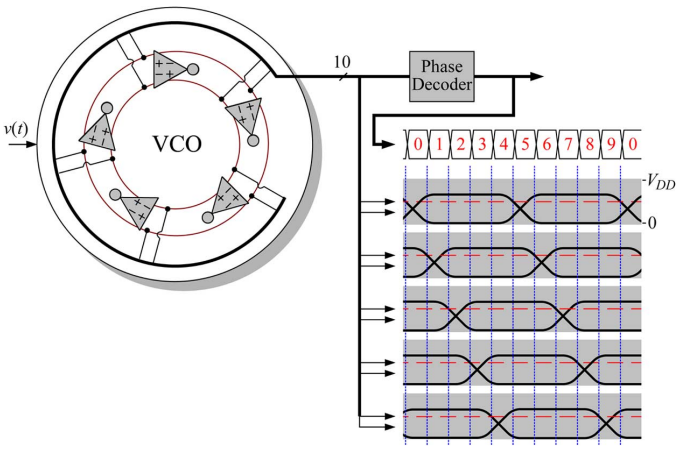

Fig. 7. Example of the solution used to solve the signal-dependent non-uniform quantization problem.

quantization that can cause significant nonlinear distortion which is not corrected by the background calibration technique. The problem is illustrated in Fig. 6 for the case of a 5-element ring oscillator implemented as a V/I converter that drives five current-starved inverters. The output waveform from each inverter is shown for the case of a constant VCO input voltage, i.e., a constant VCO frequency. The transition times and values that the phase decoder output would have if the ring sampler were bypassed are also shown. Each inverter waveform oscillates between a minimum voltage of zero and a maximum voltage that depends on the VCO input voltage. This causes the duration of each inverter's positive transition state to be much shorter than that of its negative transition state. The effect is evident in the non-uniform transition times of the phase decoder output. Since the amount of non-uniformity depends on the VCO's input signal, this phenomenon causes the $\Delta\Sigma$ modulator to introduce strong nonlinear distortion.

The implemented $\Delta\Sigma$ modulator avoids this problem with differential inverters and a modified ring sampler and phase decoder. The concept is illustrated in Fig. 7, again for a 5-element ring oscillator. In this case, each inverter is defined to be in *positive transition* when its positive input voltage and positive output voltage are less than and greater than the digital logic threshold (e.g., half the supply voltage), respectively. Similarly, each inverter is defined to be in *negative transition* when its negative input voltage and negative output voltage are less than and greater than the digital logic threshold, respectively. With these definitions all the conclusions of Section II-B apply to this example. However, unlike the example shown in Fig. 6, the duration of each inverter's positive transition state is the same as that of its negative transition state because each of the times, t_i, occur only when a *falling* output from one of the inverters crosses the logic threshold. Therefore, the transition times of the phase decoder output are uniformly spaced for any given VCO frequency.

This idea can be applied to any ring oscillator with an odd number of elements. In particular, each ICRO in the prototype IC is a ring of 15 current-starved pseudo-differential inverters as shown in Fig. 8. The ring sampler latches the 30 inverter outputs on the rising edge of each f_s-rate clock, and the phase decoder calculates a corresponding instantaneous phase number by identifying which inverter was either in positive or negative transition at the last sample time as described above and in Section II-B.

B. V/I Converter

The V/I converter is shown in Fig. 8. The outputs are from a pair of pMOS cascode current sources in which the gates of the cascode transistors are regulated by the outputs of a fully-differential op-amp, and current proportional to the differential input voltage is injected into the sources of the cascode transistors. To the extent that the op-amp input terminals present a differential virtual ground, the output current variation about the bias current into the top and bottom ICROs is $(1/2)(V_{\text{in}+} - V_{\text{in}-})/R$ and $-(1/2)(V_{\text{in}+} - V_{\text{in}-})/R$, respectively.

The V/I converter operates from a 2.5 V supply, so it consists of all thick-oxide transistors. The op-amp has a telescopic cascode structure with common-mode feedback achieved by sensing the common-mode input voltage. The simulated differential-mode open-loop gain and unity-gain bandwidth of the op-amp are 50 dB and 2.3 GHz, respectively, and the phase margin of the feedback loop is 55 degrees over worst-case process and temperature corners. Two-tone simulations across the 0 to $f_s/2$ frequency band with layout-extracted parasitics indicate that nonlinear distortion from the V/I converter is at least 20 dB less than that of the overall $\Delta\Sigma$ modulator regardless of input signal frequency.

The closed-loop bandwidth of the V/I converter is approximately g_m/C_C, where g_m is the transconductance of the op-amp's differential pair nMOS transistors and C_C is the value of the compensation capacitors. For any given phase margin, C_C depends on the magnitude of the two non-dominant poles at the sources of the pMOS cascode transistors in the op-amp and in the output current sources. These poles are inversely proportional to the intrinsic capacitances of the devices, which ultimately depends on the f_T of the CMOS process. Since g_m is relatively independent of f_T, the closed-loop bandwidth increases as f_T is increased. This implies that if the V/I converter were implemented in a more highly-scaled CMOS process, it could be designed to have a larger closed-loop bandwidth without increasing the current consumption.

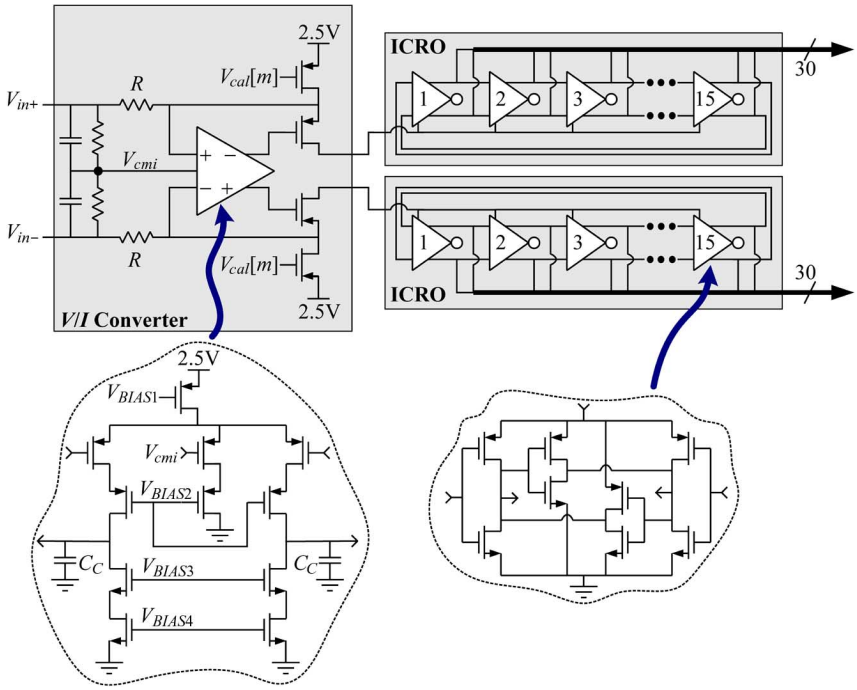

Fig. 8. Circuit diagrams of the V/I converter and ICRO.

The ICRO bias current is controlled by the calibration unit as described in Section III-A. The gate voltage of the pMOS current source, $V_{cal}[n]$, is the drain voltage of a diode connected pMOS transistor connected to an nMOS current-steering DAC driven by the 8-bit output of the VCO center frequency calculator in the calibration unit.

A side benefit of the pseudo-differential architecture is that its cancellation of common-mode circuit noise eliminates the need to filter the ICRO bias voltages. Otherwise large bypass capacitors would have been required as they are in conventional continuous-time $\Delta\Sigma$ modulators that use current steering DACs.

As shown in Fig. 3, the calibration signal bypasses the V/I converter so the digital background nonlinearity correction technique does not cancel nonlinear distortion introduced by the V/I converter. As described above, the V/I converter is sufficiently linear that this is not a problem. Alternatively, an open loop V/I converter without an op-amp could have been used. This would have introduced significant nonlinear distortion, so it would have been necessary to modify the calibration unit to inject the calibration signal into the input of a V/I converter replica. In this case, the V/I converter distortion would be cancelled along with ICRO distortion by the digital background nonlinearity correction technique. One side effect of the this approach is that the dither would have to be added prior to the V/I converters in the actual signal paths. Otherwise they would be subject to distortion that the digital background nonlinearity correction technique would not properly cancel. While this alternative approach is viable, it was not implemented because it would have dictated more complicated DACs for the calibration and dither sequences.

C. Dither DACs

The accuracy of the self-cancelling dither technique described in Section III-C depends on how well the two pseudo-differential signal paths match and how well the two dither DACs match. Mismatches between the pseudo-differential signal paths occur mainly among the ICROs, and simulations predict that such mismatches are so small as to have a negligible effect on the $\Delta\Sigma$ modulator's performance. The dither DACs generate current outputs, so their matching depends on how well multiple switched current sources can be matched, which, in turn, depends on device sizing. Unfortunately, conventional current-steering DACs with sufficient matching accuracy to meet the target specifications would occupy almost half of the total circuit area of the $\Delta\Sigma$ modulator.

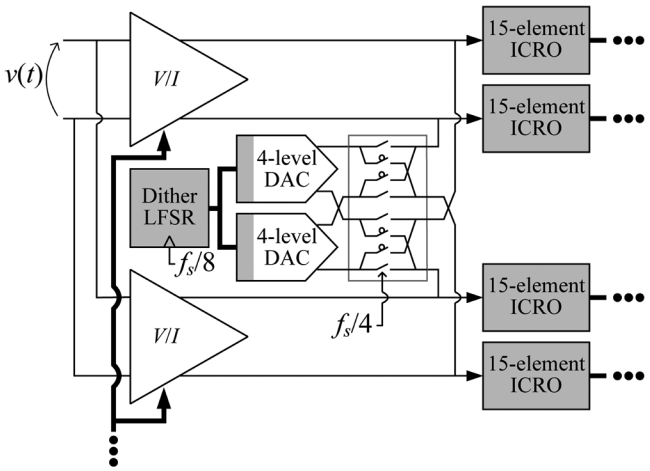

Fig. 9. The dither DAC swapping technique which causes the PSD of the error component in the $\Delta\Sigma$ modulator output arising from mismatches between the dither DACs to have a first-order high-pass shape.

A solution to this problem is shown in Fig. 9. The idea is to use a pair of very small current-steering DACs but suppress the effect of their mismatch error by alternately swapping their roles at twice their update-rate. Therefore, the outputs of each DAC

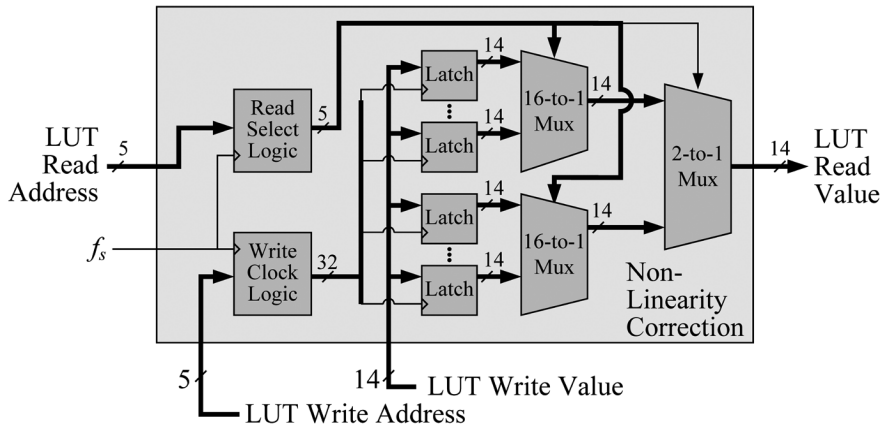

Fig. 10. Nonlinearity correction block details.

are connected to the ICRO inputs in one of the pseudo-differential signal paths for the first half the DAC's update period, and to the ICRO inputs in the other pseudo-differential signal path for the second half of the DAC's update period. It can be verified that this causes the residual dither component in the $\Delta\Sigma$ modulator output sequence arising from DAC mismatches to have a first-order highpass power spectral density. This suppresses the error sufficiently over the $\Delta\Sigma$ modulator's signal band so as to have a negligible effect on the SNR.

A potential problem with non-return-to-zero (NRZ) current steering DACs is that parasitic capacitance at the source coupled node of the current steering cell can cause nonlinear intersymbol interference. The DACs used in this work avoid this problem via the dual return-to-zero (RZ) technique in which a pair of RZ DACs offset from each other by half an update period are interlaced to achieve the combined effect of an NRZ DAC [18].

The architecture described above can be implemented directly as shown in Fig. 9 with the 4-level DACs implemented as RZ DACs. Alternatively, the switches in the swapper cells shown in Fig. 9 can be built into the current steering cells of the RZ DACs. The latter approach is taken in this work. The two implementation methods are equivalent from a signal processing point of view, but the latter results in a more compact circuit with less degradation from non-ideal circuit behavior.

D. Nonlinearity Correction Block

As described in Section III-A, each nonlinearity correction block is a high-speed look-up table (LUT). It maps a 5-bit input sequence to a 14-bit output sequence at a rate of f_s, where f_s can be as high as 1.152 GHz. The details of the block are shown in Fig. 10. The calibration unit loads the 32 14-bit registers with mapping data via the LUT write address and LUT write value lines during the first 32 T_s clock periods once every $2^{28}T_s$. The 5-bit input sequence is used as a LUT read address. Each 5-bit value routes the 14-bit output from the corresponding register to the output.

E. Circuit Noise Sources

The low-pass ring oscillator phase noise is subjected to the high-pass transfer function of the $1-z^{-1}$ blocks, so the resulting contribution to the output sequence in the signal band is nearly white noise. Simulations indicate that in each $\Delta\Sigma$ modulator the V/I converter resistors, V/I converter op-amps, VCO bias current sources, and ICROs together contribute 10 nV/$\sqrt{\text{Hz}}$, 9 nV/$\sqrt{\text{Hz}}$, 10 nV/$\sqrt{\text{Hz}}$, and 9 nV/$\sqrt{\text{Hz}}$, respectively, of noise referred to the input. For a full-scale sinusoidal input signal (800 mV differential peak-to-peak) and a signal bandwidth of 18 MHz, the resulting SNR from thermal noise only is 77 dB. It follows from (25) that for this signal bandwidth $\text{SQNR}_{\max} =$ 76 dB, so the expected peak SNR from thermal and quantization noise together is 73 dB.

The $\Delta\Sigma$ modulator is much less sensitive to clock jitter than conventional $\Delta\Sigma$ modulators with continuous-time feedback DACs because it does not contain feedback DACs. Jitter-induced ring sampler error is suppressed in the signal band because it is subjected to first-order high-pass shaping by the subsequent $1-z^{-1}$ blocks, and jitter-induced errors from the dither DACs largely cancel along with the dither when the outputs of the pseudo-differential signal paths are added. In contrast, jitter-induced error from the feedback DACs in the first stage of a conventional continuous-time $\Delta\Sigma$ modulator is neither high-pass shaped nor cancelled. Most of the published wideband continuous-time $\Delta\Sigma$ modulators use current-steering feedback DACs whose pulse widths and pulse positions are both subject to clock jitter. The jitter mixes high-frequency quantization noise into the signal band, so a very low-jitter clock is necessary so as not to degrade the noise floor of the signal band [3].

V. Measurement Results

The IC was fabricated in the TSMC 65 nm LP process with the deep nWell option and both 1.2 V single-oxide devices and 2.5 V dual-oxide devices, but without the MiM capacitor option. All pads have ESD protection circuitry. The IC was packaged in a 64-pin LFCSP package.

Each IC contains two $\Delta\Sigma$ modulators with a combined active area of 0.14 mm^2. A die photograph of one of the $\Delta\Sigma$ modulators is shown in Fig. 11. The calibration unit area is 0.06 mm^2. The *signal converter*, i.e., the portion of each $\Delta\Sigma$ modulator not including the calibration unit, has an area of 0.04 mm^2. A single calibration unit is shared by the two $\Delta\Sigma$ modulators, so the area per $\Delta\Sigma$ modulator is 0.07 mm^2.

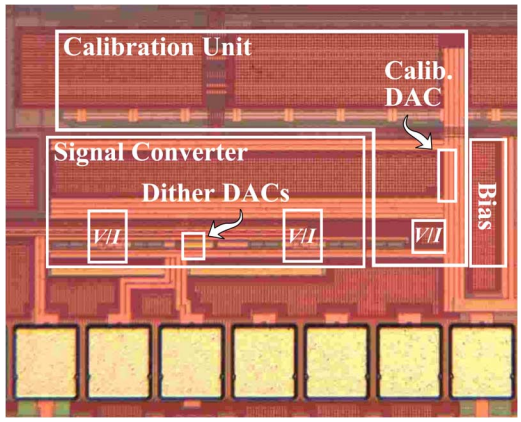

Fig. 11. Die photograph.

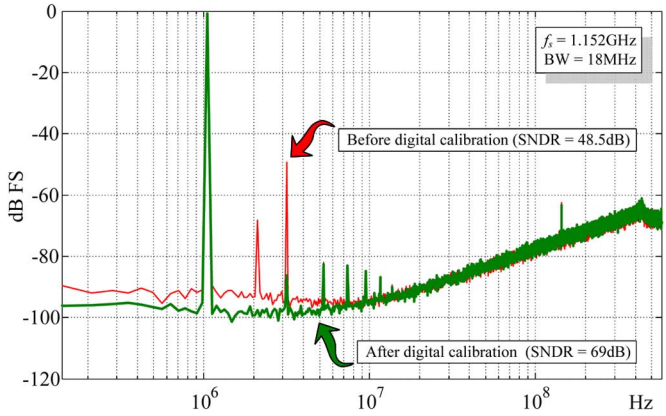

Fig. 12. Representative measured PSD plots of the $\Delta\Sigma$ modulator output before and after digital background calibration (initial convergence time of digital calibration unit is 233 ms).

All components of both $\Delta\Sigma$ modulators are implemented on-chip except for the $f_s/2^{28}$-rate coefficient calculation block within the calibration unit's nonlinearity coefficient calculator block. A schedule problem just prior to tapeout prevented on-time completion of this block so it is implemented off-chip. It has since been laid out for a new version of the IC and found to increase the overall area by 0.004 mm^2 with negligible incremental power consumption because of its low rate of operation.

A printed circuit test board was used to evaluate the IC mounted on a socket. The test board includes input signal conditioning circuitry, clock conditioning circuitry, and an FPGA for ADC data capture and serial port communication. The input conditioning circuitry uses a transformer to convert the single-ended output of a laboratory signal generator into a differential input signal for the IC. The clock conditioning circuitry also uses a transformer. It converts the single-ended output of a laboratory signal generator to a differential clock signal for the IC. Two power supplies provide the 1.2 and 2.5 V power supplies for the IC. The V/I converters operate from the 2.5 V supply, and all other blocks on the IC operate from the 1.2 V supply.

Measurements were performed with a clock frequency, f_s, ranging from 500 MHz to 1.152 GHz. Single-tone and two-tone input signals were generated by high-quality laboratory signal generators and were passed through passive narrow-band bandpass filters to suppress noise and distortion from the signal generators. Each output spectrum presented below was obtained by averaging 4 length-16384 periodograms from non-overlapping segments of $\Delta\Sigma$ modulator output data, and the SNR and SNDR values were calculated from the resulting spectra via the technique presented in [19]. Both $\Delta\Sigma$ modulators on five copies of the IC were tested with no noticeable performance differences.

Fig. 12 shows representative measured output spectra of the $\Delta\Sigma$ modulator for a 0 dBFS, 1 MHz single-tone input signal with $f_s = 1.152$ GHz, both with and without digital background calibration enabled. Without calibration, the SNDR over the 18 MHz signal band is only 48.5 dB because of harmonic distortion and a high noise floor. The high noise floor is the result of common-mode to differential-mode conversion of common-mode thermal noise via the strong second-order distortion introduced by the VCOs as described in Section III-B. With calibration enabled, the SNDR improves to 69 dB. In particular, the second-order term cancels extremely well.

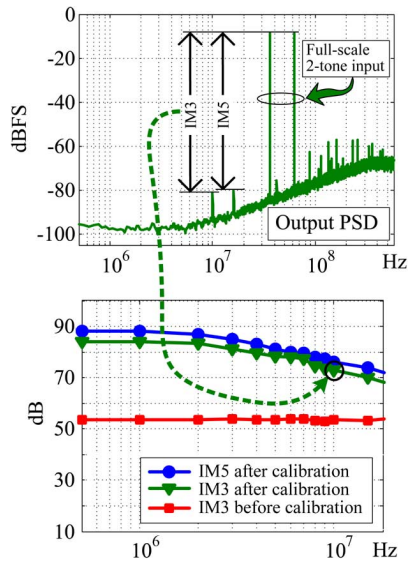

Fig. 13. Plots of the measured output PSD for a two-tone out-of-band input signal (top) and inter-modulation distortion (bottom) for the $\Delta\Sigma$ modulator run with $f_s = 1.152$ GHz. The top and bottom plots indicate how the inter-modulation values were measured.

The measured inter-modulation performance of the $\Delta\Sigma$ modulator with $f_s = 1.152$ GHz is shown in Fig. 13. The top plot shows the measured spectrum of the $\Delta\Sigma$ modulator output for a two-tone out-of-band input signal, and shows the corresponding signal to third-order and fifth-order inter-modulation distortion ratios, denoted as IM3 and IM5, respectively. Measurements indicate that the IM3 and IM5 values depend mainly on the difference in frequency between the two input tones, but not on where in the 576 MHz Nyquist band the two input tones are placed.

The bottom plot in Fig. 13 shows the measured IM3 and IM5 values as a function of the frequencies at which they occur within the signal band. Each value was measured by injecting a full-scale, out-of-band, two-tone input signal into the $\Delta\Sigma$ modulator and measuring the IM3 and IM5 values corresponding to inter-modulation terms within the 18 MHz signal band. For example, the IM3 value measured from the top plot corresponds

TABLE I
PERFORMANCE TABLE AND COMPARISON TO PRIOR STATE-OF-THE-ART $\Delta\Sigma$ MODULATORS

	This Work							Reference [2]	Reference [3]	Reference [4]	Reference [5]
Area (mm^2)	0.07							0.7	1.5	0.45	0.15
Process	65nm							180nm	130nm	130nm	65nm
f_s (MHz)	1152†						500	640	640	900	250
OSR	32			64		128	64	32	16	22.5	12.5
BW (MHz)	18			9		4.5	3.9	10	20	20	20
f_{in} (MHz)	1	2.3	5	1	2.3	1	1	2.4	3.68	2	3.9
SNR (dB)	70	70	70	76	76	80	71.5	84	76	81.2	62
SNDR (dB)	69	67.3	67*	73	72*	77.8*	71*	82	74	78.1	60
Power (mW)	17‡	17	17	17	17	17	8	100	20	87	10.5
FOM**	159	157.5	157*	160	159*	162*	157.9*	162	164	161.7	152.7

† Maximum frequency limited by test board FPGA used for data acquisition
‡ Analog (V/I circuits and DACs): 5 mW, Digital: 12 mW
* Worst-case value over stated BW (SNDR remains unchanged or improves at higher f_{in} values)
** $\text{FOM} \equiv \text{SNDR} + 10\log_{10}(\text{BW}/\text{Power})$

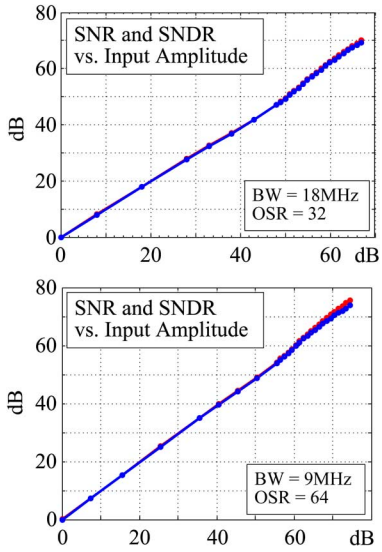

Fig. 14. Plots of the measured SNR and SNDR for an 18 MHz signal band (top) bandwidth 9 MHz signal-band (bottom) for the $\Delta\Sigma$ modulator run with $f_s = 1.152$ GHz.

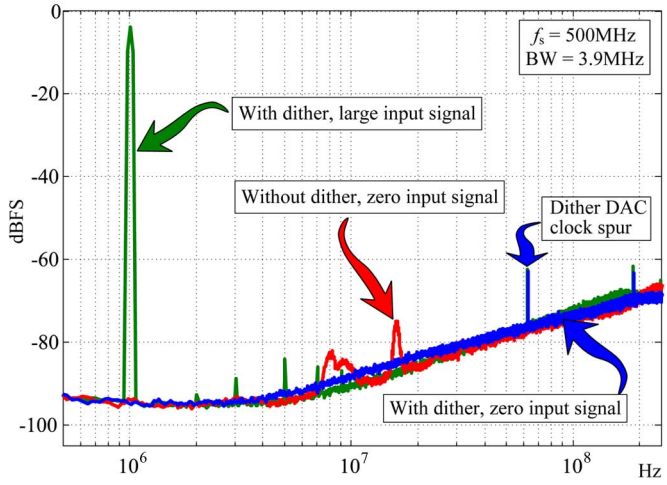

Fig. 15. Representative measured PSD plots of the $\Delta\Sigma$ modulator output with and without dither.

to the circled data point in the bottom plot of Fig. 13. The IM3 values before and after digital calibration are shown. The IM5 values were not measurably affected by digital calibration, so only the IM5 values after calibration are shown.

The low-frequency IM3 of better than 83 dB suggests that the calibration unit does a very good job of measuring third-order distortion for low-frequency inter-modulation products (even when the input tones are well above the signal bandwidth). However, the reduction in IM3 values for inter-modulation products near the high end of the 18 MHz signal band indicate that the third-order distortion coefficient is somewhat frequency dependent. Simulations suggest that this frequency dependence is caused by nonlinear phase shift at the output nodes of the V/I converters. Nevertheless, throughout the maximum signal bandwidth of 18 MHz, the IM3 product is greater than 69 dB.

Fig. 14 shows plots of the SNR and SNDR versus input amplitude for the $\Delta\Sigma$ modulator measured over an 18 MHz signal bandwidth and a 9 MHz signal bandwidth with $f_s = 1.152$ GHz. These signal bandwidths correspond to oversampling ratios of 32 and 64, respectively. The SNR and SNDR for a peak input signal with an oversampling ratio 32 are 70 dB and 69 dB, respectively, and those for an oversampling ratio of 64 are 76 dB and 73 dB. This suggests that quantization noise as opposed to thermal and $1/f$ noise limits performance at the lower oversampling ratio.

As described in Section IV-E a peak SNR of 73 dB was expected over a signal bandwidth of 18 MHz, but as mentioned above the measured SNR over this bandwidth is 70 dB. The authors believe that this discrepancy is caused by non-uniform quantization effects arising from an asymmetric layout of the ICROs. Simulations with parasitics extracted from the layout indicate that this increases the quantization noise by roughly 3 dB and reduces the no-overload range of the $\Delta\Sigma$ modulator by roughly 0.5 dB.

Fig. 15 shows representative measured output spectra of the $\Delta\Sigma$ modulator with f_s reduced to 500 MHz for a large input signal with the dither DACs enabled, and for a zero input signal both with and without the dither DACs enabled. The spectrum

corresponding to the zero input signal with the dither DACs disabled has significant spurious content, as expected. The spectrum corresponding to the zero input signal with the dither DACs enabled indicates that the quantization noise is well-behaved and the dither cancellation process is effective because the noise floor over the signal band does not change as a result of enabling the dither DACs. Clock feed-through from the dither DACs is visible at $f_s/8$, but it lies well outside the signal bandwidth. Similar results to those shown in Fig. 13 occur when f_s is varied between 500 MHz and 1.152 GHz.

Measured results from the prototype IC are summarized relative to comparable state-of-the-art $\Delta\Sigma$ modulators in Table I. As indicated in the table, the performance of the $\Delta\Sigma$ modulator is comparable to the state-of-the-art, but uses significantly less circuit area.

The $\Delta\Sigma$ modulator's performance depends mainly on the digital circuit speed of the CMOS process. As described above, quantization noise, which limits the implemented $\Delta\Sigma$ modulator's performance at low oversampling ratios, scales with the minimum delay through a ring VCO inverter. The V/I converter accounts for less than a third of the total power dissipation, and as described in Section IV-B its bandwidth should increase as f_T increases. Therefore, unlike conventional analog $\Delta\Sigma$ modulators, the $\Delta\Sigma$ modulator architecture described in this paper is likely to yield even better results when implemented in more highly scaled CMOS technology.

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