A Reconfigurable Mostly-Digital ΔΣ ADC with a Worst-Case FOM of 160dB

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Abstract

A 0.075mm^2 65nm CMOS VCO-based ΔΣ modulator ADC that operates from a single 0.9-1.2V supply is presented. Its sample-rate, f_s, is tunable from 1.3-2.4GHz over which the SNDR spans 70-75dB, the bandwidth spans 5-37.5MHz, and the minimum SNDR + 10log(bandwidth/power dissipation) figure of merit (FOM) is 160dB.

Introduction

This paper presents a mostly-digital background-calibrated ΔΣ modulator ADC based on voltage-controlled ring oscillators (VCROs). Its performance is in line with the best ΔΣ modulators published to date, but it occupies much less circuit area, and unlike other high-performance ADCs it is reconfigurable and consists mainly of digital circuitry. It does not use op-amps, analog integrators, feedback DACs, comparators, or reference voltages, so its performance is set by the speed of its digital circuitry and its supply voltage can be scaled with its sample-rate to save power.

The ΔΣ modulator is a next-generation version of that presented in [1] with several enhancements that enable significant performance improvements. The high-level architecture is similar to that presented in [1], so in the following it is described only briefly after which the enhancements are described in more detail.

Architecture Overview

The ΔΣ modulator (Fig. 1) contains a calibration unit and two pseudo-differential VCRO signal paths, each of which contains a pseudo-differential *V*/*I* circuit, a pair of 14-element current-controlled ring oscillators (ICROs), and digital processing blocks. By similar reasoning to that presented in [1] the system is equivalent to a 1st-order ΔΣ modulator with subtractive dither. Look-up-table-based nonlinearity correction (NLC) blocks continuously correct 2nd and 3rd order distortion introduced by the ICROs and (in the case of this work) the *V*/*I* circuits. The on-chip calibration unit (Fig. 2) contains a replica VCRO signal path driven by a four-level pseudo-random calibration sequence. It continuously measures the nonlinearity of the replica path, calculates new look-up data for the NLC blocks every few hundred milliseconds, and adaptively adjusts the center frequency of each ICRO as described in [1].

New Enhancements

Each pseudo-differential *V*/*I* circuit is a pair of source degenerated open-loop common-source amplifiers with the ICROs as loads (Fig. 3). The common-mode input voltage, which sets the center frequency of the ICROs, is set by a DAC in the calibration unit. The *V*/*I* circuit avoids the inherently lower-bandwidth op-amp feedback circuit and 2.5V supply used in [1], but unlike the prior design it introduces significant 2nd and 3rd order nonlinear distortion that must be corrected digitally. This requires the calibration sequence to be added prior to the *V*/*I* circuit in the calibration unit. Unfortunately, this raises a significant practical problem. The dither had to be added after the signal path *V*/*I* circuits for simplicity, so it is subjected to the nonlinearity of the ICROs but not to that of the *V*/*I* circuits. Consequently, intermodulation products of the dither and the *V*/*I* circuit output currents are not completely removed by the NLC blocks. The problem was solved using the multiple VCRO path architecture. It can be shown that the architecture is such that the most significant intermodulation terms are either pairs of differential-mode terms with opposite polarity on the two signal paths or common-mode terms, so they cancel prior to the ΔΣ modulator output. The slight source degeneration of the *V*/*I* circuits provides sufficient linearity that the remaining intermodulation terms are small enough not to limit performance.

Had conventional ICROs been used as in [1], the ΔΣ modulator's quantization step size would have been proportional to the minimum delay through each ICRO inverter, τ, which is IC technology dependent. Instead, each of the ΔΣ modulator's ICROs consists of two 7-element sub-ICROs quadrature-coupled through a resistor network to lock 90^o out of phase with each other (Fig. 3). The 7 pseudo-differential inverter outputs from each of the sub-ICROs are interlaced with those from the other to form the 14 pseudo-differential quadrature-coupled ICRO outputs. The result is equivalent to a 14-element conventional ICRO with a minimum inverter delay of τ/2 rather than τ, so the ΔΣ modulator's quantization noise floor is 6dB below that which would otherwise have been imposed by the IC technology.

A disadvantage of conventional ΔΣ ADCs in applications involving automatic gain control is that they go unstable with long recovery times if their input no-overload ranges are exceeded. The digital over-range correction (ORC) blocks in the VCRO signal paths prevent this problem and extend dynamic range by detecting and compensating for overload-induced phase roll-overs (Fig. 4). The ORC blocks exploit the property that even with relaxed antialias filtering, e.g., one pole at $f_s/(4\pi)$, the phase decoder outputs change by more than 8 quantization steps only when overload-induced phase roll-overs occur. In these cases the ORC blocks unwrap the phase up to the maximum range of the NLC blocks after which they clip.

Measured Results

Each IC (Fig. 7) contains two ΔΣ modulators including all the blocks shown in Figures 1 and 2, a pair of 8-fold CIC decimation filters, and a serial port interface (SPI). The combined area of the two ΔΣ modulators and shared calibration unit is 0.15mm^2. Both ΔΣ modulators on 4 copies of the IC were tested.

Typical measured results are shown in Figures 5-7. Fig. 5 shows measured output PSD plots with and without calibration enabled. Fig 6 shows measured decimation filter output sequences (as opposed to the simulated ΔΣ modulator output sequences shown in Fig. 4) with and without the ORC blocks enabled for an overloading sinusoidal ΔΣ modulator input signal below the clipping level of the ORC blocks with f_s = 2.4GHz. Fig. 7 summarizes measured performance for a typical instance of the ΔΣ modulator for four f_s settings with signal frequencies corresponding to worst-case performance and also shows data for comparable state-of-the-art ΔΣ modulators. The results indicate that the new ΔΣ modulator achieves state-of-the-art FOM performance, yet exceeds the previously published state-of-the-art in terms of area and reconfigurability.

References

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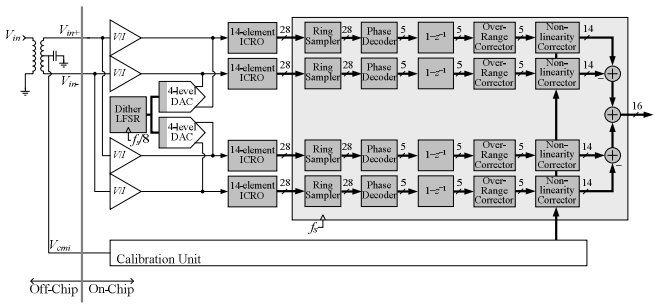


Fig 1: High-level diagram of the ΔΣ modulator and test board input network.

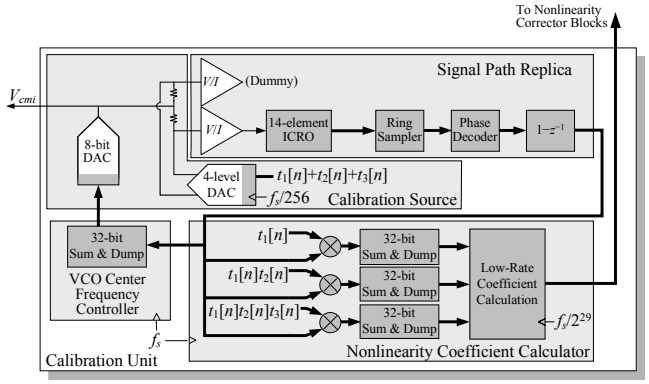


Fig 2: High-level diagram of the Calibration Unit..

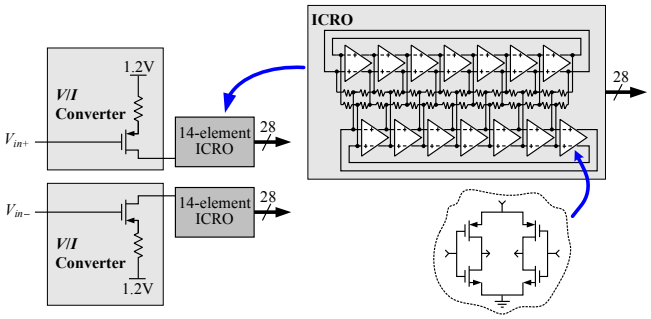


Fig 3: Pseudo-differential *V/I* converter and quadrature-coupled ICRO details.

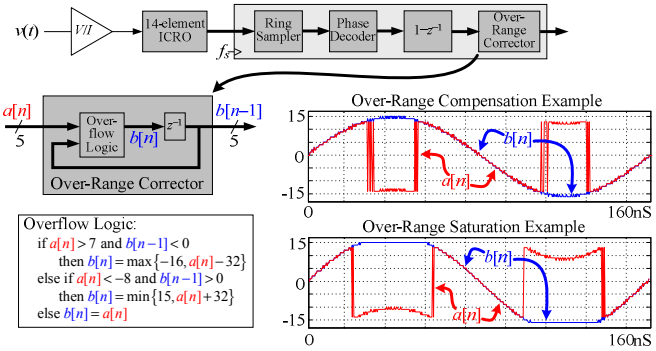


Fig 4: Over-range Corrector Block details.

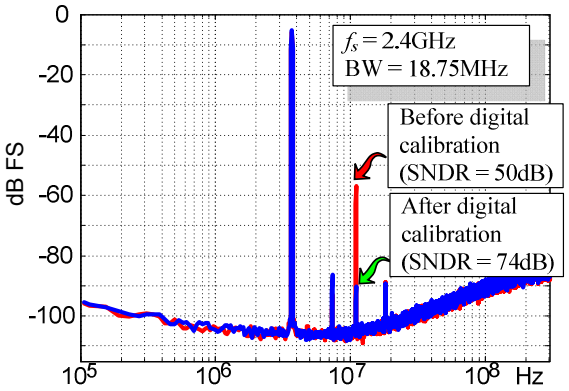


Fig 5: Typical measured output PSD plots with and without calibration enabled for f_s = 2.4GHz.

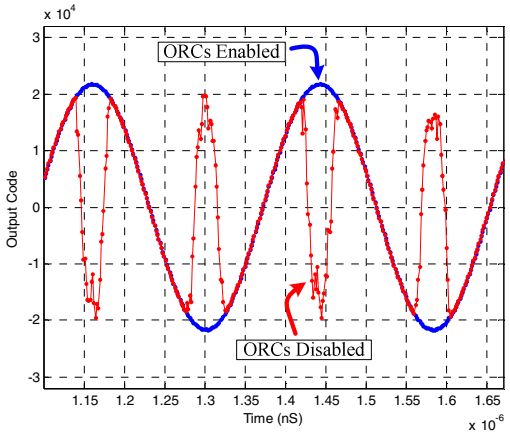
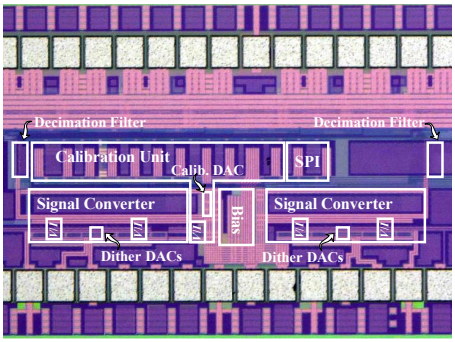


Fig 6: Measured decimation filter output sequences with the ORC blocks enabled and disabled for f_s = 2.4GHz.

	This Work												[1]	[2]	[3]	[4]	[5]	[6]	[7]
Area (mm^2)	0.075												0.07	0.7	1.5	0.45	0.9	0.15	0.4
Process	65nm G+												65nm LP	180nm	130nm	130nm	45nm	90nm	90nm
f_s (MHz)	1300			1600			1920			2400			500	1152	640	640	900	4000	500	640
OSR	128	64	32	128	64	32	64	48	32	64	48	32	64	32	32	16	22.5	16	10	32
BW (MHz)	5.08	10.2	20.3	6.25	12.5	25	15	20	30	18.8	25	37.5	3.9	18	10	20	20	125	25	10
f_{in} (MHz)	1*	1*	3.5*	1*	2.3*	4.9*	2.3*	3.5*	5*	3.5*	4.9*	7.49*	1*	2.3*	2.4	3.68	2	41	2	2
SNR (dB)	76	74	70	76	75	71	75	74	71	76	74	71	71.5	70	84	76	81.2	65.5	64	
SNDR (dB)	75	73	69	75	74	70	74	73	70	74	73	70	71	67.3	82	74	78.1	65	63.5	65
DR (dB)	78	76	71	80	77	72	78	76	72	78	76	73	70	68	84	80	81.2	70	68	67
THD (dB)	81	79	80	82	82	79	81	80	77	79	80	76						74		
SFDR (dB)	82	82	82	83	83	80	82	81	78	81	81	77							81	72
Power Supply (V)	0.9			1.0			1.1			1.2			2.5/1.2	2.5/1.2	1.8	1.2	1.2	1.1/1.8	1.2	1.2
Power Total (mW)	11.5			17.5			26			39			8	17	100	20	87	256	8	6.8
Power Analog (mW)	3			4			5			7			2.5	5						
Power Digital (mW)	8.5			13.5			21			32			5.5	12						
FOM (dB) **	161	162	161	161	163	162	162	162	161	161	161	160	158	158	162	164	162	152	158	157
FOM2 (fJ/conv) ***	246	155	123	305	171	135	212	178	168	254	214	201	354	249	486	122	331	705	131	234



* Worst-case input frequency over stated BW (SNDR remains unchanged or improves with higher f_{in})
** FOM = SNDR + 10 $\log_{10}$(BW/Power)
*** FOM2 = Power / (2·BW·2^{ENOB})

Fig 7: Performance table with comparison to relevant prior ADCs and die photograph.