

# ECEN620: Network Theory Broadband Circuit Design Fall 2025

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## Lecture 14: Limiting Amplifiers (LAs)



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# Announcements

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- Project Preliminary Report (HW5) due Nov 18

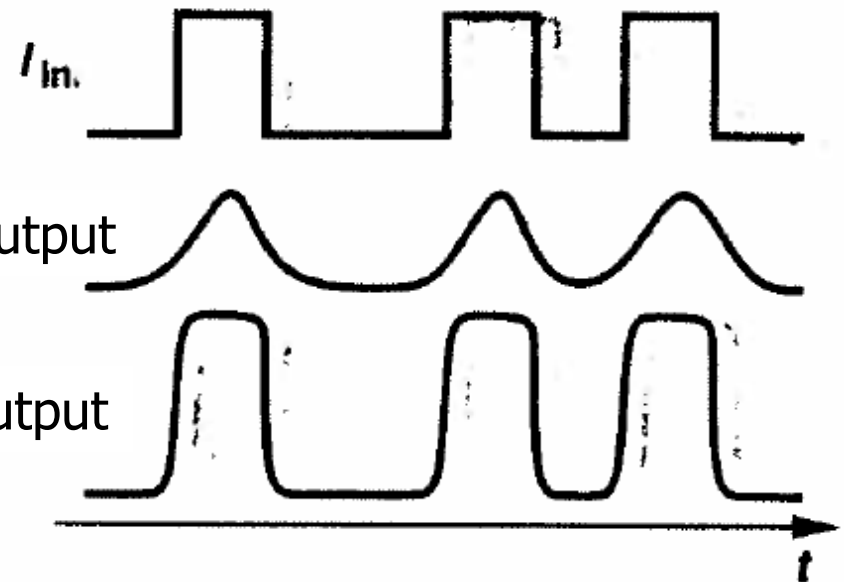
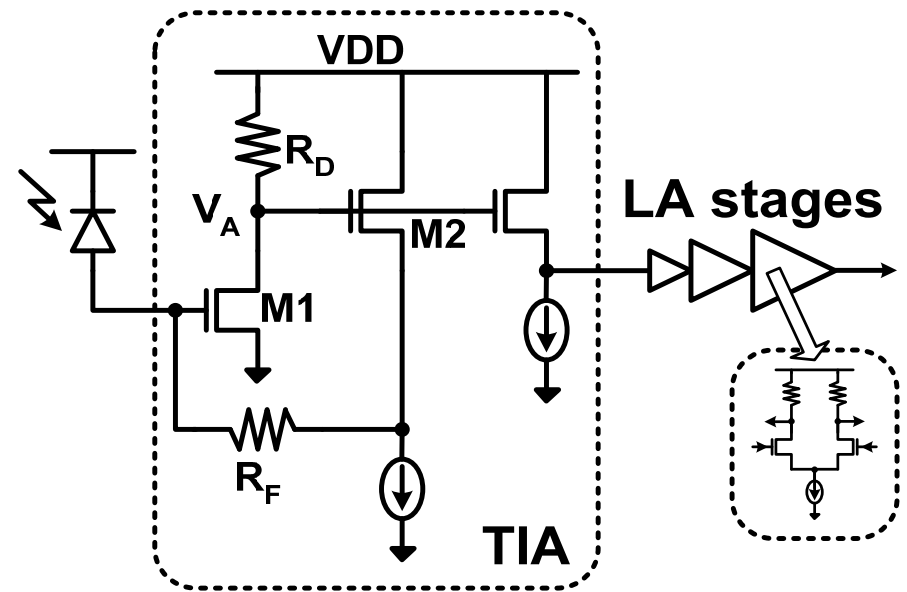
# Agenda

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- Multi-stage limiting amplifiers
- Bandwidth extension techniques
- Offset compensation

# Limiting Amplifiers

- Limiting amplifier amplifies the TIA output to a reliable level to achieve a given BER with a certain decision element (comparator)
- Typically designed with a bandwidth of 1-1.2X data rate
- Want group delay variation  $< \pm 10\%$  over bandwidth of interest to limit DDJ



# How to Achieve an Amplifier $GBW > f_T$ ?

Assume for a 10Gb/s system that we need to build an amplifier with  $A_v = 30dB$  and  $f_{3dB} = 10GHz$ .

$$GBW_{tot} = (31.6)(10GHz) = 316GHz$$

However, the peak  $f_T$  of our technology is only 200GHz, and generally we can only achieve a single - stage amplifier GBW of

$$\text{Max Single - Stage } GBW_s \approx \frac{f_T}{3} = \frac{200GHz}{3} = 66.7GHz$$

$$\text{with } A_v = 30dB \Rightarrow f_{3dB} = \frac{66.7GHz}{31.6} = 2.11GHz, \text{ well below our } 10GHz \text{ spec.}$$

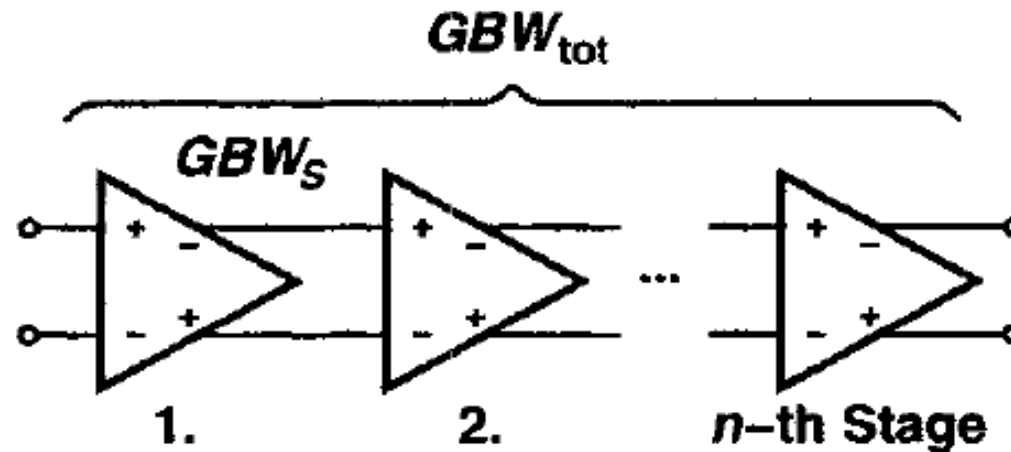
Instead of using a single - stage, let's break the amplifier into multiple stages with lower gain, but higher bandwidth. An optimal choice, from a maximum GBW perspective, is

$$n = 7 \text{ stages, with } A_{vs} = \sqrt[7]{31.6} = 1.64 \text{ and } f_{3dB} = 31GHz, \text{ or } GBW_s = 50.8GHz$$

After multi - stage bandwidth compression, this will yield a total  $GBW \approx 316GHz$

with our target gain of 31.6 and with a single - stage  $GBW_s = 50.8GHz$  that our technology can support.

# Multi-Stage Amplifier GBW



If every stage is a single - pole amplifier

$$\frac{A_{vs}}{1 + \frac{s}{\omega_{3dBs}}}$$

The total multi - stage amplifier transfer function will be

$$\frac{v_{out}}{v_{in}} = \left( \frac{A_{vs}}{1 + \frac{s}{\omega_{3dBs}}} \right)^n = A_{vs}^n \frac{1}{\left( 1 + \frac{s}{\omega_{3dBs}} \right)^n}$$

The gain has increased significantly, but the bandwidth does compress relative to a single stage.

# Multi-Stage Amplifier Bandwidth Compression

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The total amplifier 3 - dB bandwidth,  $\omega_{3dBtot}$ , is where

$$\left| \frac{v_{out}}{v_{in}} \right| = \left| \frac{A}{1 + \frac{j\omega_{3dBtot}}{\omega_{3dBs}}} \right|^n = \frac{A^n}{\sqrt{2}}$$

$$\left( \frac{A_{vs}}{\sqrt{1 + \left( \frac{\omega_{3dBtot}}{\omega_{3dBs}} \right)^2}} \right)^n = \frac{A_{vs}^n}{\sqrt{2}}$$

$$\left( 1 + \left( \frac{\omega_{3dBtot}}{\omega_{3dBs}} \right)^2 \right)^n = 2$$

$$\omega_{3dBtot} = \omega_{3dBs} \sqrt{2^{1/n} - 1}$$

The total multi - stage bandwidth does compress, although at a much slower rate than the increase in gain.

Thus, a significant increase in GBW can be achieved with a multi - stage amplifier approach.

# Optimum Number of Gain Stages

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Assuming that there is a maximum per - stage  $GBW_s$  that the technology can support

$$GBW_s = A_{vs} \omega_{3dBs} \Rightarrow \omega_{3dBs} = \frac{GBW_s}{A_{vs}} \quad (\text{Note, here GBW is in rad/s})$$

If we need to achieve a high bandwidth, we have to reduce the per - stage gain and increase the number of stages. However, the bandwidth will compress with cascaded stages. Thus, there must be an optimum number of stages for a maximum potential gain bandwidth.

Recall that the total bandwidth is

$$\omega_{3dBtot} = \omega_{3dBs} \sqrt{2^{1/n} - 1} = \frac{GBW_s}{A_{vs}} \sqrt{2^{1/n} - 1}$$

and we will achieve a total gain  $G_{tot}$  with n stages

$$A_{vs} = G_{tot}^{1/n} \Rightarrow \omega_{3dBtot} = \frac{GBW_s}{G_{tot}^{1/n}} \sqrt{2^{1/n} - 1}$$

# Optimum Number of Gain Stages

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For a given total gain, we would like to maximize the bandwidth. In order to do this, let's make the following approximation

$$\omega_{3dBtot} = \frac{GBW_s}{G_{tot}^{1/n}} \sqrt{2^{1/n} - 1} \approx \frac{GBW_s}{G_{tot}^{1/n}} \sqrt{\frac{1}{n} \ln 2}$$

Also, instead of maximizing this expression, let's minimize its reciprocal w.r.t the number of stages

$$\frac{1}{\omega_{3dBtot}} = \left( \frac{\sqrt{n}}{GBW_s \sqrt{\ln 2}} \right) G_{tot}^{1/n}$$
$$\frac{d}{dn} \left( \frac{1}{\omega_{3dBtot}} \right) = \frac{d}{dn} \left( \left( \frac{\sqrt{n}}{GBW_s \sqrt{\ln 2}} \right) G_{tot}^{1/n} \right) = 0$$

Moreover, to make this easier, let's minimize the natural log of the denominator, as this should yield the same optimum.

$$\frac{d}{dn} \left( \ln \left( \frac{1}{\omega_{3dBtot}} \right) \right) = \frac{d}{dn} \left( \ln \left( \left( \frac{\sqrt{n}}{GBW_s \sqrt{\ln 2}} \right) G_{tot}^{1/n} \right) \right) = \frac{d}{dn} \left( \frac{1}{2} \ln(n) + \frac{1}{n} \ln(G_{tot}) - \ln(GBW_s \sqrt{\ln 2}) \right) = 0$$

# Optimum Number of Gain Stages

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$$\frac{d}{dn} \left( \ln \left( \frac{1}{\omega_{3dBtot}} \right) \right) = \frac{d}{dn} \left( \ln \left( \left( \frac{\sqrt{n}}{GBW_s \sqrt{\ln 2}} \right) G_{tot}^{1/n} \right) \right) = \frac{d}{dn} \left( \frac{1}{2} \ln(n) + \frac{1}{n} \ln(G_{tot}) - \ln(GBW_s \sqrt{\ln 2}) \right) = 0$$

$$\frac{1}{2n} - \frac{1}{n^2} \ln(G_{tot}) = 0$$

$$\frac{1}{n} \ln(G_{tot}) = \frac{1}{2}$$

Thus, the optimum number of stages is

$$n_{opt} = 2 \ln(G_{tot})$$

and the optimum stage gain is

$$A_{vs,opt}^{2 \ln(G_{tot})} = G_{tot}$$

$$2 \ln(G_{tot}) \ln(A_{vs,opt}) = \ln(G_{tot})$$

$$A_{vs,opt} = \sqrt{e} = 1.65$$

# Optimum Number of Gain Stages

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For example, a multi - stage amplifier with  $G_{tot} = 100$  should have

$$n_{opt} = 2\ln(G_{tot}) = 2\ln(100) = 9.21$$

Assuming 9 stages results in

$$A_{vs} = \sqrt[9]{100} = 1.67$$

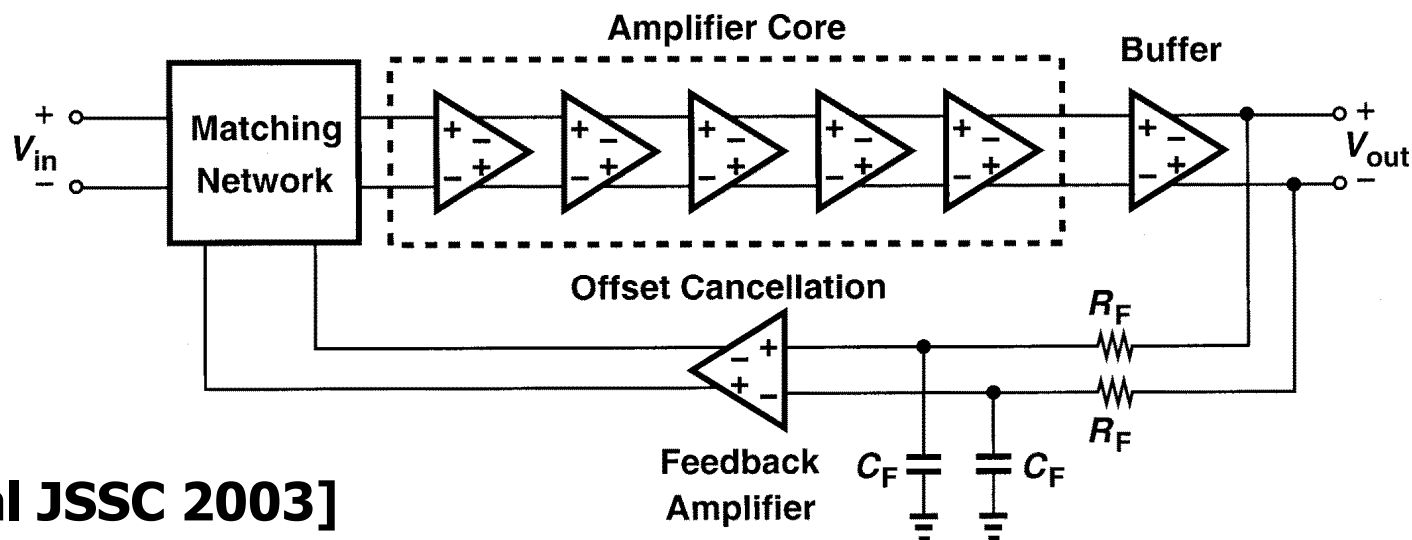
which is close to  $\sqrt{e} = 1.65$

Relative to the per - stage bandwidth, the total amplifier bandwidth will compress to

$$\omega_{3dBtot} = \omega_{3dBs} \sqrt{2^{1/9} - 1} = 0.283\omega_{3dBs}$$

# Optimum Number of Gain Stages

- Note, while this is the optimum number of stages from a maximum GBW perspective, the bandwidth doesn't falloff too dramatically with lower  $n$
- Thus, from a power and noise perspective, it may make sense to use a lower number of LA stages
- Typically high-gain LAs use between 3-7 stages



[Galal JSSC 2003]

# Agenda

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- Multi-stage limiting amplifiers
- Bandwidth extension techniques
- Offset compensation

# Bandwidth Extension Techniques

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- In order to increase the bandwidth of our multi-stage amplifiers, we need to increase the bandwidth of the individual stages
- Passive bandwidth extension techniques
  - Shunt Peaking
  - Series Peaking
  - T-coil Peaking
- An excellent reference

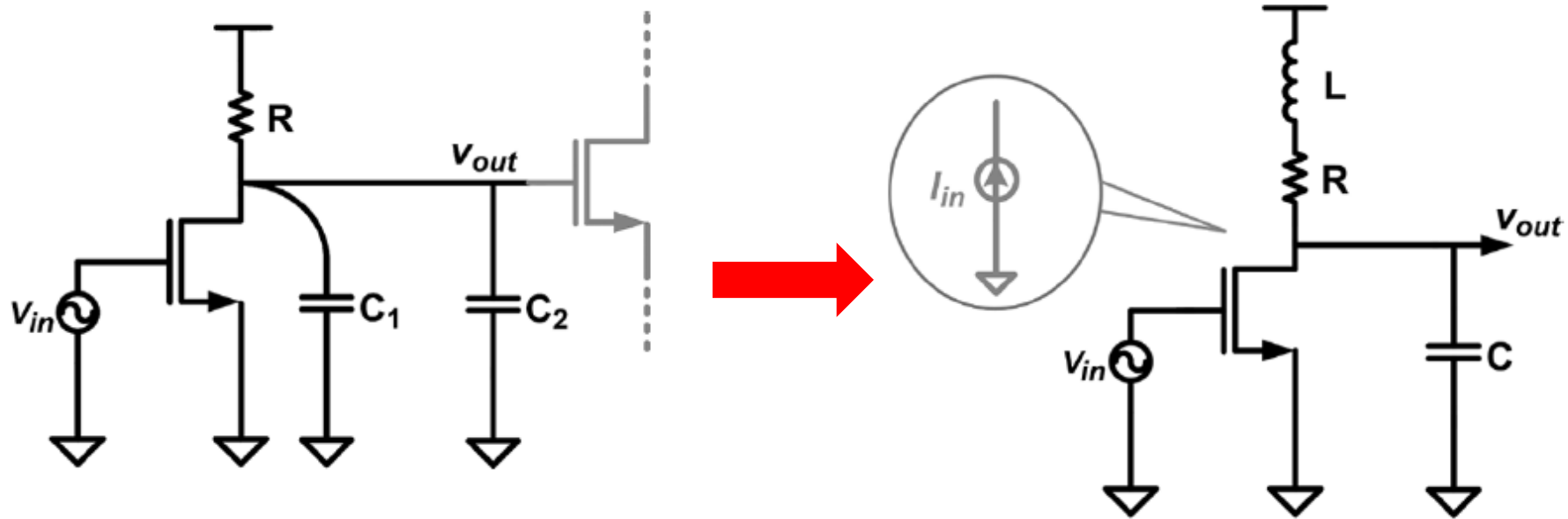
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IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 11, NOVEMBER 2006

## Bandwidth Extension Techniques for CMOS Amplifiers

Sudip Shekhar, *Student Member, IEEE*, Jeffrey S. Walling, *Student Member, IEEE*, and David J. Allstot, *Fellow, IEEE*

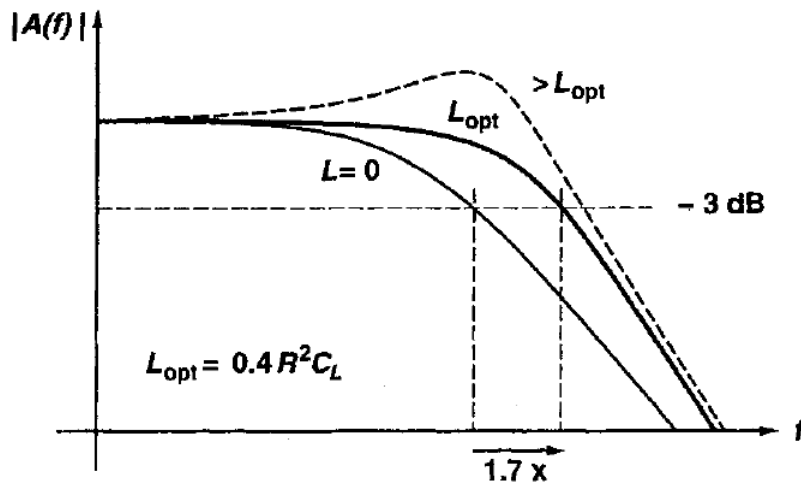
# Shunt Peaking



$$Z(s) = \frac{V_{out}}{I_{in}} = \left( \frac{1}{sC} \right) \parallel (R + sL) = \frac{R + sL}{1 + sRC + s^2LC}$$

- Adding an inductor in series with the load resistor introduces a zero in the impedance transfer function
- This zero increases the impedance with frequency, compensating the decrease caused by the capacitor, and extending the bandwidth

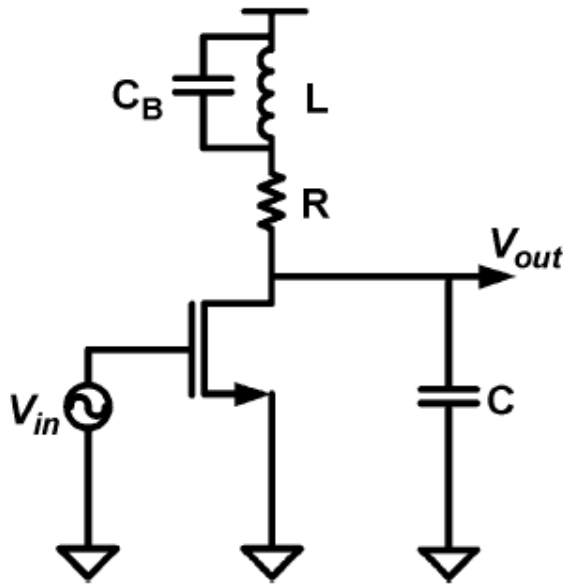
# Shunt Peaking



- While the inductor can increase the bandwidth significantly, frequency peaking can occur if the inductor is too big
- For a flat frequency response,  $\sim 70\%$  bandwidth increase can be achieved
- A maximum 85% bandwidth increase is possible with 1.5dB of peaking

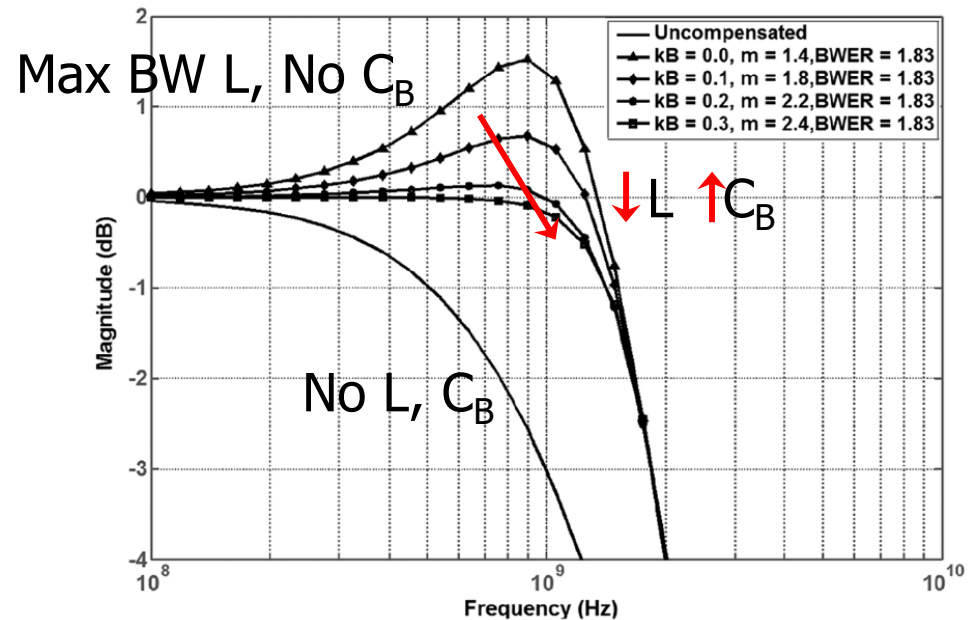
Condition	Ratio of $\left(\frac{RC}{L/R}\right)$ time constants $\rightarrow m = R^2C/L$	Normalized bandwidth	Normalized peak frequency response
Maximum bandwidth	$\sim 1.41$	$\sim 1.85$	1.19
$ Z  = R @ \omega = 1/RC$	2	$\sim 1.8$	1.03
Maximally flat frequency response	$\sim 2.41$	$\sim 1.72$	1
Best group delay	$\sim 3.1$	$\sim 1.6$	1
No shunt peaking	$\infty$	1	1

# Bridged-Shunt Peaking



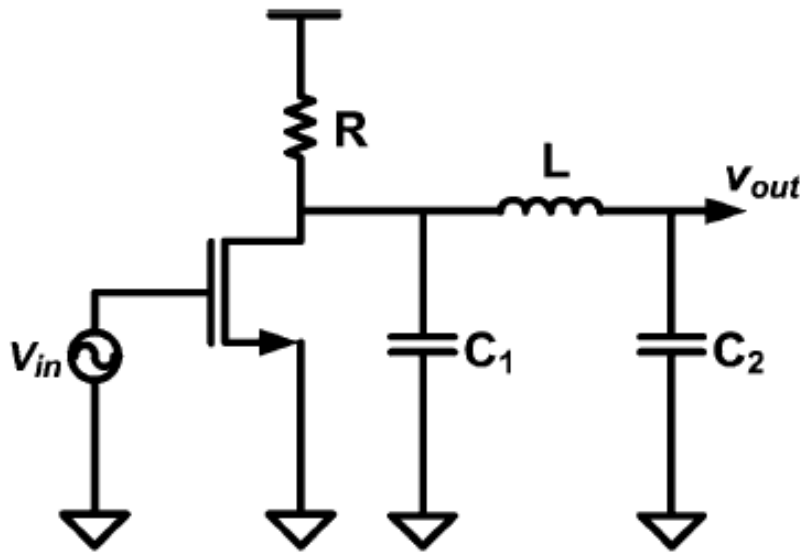
$$Z_N(s) = \frac{1 + \left(\frac{1}{m}\right) \frac{s}{\omega_0} + \left(\frac{k_B}{m}\right) \frac{s^2}{\omega_0^2}}{1 + \frac{s}{\omega_0} + \left(\frac{k_B + 1}{m}\right) \frac{s^2}{\omega_0^2} + \left(\frac{k_B}{m}\right) \frac{s^3}{\omega_0^3}}$$

$$k_B = C_B/C, \omega_0 = 1/RC, \text{ and } m = R^2C/L$$



- Adding a bridge capacitor in parallel with the inductor allows for compensation of the frequency peaking with the possible maximum shunt peaking bandwidth increase
- A real inductor will always have some parasitic  $C_B$ , and thus  $k_B$  will be  $>0$  in practice even without an extra cap

# Series Peaking

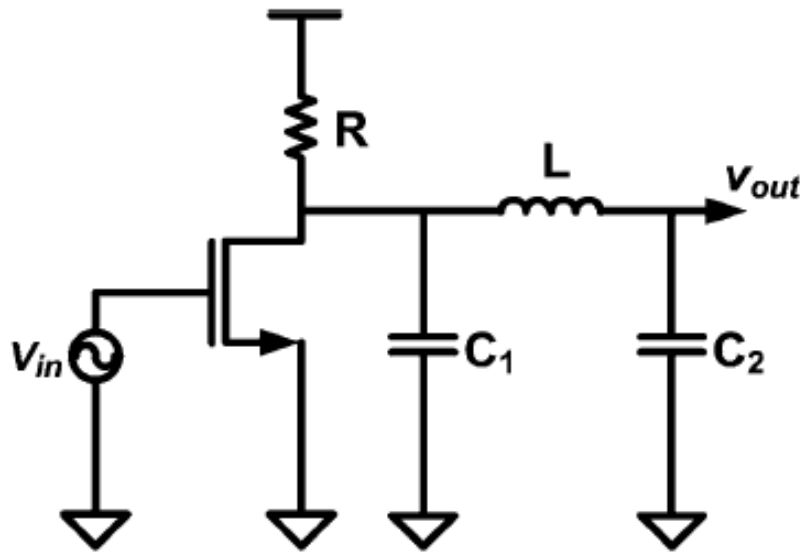


$$Z_N(s) = \frac{1}{1 + \frac{s}{\omega_0} + \left(\frac{1 - k_C}{m}\right) \frac{s^2}{\omega_0^2} + \left(\frac{k_C(1 - k_C)}{m}\right) \frac{s^3}{\omega_0^3}}$$

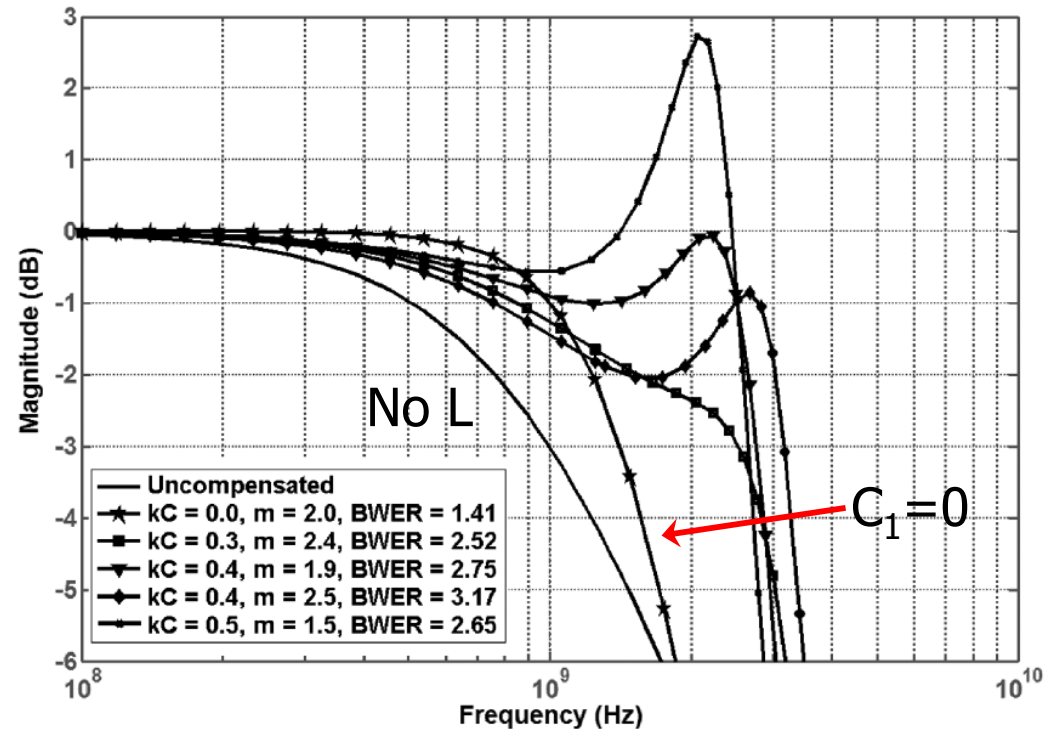
$$k_C = C_1/C \quad m = R^2C/L$$

- Introducing a series peaking inductor is useful to “split” the load capacitance between the amplifier drain capacitance and the next stage gate capacitance
- Without L, the transistor has to charge the total capacitance at the same time
- With L, initially only  $C_1$  is charged, reducing the risetime at the drain and increasing bandwidth

# Series Peaking



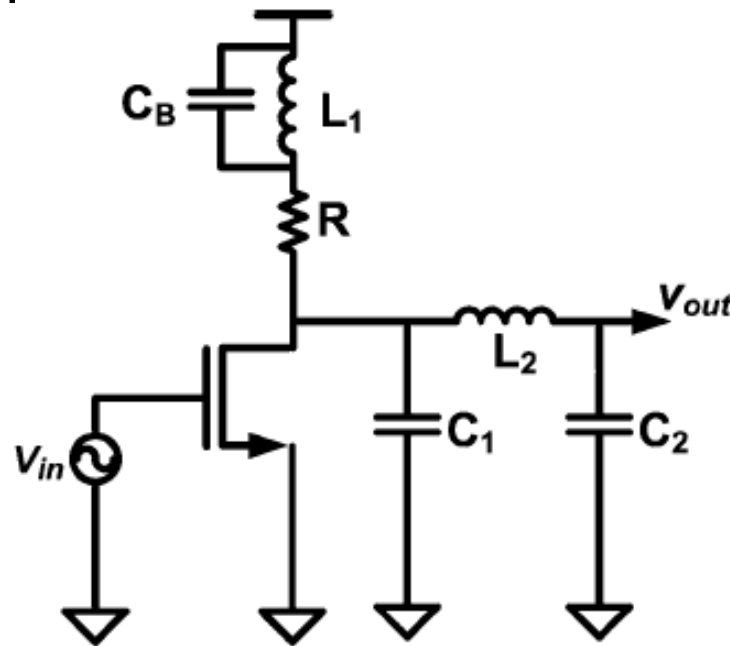
- As the capacitance is more distributed with a higher  $k_C$  value, a higher BWER is achieved
- Up to 2.5x bandwidth increase is achieved with no peaking
- Higher BWER is possible with some frequency peaking



$k_C = C_1/C$	Ripple (dB)	$m = R^2 C / L$	BWER
0	0	2	1.41
0.1	0	1.8	1.58
0.2	0	1.8	1.87
0.3	0	2.4	2.52
0.4	1	1.9	2.75
	2	2.5	3.17
0.5	3.3	1.5	2.65

# Bridged-Shunt-Series Peaking

- Combining both shunt and series peaking can yield even higher bandwidth extension

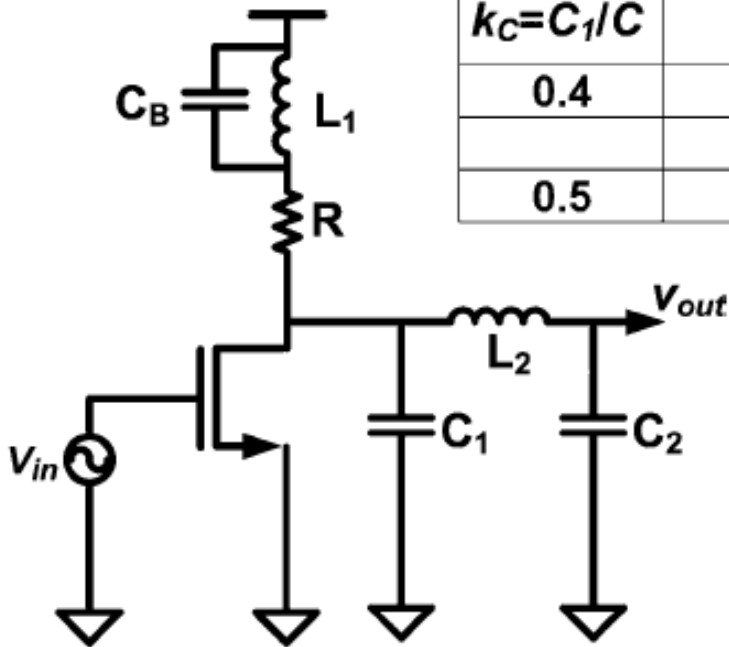


$$Z_N(s) = \frac{1 + \left(\frac{1}{m_1}\right) \frac{s}{\omega_0} + \left(\frac{k_B}{m_1}\right) \frac{s^2}{\omega_0^2}}{1 + \frac{s}{\omega_0} + \left(\frac{1+k_B}{m_1} + \frac{1-k_C}{m_2}\right) \frac{s^2}{\omega_0^2} + \left(\frac{k_B}{m_1} + \frac{k_C(1-k_C)}{m_2}\right) \frac{s^3}{\omega_0^3} + \left(\frac{(k_C+k_B)(1-k_C)}{m_1 m_2}\right) \frac{s^4}{\omega_0^4} + \left(\frac{k_B k_C(1-k_C)}{m_1 m_2}\right) \frac{s^5}{\omega_0^5}}$$

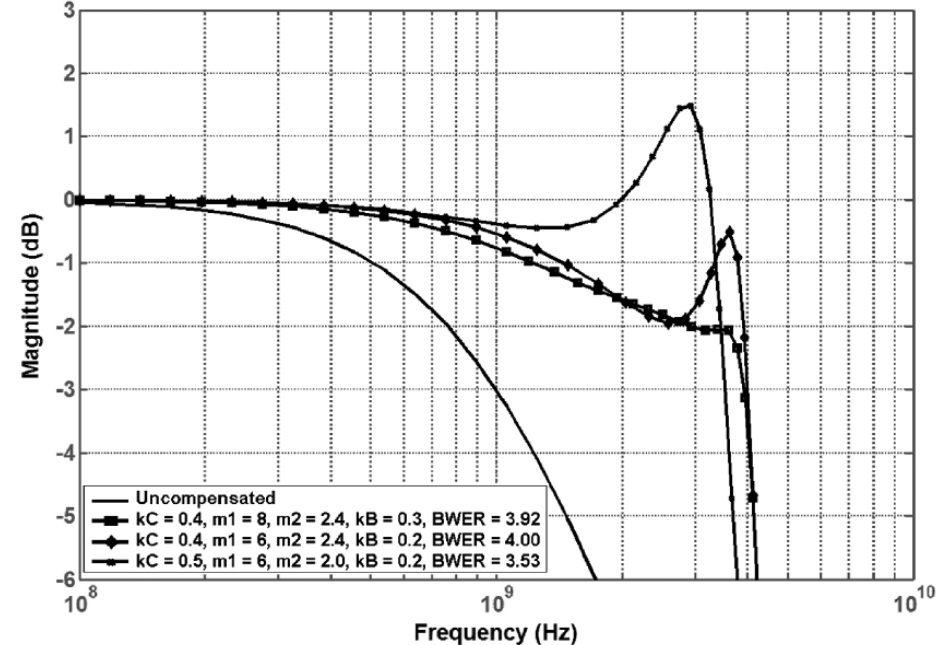
$$m_1 = R^2 C / L_1$$

$$m_2 = R^2 C / L_2$$

# Bridged-Shunt-Series Peaking



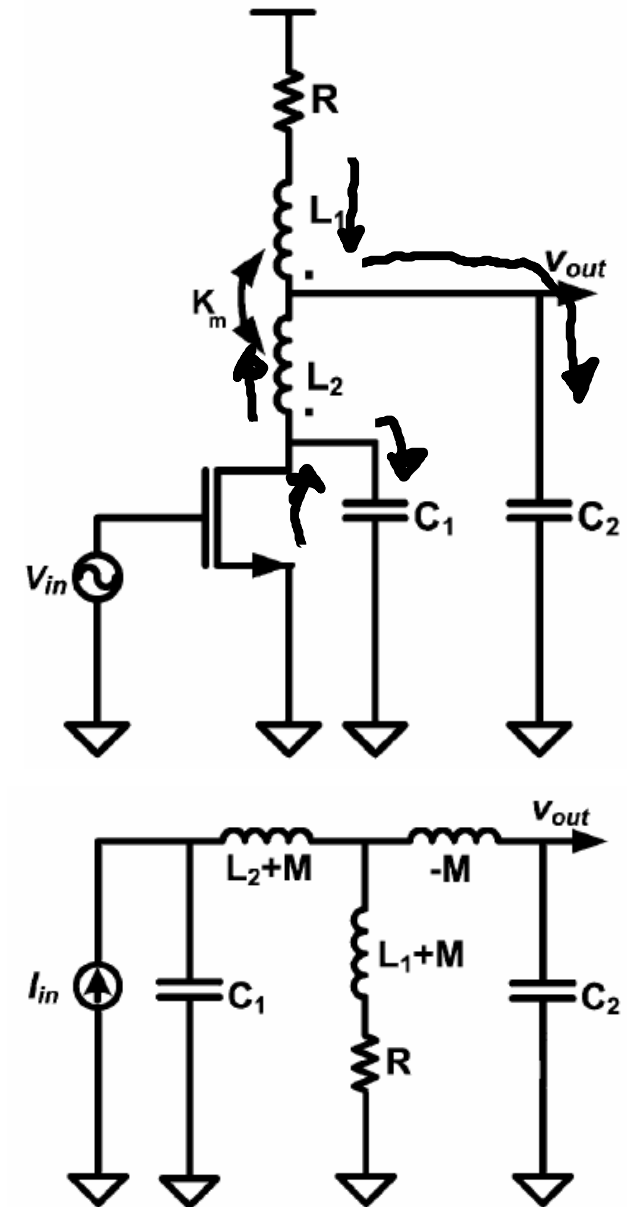
$k_C=C_1/C$	Ripple (dB)	$m_1=R^2C/L_1$	$m_2=R^2C/L_2$	$k_B=C_B/C$	BWER
0.4	0	8	2.4	0.3	3.92
	2	6	2.4	0.2	4
0.5	2	6	2	0.2	3.53



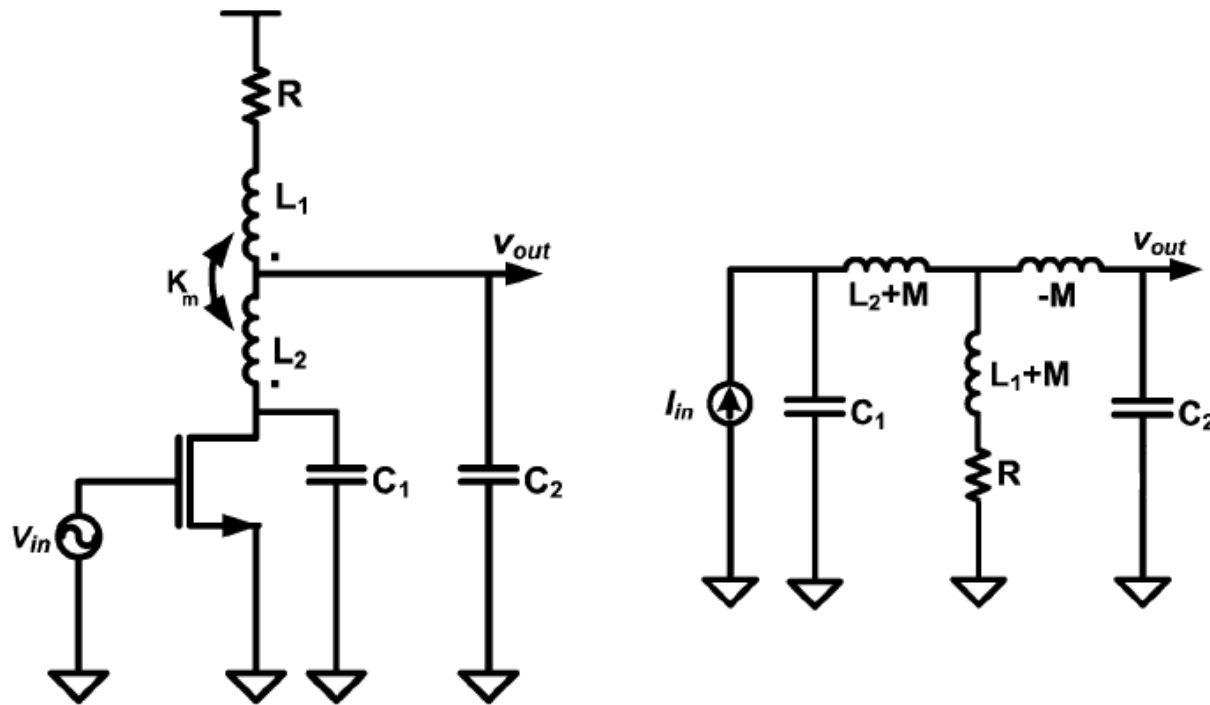
- Proper choice of component values can yield close to 4x increase in bandwidth with no peaking
- However, this requires tight control of these components, which can be difficult with PVT variations

# T-Coil Peaking

- If the input transistor drain capacitance ( $C_1$ ) is relatively small, then the bandwidth extension through shunt-series peaking is limited
- T-coil peaking, which utilizes the magnetic coupling of a transformer, provides better bandwidth extension in this case
  - $L_2$  performs capacitive splitting, such that the initial current charges only  $C_1$
  - As current begins to flow through  $L_2$ , magnetically coupled current also flows through  $L_1$ , providing increased current to charge  $C_2$  which improves bandwidth and transition times



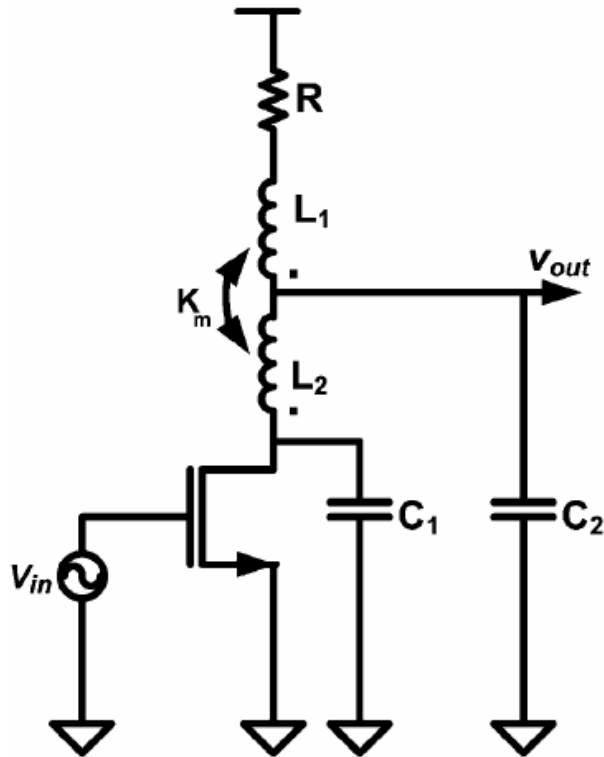
# T-Coil Peaking



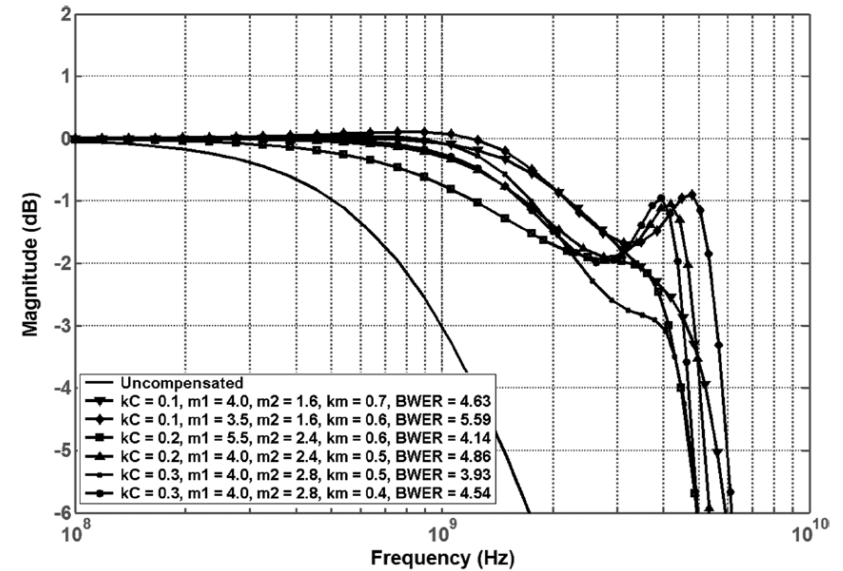
$$Z_N(s) = \frac{1 + \left( \frac{1}{m_1} + \frac{k_m}{\sqrt{m_1 m_2}} \right) \frac{s}{\omega_0}}{1 + \frac{s}{\omega_0} + \left( \frac{1}{m_1} + \frac{k_C}{m_2} + \frac{2k_C k_m}{\sqrt{m_1 m_2}} \right) \frac{s^2}{\omega_0^2} + \left( \frac{k_C(1 - k_C)}{m_2} \right) \frac{s^3}{\omega_0^3} + \left( \frac{k_C(1 - k_C)(1 - k_m^2)}{m_1 m_2} \right) \frac{s^4}{\omega_0^4}}$$

$$k_m = M / \sqrt{L_1 L_2}$$

# T-Coil Peaking



- A bandwidth extension of 4x is possible without any frequency peaking
- If peaking is acceptable, then a BWER near 5 can be achieved, depending on the size of  $C_1$



$k_C = C_1/C$	Ripple (dB)	$m_1 = R^2 C_1 L_1$	$m_2 = R^2 C_1 L_2$	$k_m = M / \sqrt{L_1 L_2}$	BWER
0.1	0	4	1.6	-0.7	4.63
	1	3.5	1.2	-0.6	4.92
	2	3.5	1.6	-0.6	5.59
0.2	0	5.5	2.4	-0.6	4.14
	1	3	2	-0.6	4.51
	2	4	2.4	-0.5	4.86
0.3	0	4	2.8	-0.5	3.93
	1	3.5	2	-0.4	3.98
	2	4	2.8	-0.4	4.54

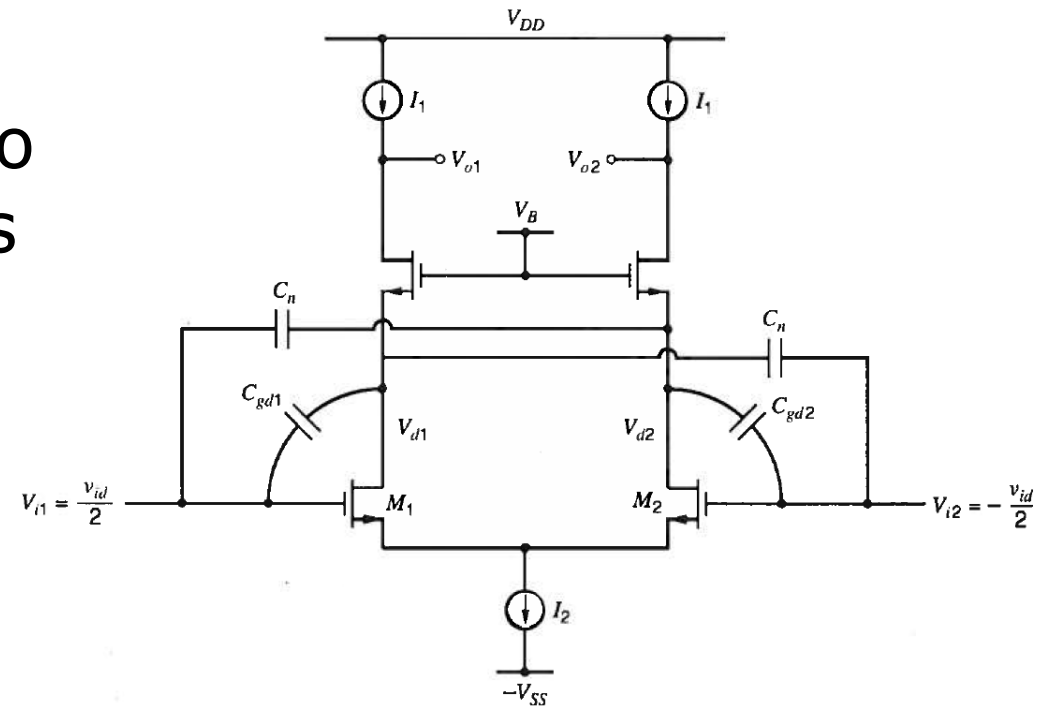
# Active Bandwidth Extension Techniques

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- While passive techniques offer excellent bandwidth extension at near zero power cost, there are some disadvantages
  - Generally large area
  - Process support/characterization of inductors/transformers
- Active circuit techniques can also be employed to extend amplifier bandwidth
- Some active bandwidth extension techniques
  - Negative Miller Capacitance
  - Active Negative Feedback
- There are numerous other techniques, but that is all we have time for this semester 😊

# Negative Miller Capacitance

- In modern technologies,  $C_{gd}$  is a significant (50% to near 100%) fraction of  $C_{gs}$
- Amplifier effective input capacitance can increase significantly due to the Miller multiplication of  $C_{gd}$
- Without additional  $C_n$ :

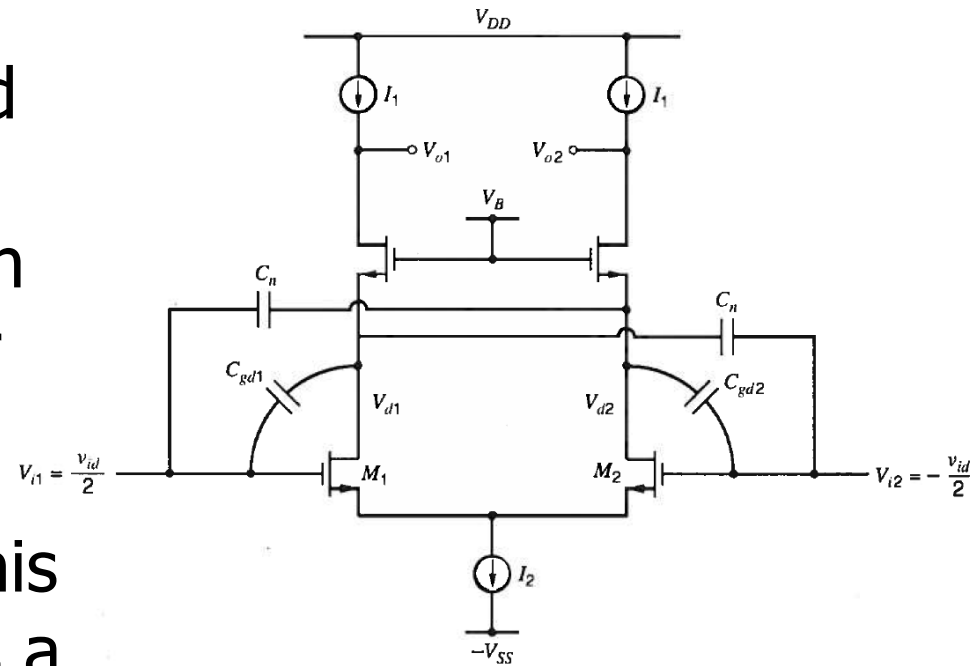


$$C_{in} = C_{gs1} + C_{gd1}(1 - A_{gd})$$

As  $A_{gd}$  is negative, and often is the differential gain of the amplifier, this can result in significant increase in the effective input capacitance

# Negative Miller Capacitance

- In order to mitigate this  $C_{gd}$  multiplication, additional cross-coupled capacitors can be added from the amplifier inputs to the outputs
- Effectively, the charge on this additional capacitor charges a (large) portion of the  $C_{gd}$  capacitor



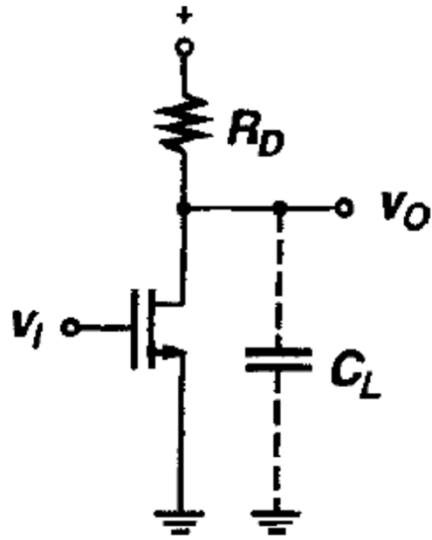
$$C_{in} = C_{gs1} + C_{gd1}(1 - A_{gd}) + C_n(1 - (-A_{gd}))$$

If  $C_n$  is set equal to  $C_{gd1}$

$$C_{in} = C_{gs1} + 2C_{gd1}$$

Thus, as long as the amplifier gain is  $> 1$ , a reduction in the effective input capacitance is achieved

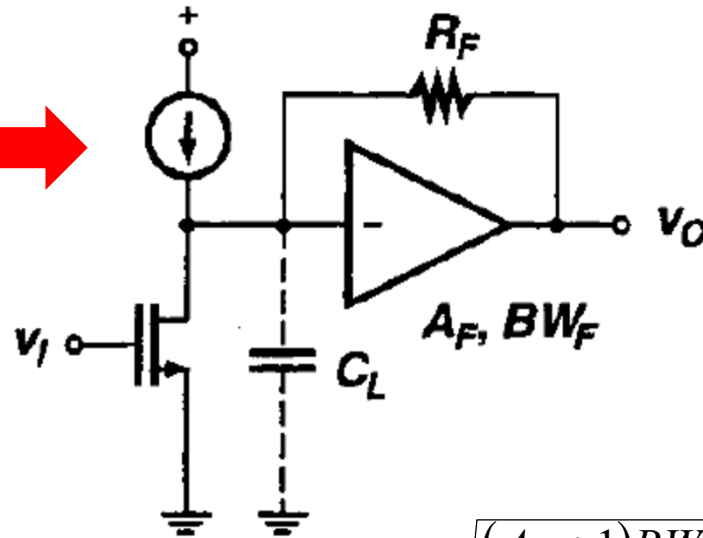
# TIA Load



$$A_v = -g_m R_D$$

$$C_{in} = C_{gs} + C_{gd}(1 + g_m R_D)$$

$$\omega_p = \frac{1}{R_D C_L}$$



$$\omega_o = \sqrt{\frac{(A_F + 1)BW_F}{R_F C_L}}$$

$$Q = \sqrt{\frac{(A_F + 1)R_F C_L \left(\frac{1}{BW_F}\right)}{R_F C_L + \frac{1}{BW_F}}}$$

$$A_v = -g_m Z_T(s)$$

$$Z_T(s) = \frac{\left(\frac{R_F A_F}{1 + A_F}\right)}{1 + \frac{s}{\omega_o Q} + \frac{s^2}{\omega_o^2}}$$

with a Butterworth response, can show that

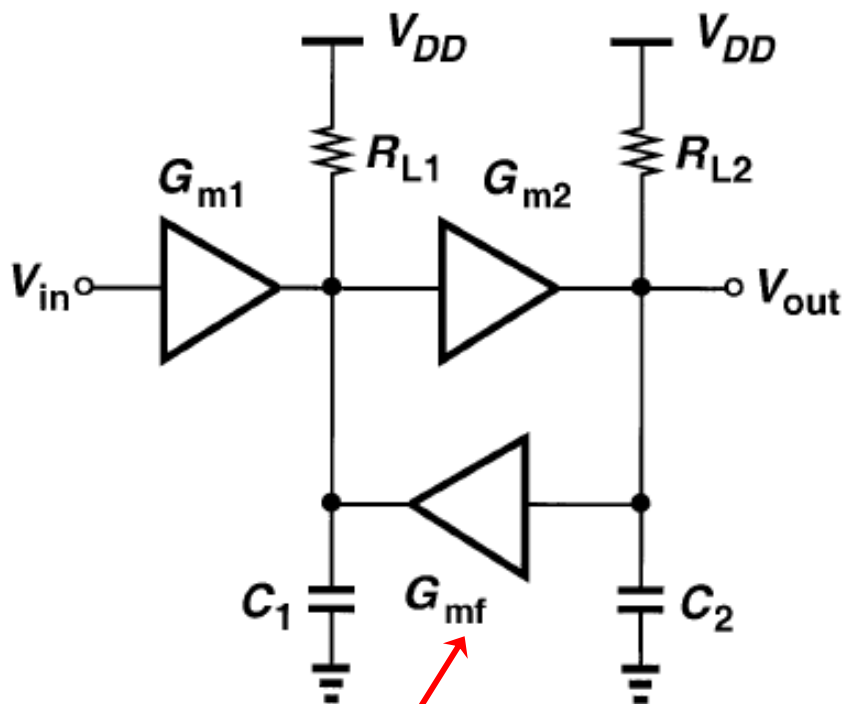
$$\omega_{3dB} \approx \frac{\sqrt{A}}{R_D C_L} \text{ for the same gain.}$$

$$C_{in} = C_{gs} + C_{gd} \left(1 + \frac{g_m R_D}{A_F}\right)$$



# Active Negative Feedback

- Instead of using simple first-order amplifier cells, a second-order cell with active negative feedback can provide bandwidth enhancement



**Inverting**

$$\frac{V_{out}}{V_{in}} = \frac{A_{vo}\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

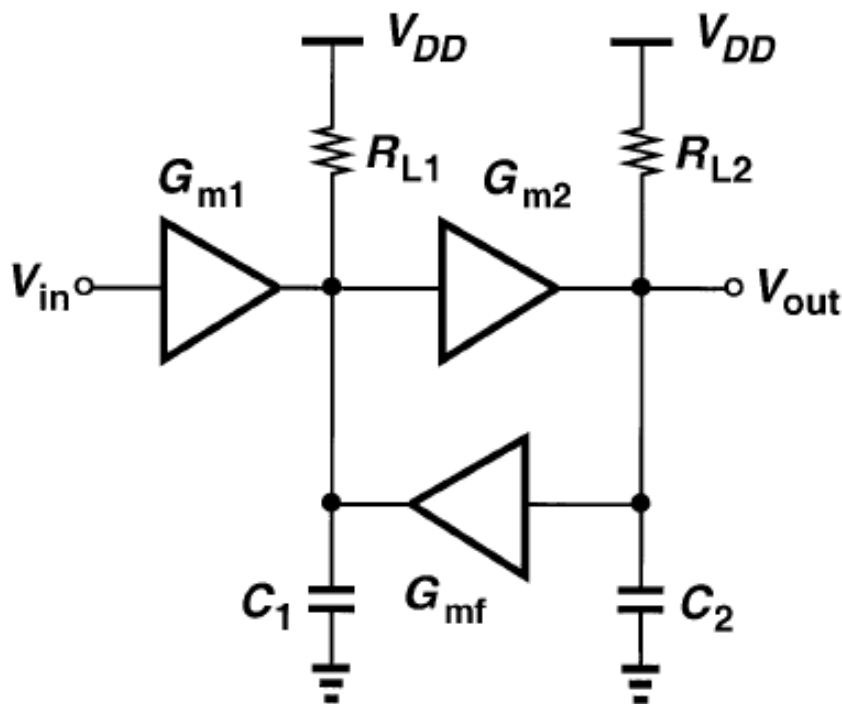
$$A_{vo} = \frac{G_{m1}G_{m2}R_{L1}R_{L2}}{1 + G_{m2}G_{mf}R_{L1}R_{L2}}$$

$$\zeta = \frac{1}{2} \frac{R_{L1}C_1 + R_{L2}C_2}{\sqrt{R_{L1}R_{L2}C_1C_2(1 + G_{mf}G_{m2}R_{L1}R_{L2})}}$$

$$\omega_n^2 = \frac{1 + G_{mf}G_{m2}R_{L1}R_{L2}}{R_{L1}R_{L2}C_1C_2}$$

# Active Negative Feedback

- This second-order amplifier cell can be optimized for different objectives, but  $G_{mf}$  can be set to yield a Butterworth response with a maximally-flat frequency response



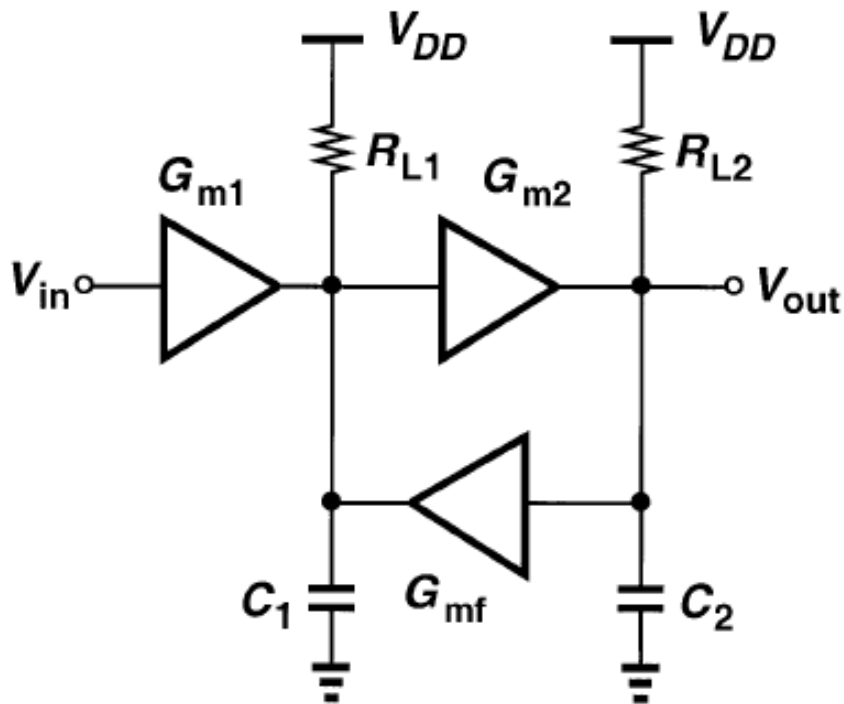
$$\zeta = \sqrt{2}/2$$

$$\omega_{-3dB} = 2\pi f_{-3dB} = \omega_n / (2\pi)$$

$$A_{vo}\omega_{-3dB}^2 = \frac{G_{m1}G_{m2}}{C_1C_2}$$

$$A_{vo}\omega_{-3dB} = \frac{G_{m1}G_{m2}}{C_1C_2} \frac{1}{\omega_{-3dB}}$$

# Active Negative Feedback



$$A_{vo}\omega_{-3dB} = \frac{G_{m1}G_{m2}}{C_1C_2} \frac{1}{\omega_{-3dB}}$$

The ratio  $\frac{G_m}{C}$  is proportional to the technology  $\omega_T$

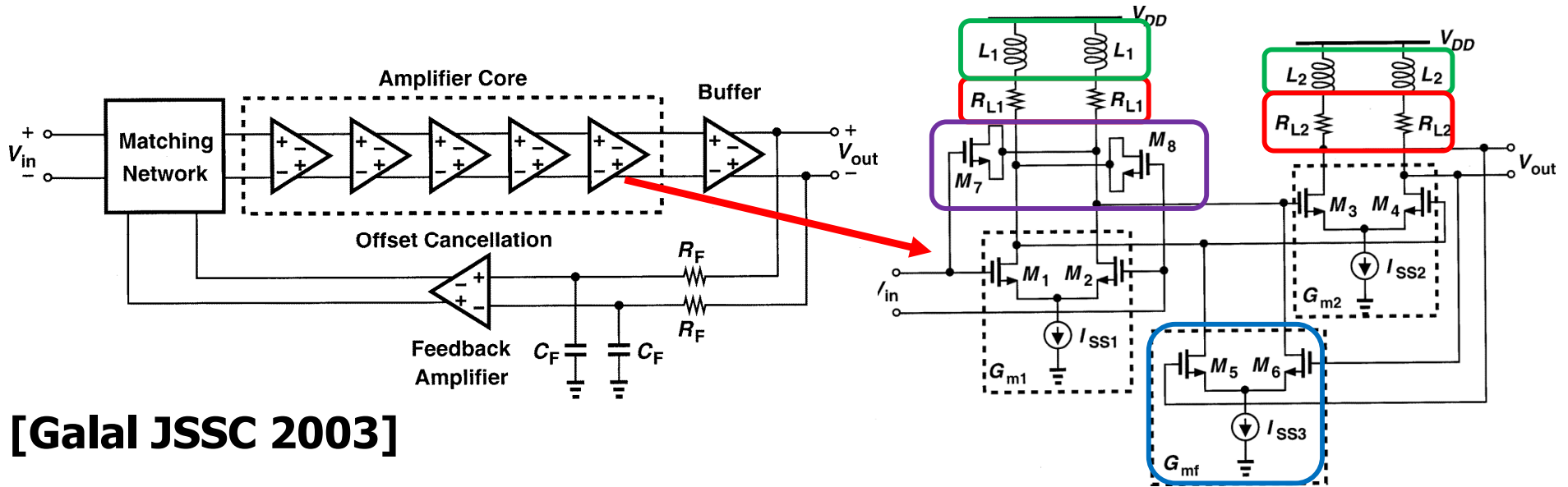
$$\frac{G_m}{C} = \alpha\omega_T$$

Assuming  $\frac{G_{m1}}{C_1} \approx \frac{G_{m2}}{C_2} \approx \alpha\omega_T$

$$A_{vo}\omega_{-3dB} = \frac{(\alpha\omega_T)^2}{\omega_{-3dB}} = \alpha^2\omega_T \frac{\omega_T}{\omega_{-3dB}}$$

- The second-order cell gain-bandwidth can potentially achieve a value greater than the technology  $f_T$

# Limiting Amplifier Example 1



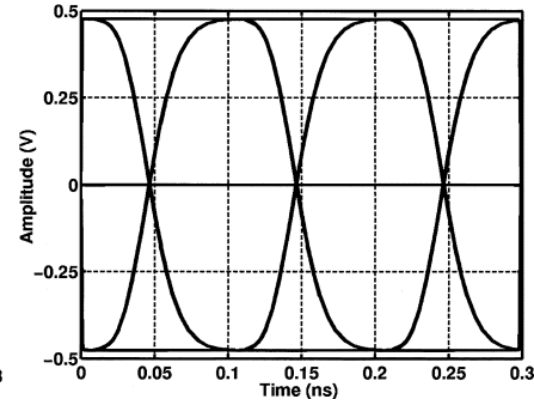
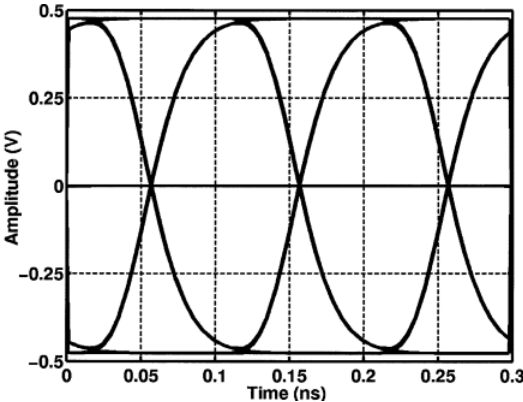
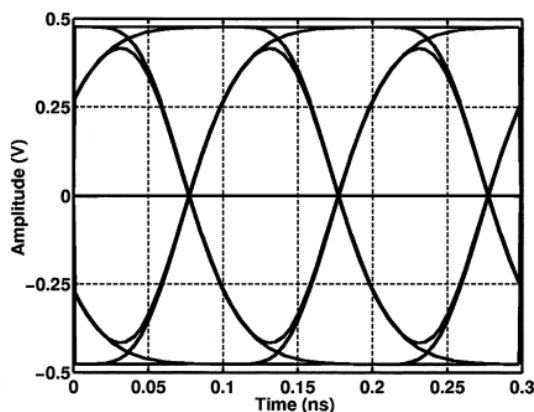
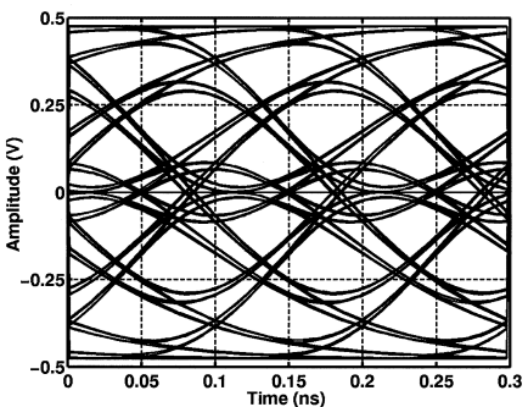
[Galal JSSC 2003]

**Resistive Load Only**

**Active Negative Feedback**

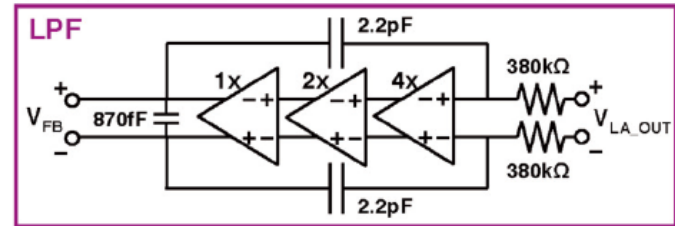
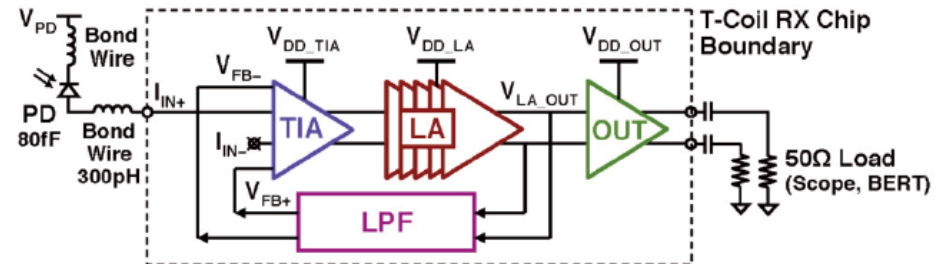
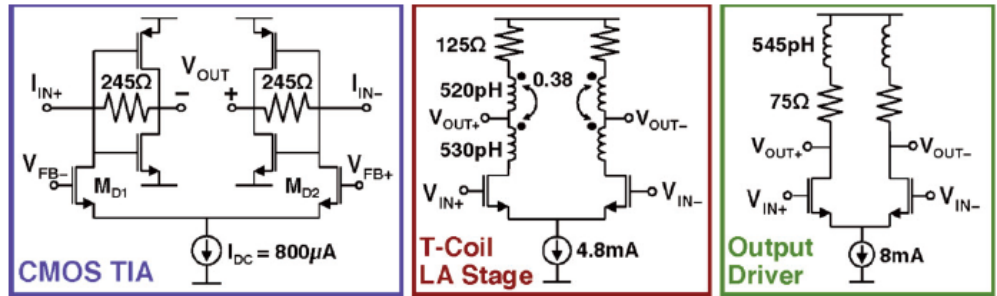
**Shunt Inductive Peaking**

**Negative Miller Capacitance**

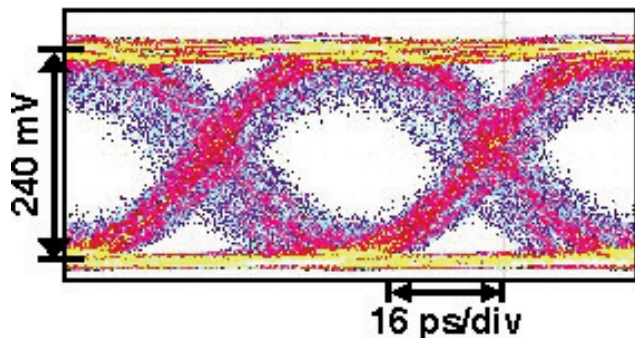


# Limiting Amplifier Example 2

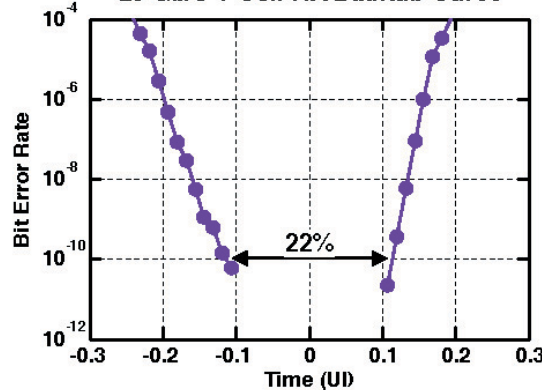
- T-coils in LA stages allow for a combination of series and shunt peaking and close to 3x bandwidth extension



25 Gb/s T-Coil RX Eye



25 Gb/s T-Coil RX Bathtub Curve



[Proesel ISSCC 2012]

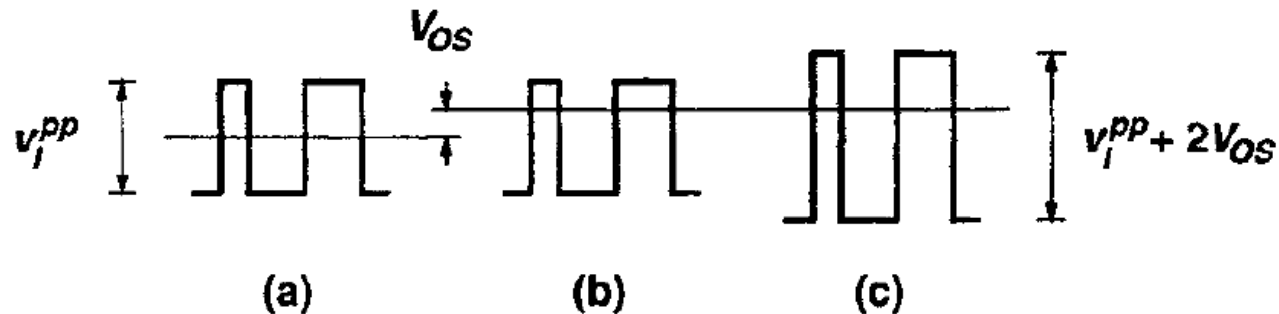
# Agenda

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- Multi-stage limiting amplifiers
- Bandwidth extension techniques
- Offset compensation

# Offset Compensation

- The receiver sensitivity is degraded if the limiting amplifier has an input-referred offset
- This is often quantified in terms of a Power Penalty, PP

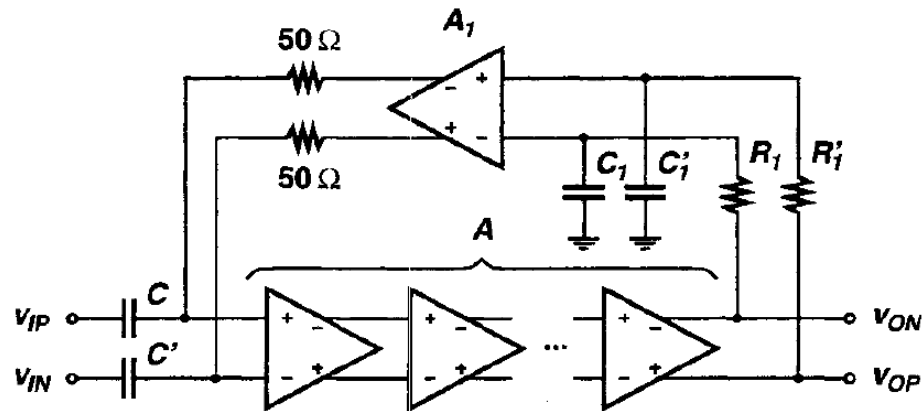


**Fig. 6.5** Effect of an input offset voltage in the LA: (a) without offset, (b) with offset, and (c) with offset and increased signal swing to restore the original bit-error rate.

$$PP = \frac{v_I^{pp} + 2V_{OS}}{v_I^{pp}} = 1 + \frac{2V_{OS}}{v_I^{pp}}$$

- It is important to minimize the offset of these multi-stage limiting amplifiers!

# Offset Compensation



- The DC offset,  $V_{os}$ , of the limiting amplifier is compensated by a low-frequency negative feedback loop

Ideally, this reduces the offset to

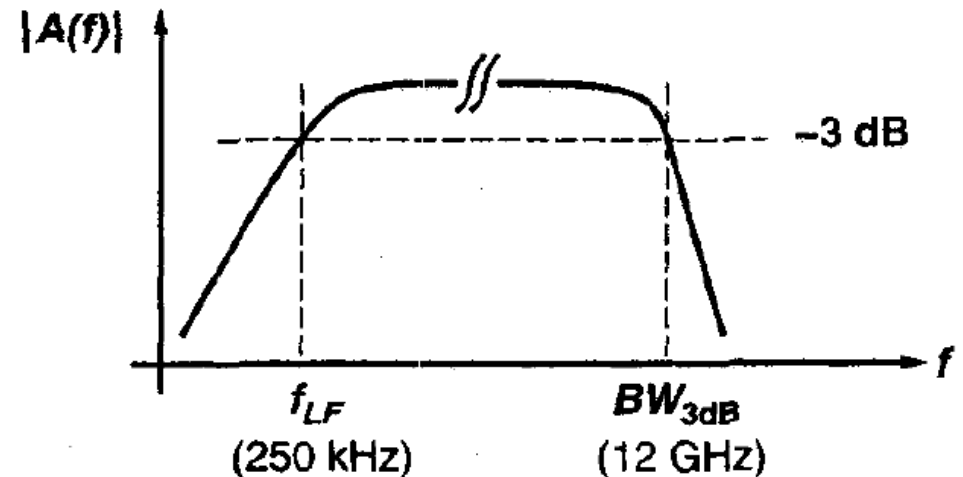
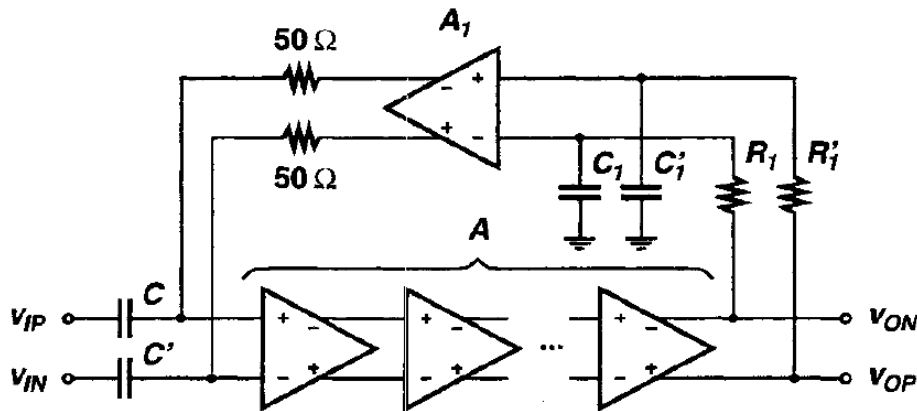
$$\frac{V_{os}}{1 + AA_1} \approx \frac{V_{os}}{AA_1}$$

However, if the error amplifier has an offset,  $V_{os1}$ , the offset becomes

$$\sqrt{\left(\frac{V_{os}}{AA_1}\right)^2 + \left(\frac{V_{os1}}{A}\right)^2}$$

with uncorrelated offset voltages

# Offset Compensation



- The low-pass filtering in the feedback loop causes a low-frequency cutoff

$$f_{LF} = \frac{1}{2\pi} \frac{AA_1/2 + 1}{R_1 C_1}$$

Note, the  $AA_1/2$  factor assume a  $50\Omega$  driver source

- Thus, the feedback loop bandwidth should be made much lower than the lowest frequency content of the input data
- This may lead to large-area passive in the offset correction feedback
- Some designs leverage Miller capacitive multiplication with the error amplifier to reduce this filter area

# Next Time

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- High-Speed Wireline Transmitters