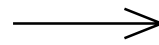


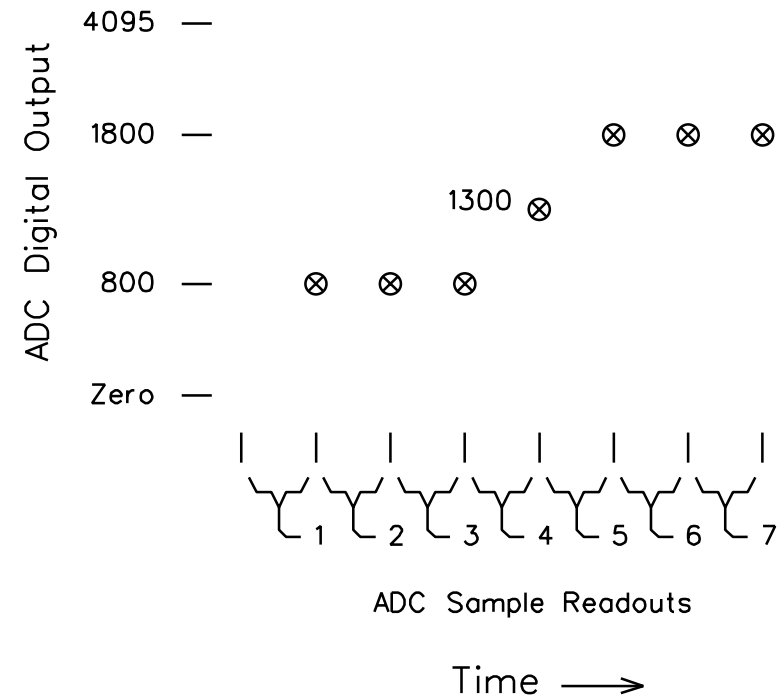
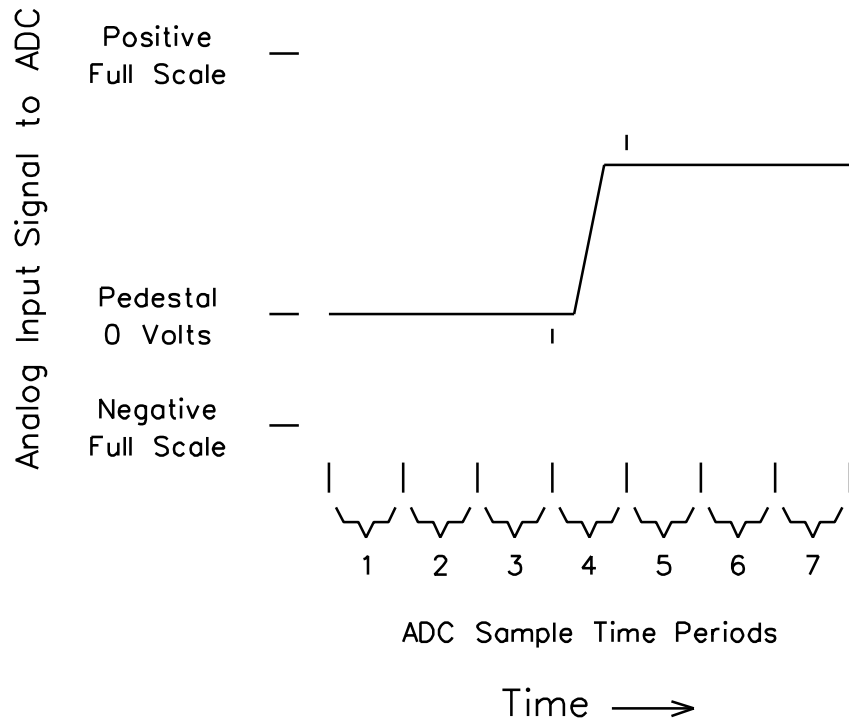
Input Signal: Rise is Centered in a Sample Period

Signal Rise Started 1.4 nsec Later than in Drw: 1

"Thinking Positive"
Analog Signal Input



Resulting ADC Digital Output



Sample Period: 4.8 nsec.
Signal Risetime: 2.0 nsec.
Signal Rise Is Linear