

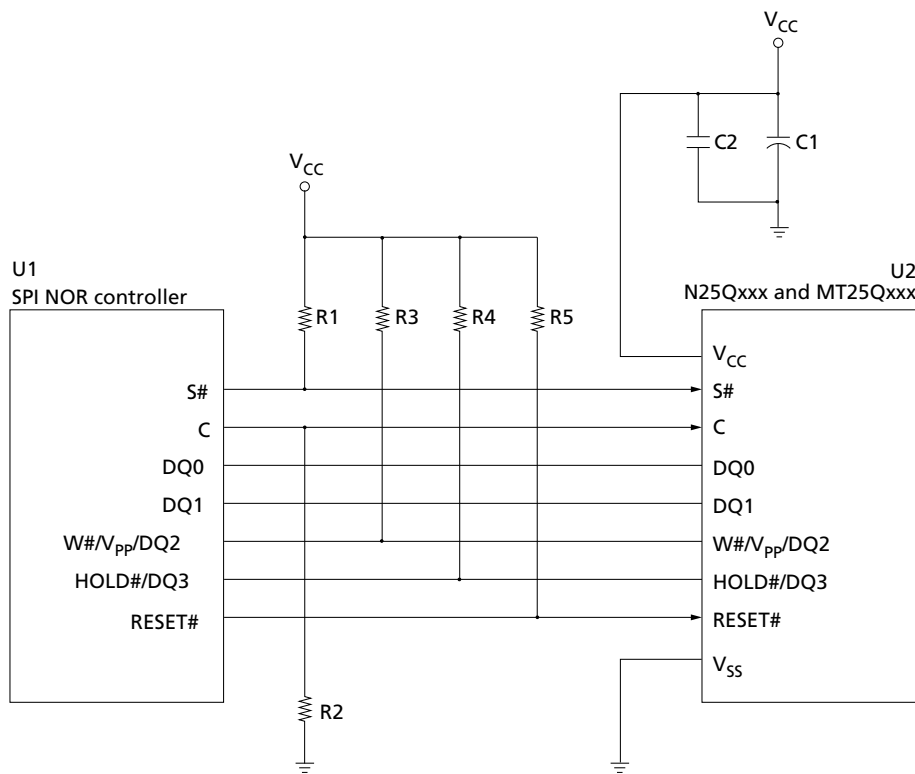
# Technical Note

## PCB Layout Design Guidelines

### Introduction

This technical note provides PCB designers basic guidelines for optimizing signal layout and power supply lines in Micron's Serial NOR Flash device to prevent signal integrity problems. The standard data sheet provides a complete description of functionality, operating modes, and specifications. IBIS models for simulating signal integrity issues are available at [micron.com](http://micron.com).

**Figure 1: Serial NOR Flash Recommended Schematic**



- Notes:
1. V<sub>pp</sub> is available only with N25Qxxx products.
  2. MT25Q devices already include a RESET# pull-up resistor.
  3. When HOLD# is disabled, a pull-up resistor for it is unnecessary. The HOLD# functionality can be disabled using bit 4 of the NVCR as described in device datasheet.
  4. When the controller drives input signals at proper V<sub>IL</sub>/V<sub>IH</sub> levels, pull-up and pull-down resistors are unnecessary.

## Resistor Terminations

**Table 1: Recommended Resistor Terminations**

Parameter	Symbol	Min	Max	Recommended	Unit	Description	Notes
S# pull-up resistor	R1	4.7	50	10	K $\Omega$	Prevents bus floating	–
CLK pull-down resistor	R2	47	500	100	K $\Omega$	Ensures that S# and CLK are not HIGH simultaneously and that $t^{SHCH}$ is met.	–
W# pull-up resistor	R3	4.7	50	10	K $\Omega$	Prevents bus floating	–
HOLD# pull-up resistor	R4	4.7	50	10	K $\Omega$	Prevents bus floating	–
RESET# pull-up resistor	R5	4.7	50	10	K $\Omega$	Prevents bus floating	1
CLK/ Control/DAT impedance	–	45	55	50	$\Omega$	Impedance match: Final manufacturing value	2
V <sub>CC</sub> capacitor value	C1, C2	3.3 + 0.01	10 + 0.22	4.7 + 0.1	$\mu$ F	Decoupling capacitor should be connected as closely as possible to V <sub>CC</sub> and V <sub>SS</sub>	–

- Notes:
1. With specific reference to N25Q256A8xxxxxx and N25Q512A8xxxxxx (with dedicated RESET# pin), the recommended values of pull-up resistor are 4.7K Ohm (for N25Q256A8xxxxxx) and 2.2K Ohm (for N25Q512A8xxxxxx).
  2. All signals should be routed with controlled impedance. When trace impedance is outside the specified range, simulation with IBIS models is strongly recommended to determine serial resistor terminations for data lines.

## PCB Design Recommendations

### V<sub>CC</sub> Power Supply Decoupling

For decoupling power supply V<sub>CC</sub>, two ceramic capacitors are recommended, one 4.7µF 0805 and one 0.1µF 0603.

### Decoupling Capacitor Routing Lengths

Reducing decoupling capacitor routing lengths helps minimize total loop inductance. The measure includes the following:

- Reduced V<sub>CC</sub> and V<sub>SS</sub> decoupling capacitor pad fan out trace length
- Fan out trace width equal to or less than the capacitor pad width
- Power and ground planes
- Decoupling capacitor placement relative to device

Figure 2: Connecting Capacitor Pads

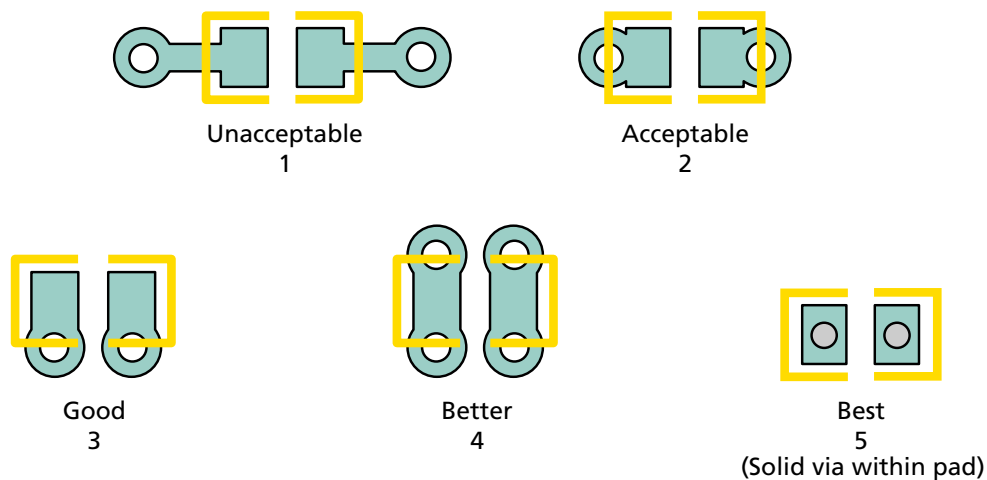
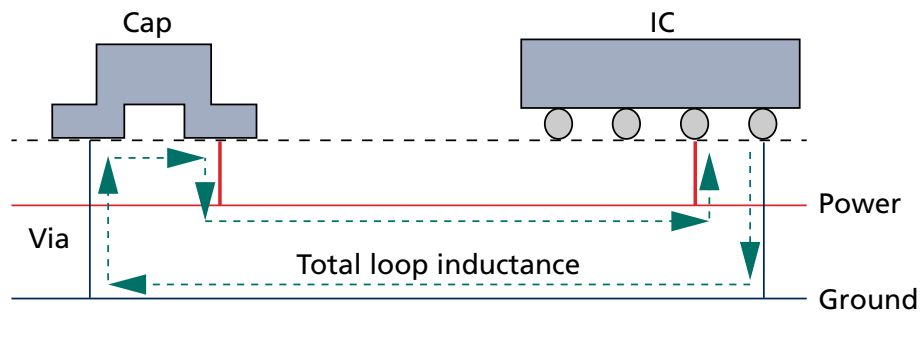


Figure 3: Routing Decoupling Capacitor



## Decoupling Capacitor Placement

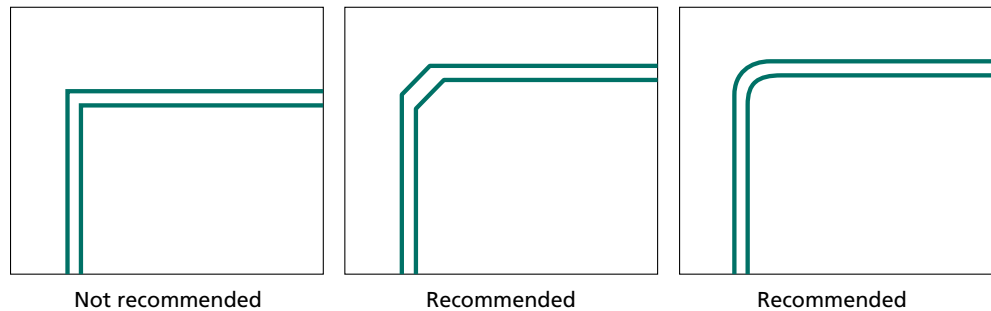
Decoupling capacitors should be as close as possible to  $V_{CC}$  and  $V_{SS}$  pads with priority as follows: Closest is  $0.1\mu\text{F}$  followed by  $4.7\mu\text{F}$ .

## CLK Signal Routing

The following clock trace guidelines help minimize impedance variation:

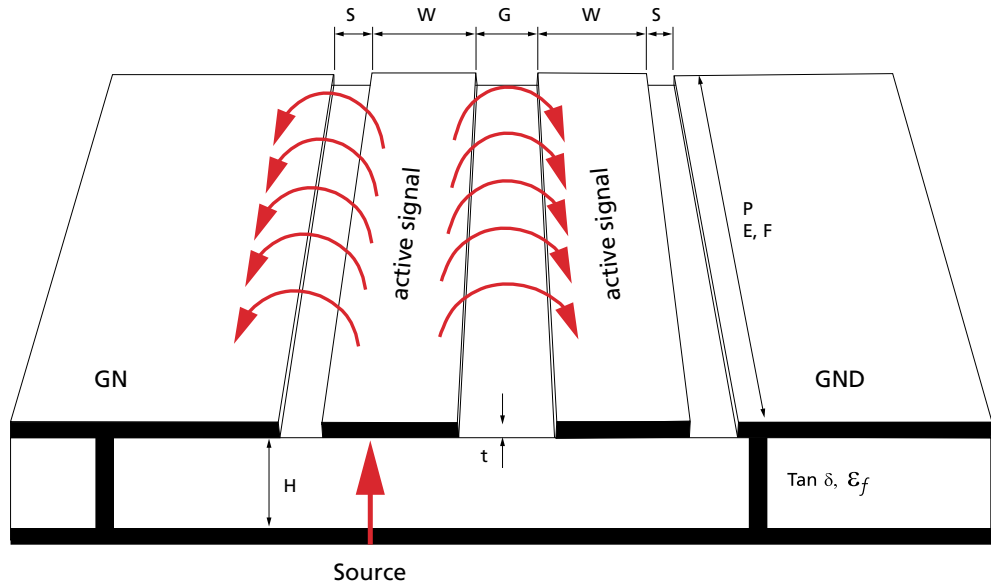
- To minimize impedance variation, maintain a straight clock trace, as much as possible, by using arc-shaped bends instead of right-angle bends.

**Figure 4: Trace Shape**



- Maintain a short clock trace, as much as possible, and match lengths between clock and data signals.
- Use one signal layer to ensure constant transmission line impedance for the clock signal.
- Place a ground plane next to the outer layer to minimize noise from other signals.
- If an inner layer is used to route the clock trace, sandwich the inner layer between reference planes.
- To minimize reflection, terminate clock signals or set up an appropriate driver strength, and keep the clock trace with controlled impedance (typically 50 ohm trace impedance).
- To ensure signal quality, use point-to-point clock trace as much as possible.
- To reduce crosstalk from other, nearby signals, maintain space between the clock signal line and other signal lines as wide as possible. Moreover, take care to have dielectric height more than three times the distance among two adjacent lines, as showed in the below drawing:

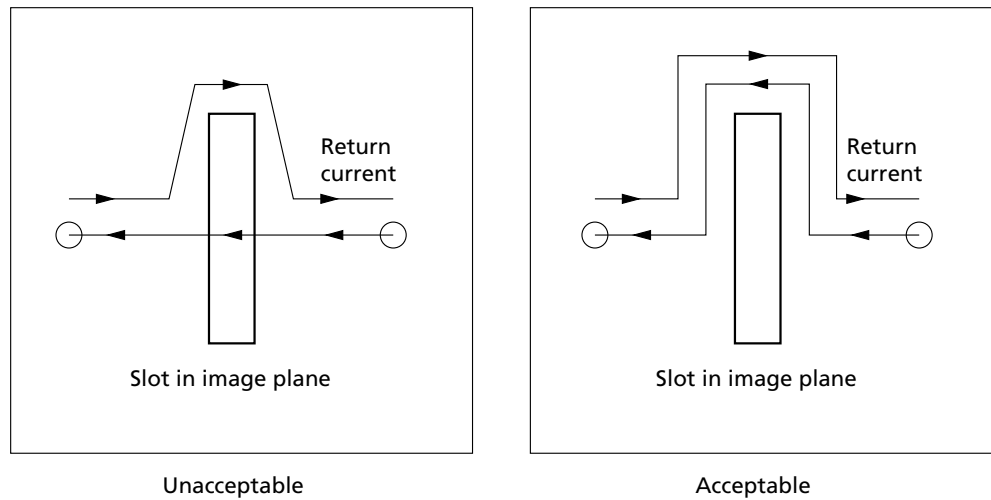
**Figure 5: Trace Width Example**



Note: 1. Dielectric height =  $H$ , trace to trace separation =  $G$ . For optional crosstalk performance  $G/H \geq 3$ .

- The clock signal should not be over the split plane.

**Figure 6: Avoiding Breaks and Voids**

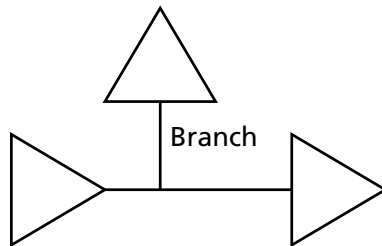


## Data Signal Routing

- Data signals should not be over the split plane.
- Data signals should not be routed over via-anti pads.
- Maintain a continuous reference plane for each data signal over its entire path.
- If the signal reference plane changes from ground plane to power plane, add capacitors near the via transition site to help support a good return path.

- If the signal reference plane changes from one ground plane to another, ground vias should surround all signals (Two ground vias per clock via; one ground via per high-speed signal via).
- Keep stubs short to avoid reflections. Keep stub propagation delay to <20% of the signal rise time.

**Figure 7: Typical Stub Case**





## **Revision History**

### **Rev. B – 7/16**

- Added note to Recommended Resistor Terminations table for N25Q

### **Rev. A – 7/15**

- Initial release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.  
Although considered final, these specifications are subject to change, as further product development and data characterization some-  
times occur.