IEEE803.2cg (10BASE-T1L)
Standard Amendment

Contents

Rev. D: First public Version

Rev. E: Correction in figure 164-6 PCS Receive state diagram (brackets in condition from initial state to "IDLE" state)

Rev. F: Corrected figures A-1 to A-3 in Informative Annex, minor editorial corrections in document

164 Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1L

164.1 Overview

To Do.

164.2 10BASE-T1L service primitives and interfaces

To Do.

164.3 100BASE-T1 Physical Coding Sublayer (PCS) functions

The Physical Coding Sublayer (PCS) consists of PCS Reset, the PCS Data Transmission Enable, PCS Transmit, and PCS Receive functions as shown in figure 164-1. The PCS Reset function is explained in 164.3.1, the PCS Data Transmission Enable function is explained in 164.3.2, the PCS Transmit function is explained in 164.3.3, and the PCS Receive function is explained in 164.3.4.

164.3.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on (see 36.2.5.1.3).
b) The receipt of a request for reset from the management entity.

PCS Reset shall set pcs_reset = ON while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

164.3.2 PCS Data Transmission Enable

The PCS Data Transmission Enable function shall conform to the PCS Data Transmission Enable state diagram in figure 164-2. When tx_mode is equal to SEND_N, the signals tx_enable_mii and tx_error_mii are equal to the values of the MII signals TX_EN and TX_ER respectively, otherwise tx_enable_mii and tx_error_mii are set to the value FALSE.

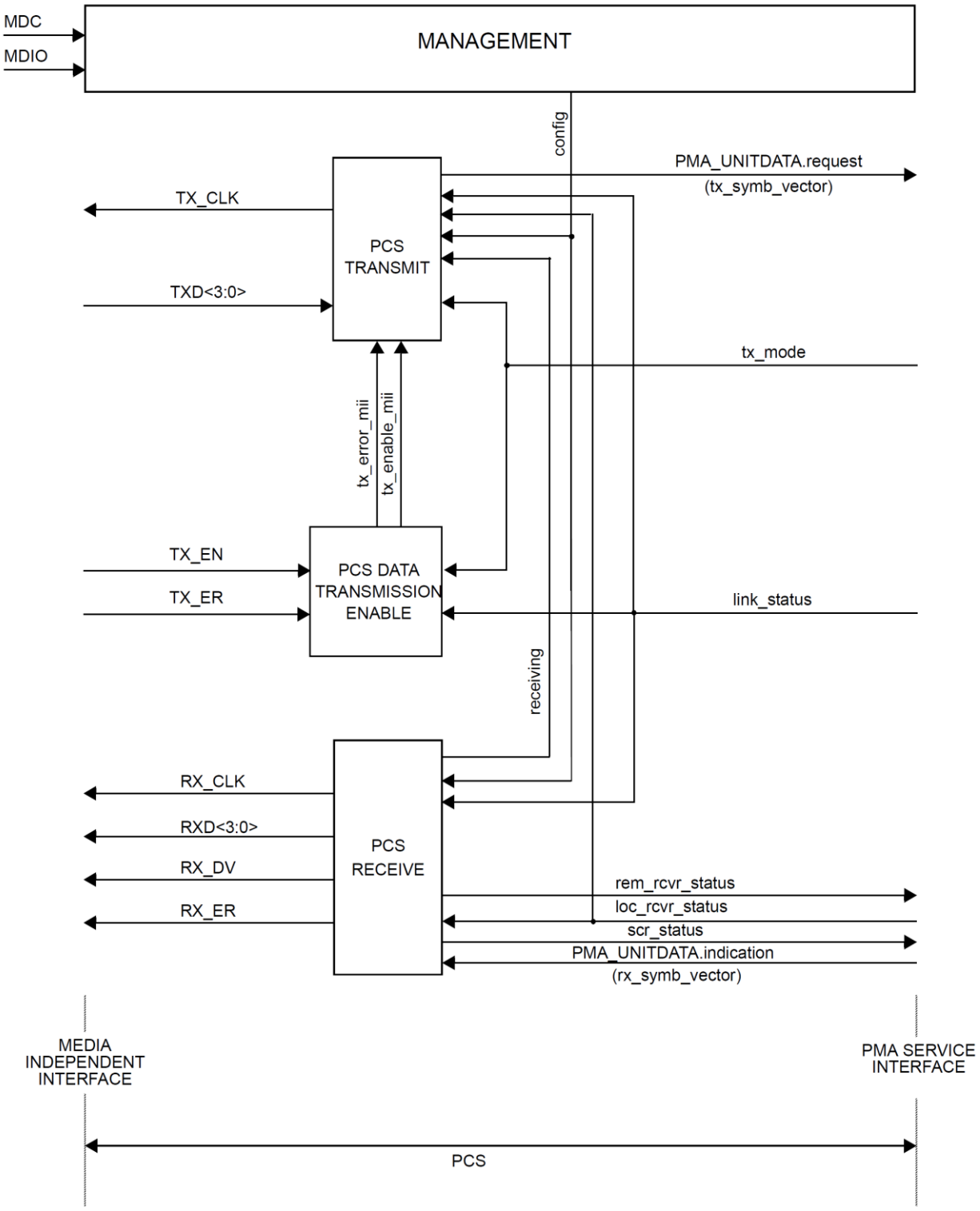


Figure 164-1 PCS reference design

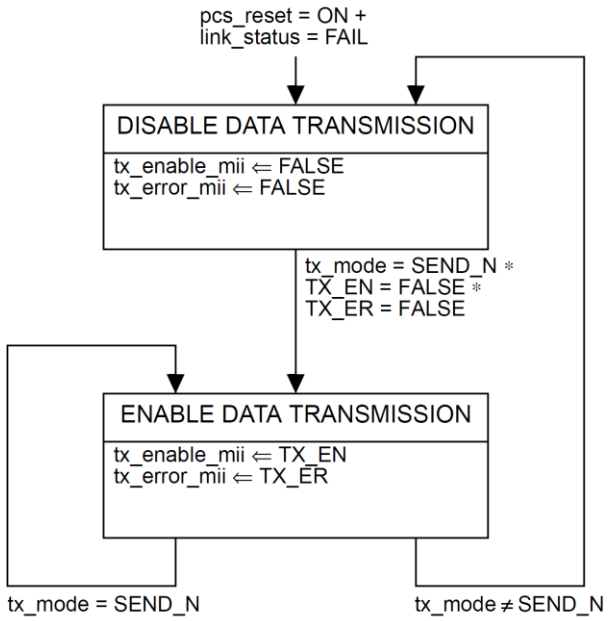


Figure 164-2 PCS Data Transmission Enable state diagram

164.3.2.1 Variables

link_status — The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK or FAIL

pcs_reset — The pcs_reset parameter set by the PCS Reset function.
Values: ON or OFF

tx_enable_mii — The tx_enable_mii variable is generated in the PCS Data Transmission Enable state diagram as specified in figure 164-2. When set to FALSE transmission is disabled, when set to TRUE transmission is enabled.
Values: TRUE or FALSE

tx_error_mii — The tx_error_mii variable is generated in the PCS Data Transmission Enable state diagram as specified in figure 164-2.When this variable is set to FALSE it indicates a non-errored transmission, when set to TRUE it indicates an errored transmission.
Values: TRUE or FALSE

TX_EN — The TX_EN signal of the MII as specified in 22.2.2.3.

TX_ER — The TX_ER signal of the MII as specified in 22.2.2.5.

tx_mode — The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indication primitive.
Values: SEND_Z, SEND_N, or SEND_I

164.3.3 PCS Transmit

164.3.3.1 PCS Transmit state diagram

The PCS Transmit function shall conform to the PCS Transmit state diagram in figure 164-3, and the associated state variables, functions, timers and messages.

In each symbol period, PCS Transmit generates a symbol A_n provided to the PMA, operating in one of three different modes (tx_mode), where symbol A_n is a ternary code that can take values of {-1, 0, +1}. The PMA transmits symbol A_n over the wire pair BI_DA. The integer, n, is a time index, introduced to establish a temporal relationship between different symbol periods. The nominal symbol clock frequency is specified in 164.5.4.5.

Upon the assertion of TX_EN, the PCS Transmit function passes an SSD of 12 consecutive symbols to the PMA, which replaces the first 16 bits of the preamble. Following SSD, TXD[3:0] is encoded into ternary symbols using encoding rules specified in 164.3.3.2.5, until TX_EN is de-asserted.

Following the de-assertion of TX_EN, a special code ESD (or ERR_ESD when a transmit error is encountered, which means that TX_ER was high at any point during the transmission) of 12 consecutive symbols is generated, after which the transmission of idle mode according to 164.3.3.2.5 is resumed.

10BASE-T1L has one special symbol triplet (0, 0, 0) that is not used by Idle or Data symbols. Therefore this symbol triplet will be used for the COMMA symbols within the delimiters. See figure 164-6 for more details.

The 10BASE-T1L PHY supports normal operation and link training operation. In training operation, the PCS ignores signals from the MII and sends only the idle signals to the PMA until training process is complete.

If tx_mode has the value SEND_Z, PCS Transmit passes a vector of zeros at each symbol period to the PMA.

If tx_mode has the value SEND_I, PCS Transmit generates sequences of symbols according to the encoding rule in idle mode as described in 164.3.3.2.5.

If tx_mode has the value SEND_N, PCS Transmit generates symbols A_n at each symbol period representing data, special control symbols like SSD/ESD or IDLE symbols as defined in 164.3.3.2.5. The transition from idle to data is signaled by an SSD, and the end of transmission of data is signaled by an ESD.

During training operation (when tx_mode is SEND_I), knowledge of the transmitted symbols may be used at receiver side to perform any signal conditioning necessary for meeting the required performance during normal operation. When the link is up, the PHY enters SEND_N mode and the transmitted PAM3 symbols are used at receiver PHY for continued clock frequency/phase tracking.

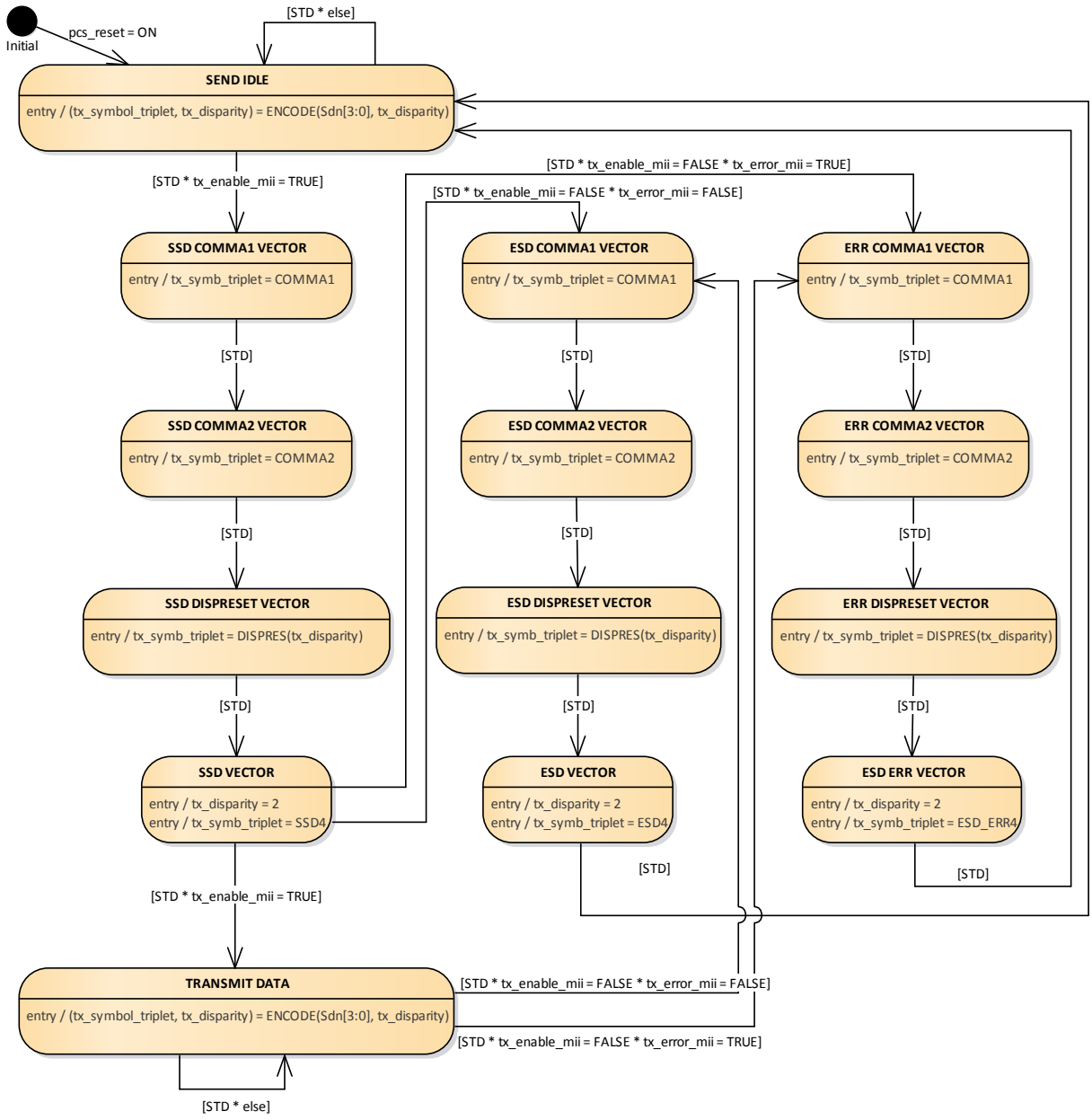


Figure 164-3 PCS Transmit state diagram

164.3.3.1.1 Variables

COMMA1 — A vector of three ternary symbols in the first code-group of any delimiter as specified in 164.3.3.2.5.

COMMA2 — A vector of three ternary symbols in the second code-group of any delimiter as specified in 164.3.3.2.5.

DISPRESET3 — A vector of three ternary symbols in the third code-group of any delimiter as specified in 164.3.3.2.5.

SSD4	A vector of three ternary symbols in the fourth code-group of SSD as specified in 164.3.3.2.5.
ESD4	A vector of three ternary symbols in the fourth code-group of ESD as specified in 164.3.3.2.5.
ESD_ERR4	A vector of three ternary symbols in the fourth code-group of ESD as specified in 164.3.3.2.5.
pcs_reset	The pcs_reset parameter set by the PCS Reset function. Values: ON or OFF
tx_enable_mii	The tx_enable_mii variable is generated in the PCS Data Transmission Enable state diagram as specified in figure 164-5. When set to FALSE transmission is disabled, when set to TRUE transmission is enabled. Values: TRUE or FALSE
tx_error_mii	The tx_error_mii variable is generated in the PCS Data Transmission Enable state diagram as specified in figure 164-5.When this variable is set to FALSE it indicates a non-errored transmission, when set to TRUE it indicates an errored transmission. Values: TRUE or FALSE
tx_mode	The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indication primitive. Values: SEND_Z, SEND_N, or SEND_I
loc_rcvr_status	The loc_rcvr_status parameter set by the PMA Receive function and passed to the PCS via the PMA_RXSTATUS.indication primitive. Values: OK or NOT_OK
loc_lpi_req	The loc_lpi_req is set TRUE, if low power idle mode is requested. To Do. Values: TRUE or FALSE.
$Sd_n[3:0]$	The $Sd_n[3:0]$ signal of the scrambler output as defined in 164.3.3.2.4.
Tx_n	Alias for tx_symb_vector at time n.
tx_symb_triplet	A triplet of ternary symbols generated by the PCS Transmit function after 4B3T encoding. Value: A triplet of ternary transmit symbols. Each of the ternary symbols may take on one of the values {–1, 0, +1}.
tx_disparity	PCS local variable containing the running disparity. After PCS Reset the initial value shall be set to 2. Values: 1 to 4, depending on running disparity.

164.3.3.1.2 Functions

ENCODE — In the PCS Transmit process, this function takes as its arguments $Sd_n[3:0]$ and the tx_disparity and returns the corresponding tx_symb_triplet as well as the updated tx_disparity. ENCODE follows the 4B3T rules defined in 164.3.3.2.5.

(tx_symbol_triplet, tx_disparity) = ENCODE(Sd_n[3:0], tx_disparity)

The tx_disparity can be between 1 and 4 and the respective tx_symbol_triplet is taken from the 4B3T encoding rules defined in table 164-1 based on the $Sd_n[3:0]$ value and the tx_disparity:

tx_symbol_triplet = $table_{4B3T}$(Sd_n[3:0], tx_disparity)

The second output value of this function is an updated tx_disparity value, which is calculated in the following way:

tx_disparity = tx_disparity + disparity of currently encoded tx_symbol_triplet

DISPRES — The function DISPRES returns one of the four possible DISPRESET3 triple ternary symbols (see table 164-3), depending on the actual tx_disparity:

tx_symbol_triplet = $table_{DISPRESET3}$(tx_disparity)

164.3.3.1.3 Timers

symb_timer — The symb_timer shall be generated synchronously with TX_TCLK. In the PCS Transmit state diagram, the message PMA_UNITDATA.request is issued concurrently with symb_timer_done.

Continuous timer:	The condition symb_timer_done becomes true upon timer expiration.
Restart time:	Immediately after expiration, timer restart resets the condition symb_timer_done.
Duration:	1 symbol time (see chapter 164.5.4.5)

symb_triplet_timer — The symb_triplet_timer shall be generated synchronously with PCS transmit clock TX_CLK.

Continuous timer:	The condition symb_triplet_timer_done becomes true upon timer expiration.
Duration:	3 symbol times (see chapter 164.5.4.5)

164.3.3.1.4 Abbreviations

STD — Alias for symb_triplet_timer_done.

164.3.3.2 PCS transmit symbol generation

The reference diagram of transmit symbol generation is indicated in figure 164-4. The tx_symb_triplet is the ternary triplet (TA_n, TB_n, TC_n).

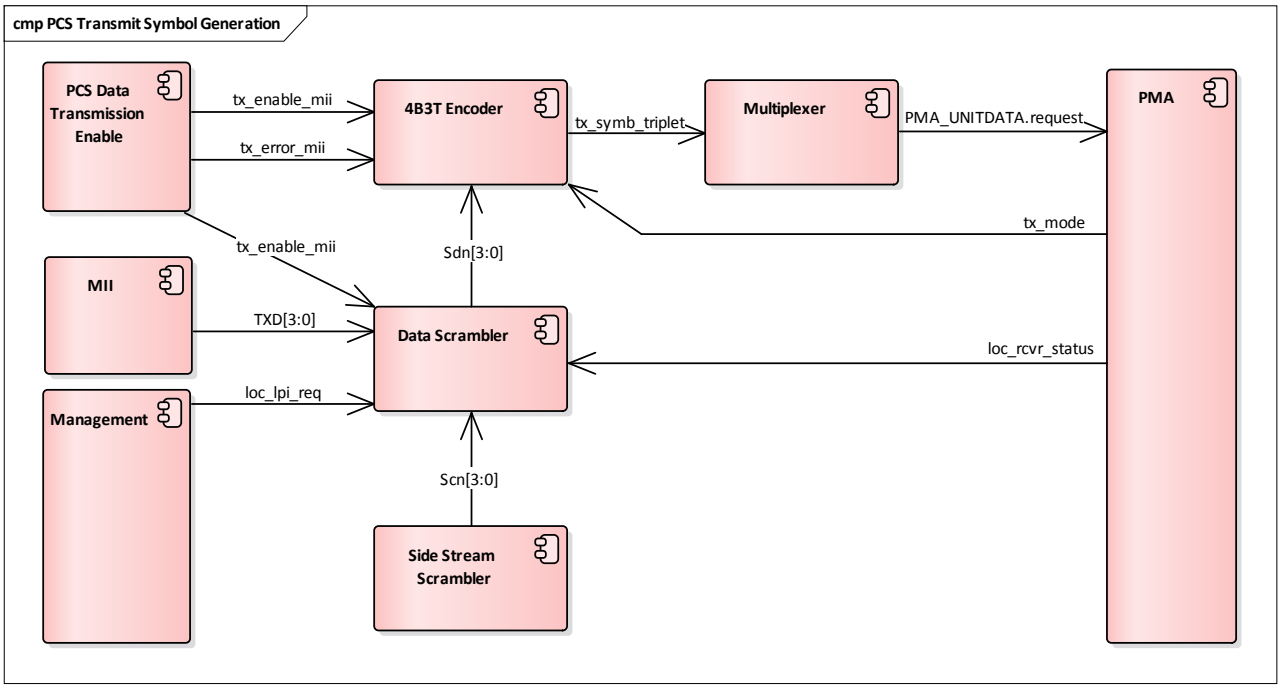


Figure 164-4 PCS transmit symbol generation

164.3.3.2.1 Side-stream scrambler polynomial

The PCS Transmit function employs side-stream scrambling. For the master PHY PCS Transmit shall employ

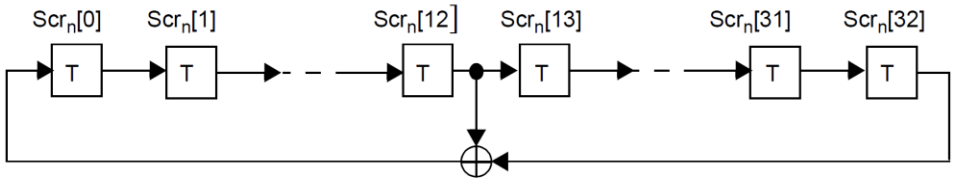
$$g_M(x) = 1 + x^{13} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. For the slave PHY PCS Transmit shall employ

$$g_S(x) = 1 + x^{20} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. An implementation of master and slave PHY side-stream scramblers by linear-feedback shift registers is shown in figure 164-5. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros.

Side-stream scrambler employed by the MASTER PHY



Side-stream scrambler employed by the SLAVE PHY

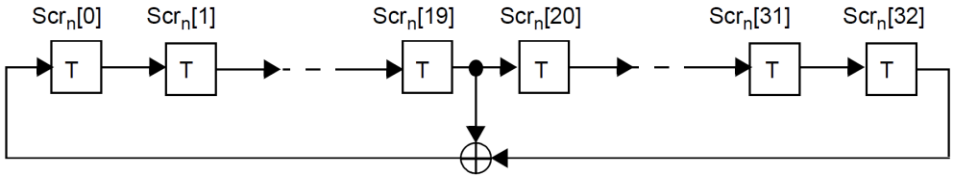


Figure 164-5 A realization of side-stream scramblers by linear feedback shift registers

164.3.3.2.2 Generation of $Sy_n[3:0]$

PCS Transmit encoding rules are based on the generation, at time n, of the four bits $Sy_n[3:0]$. The four bits $Sy_n[3:0]$ are used for de-correlating the MII data word TXD<3:0> during data transmission and for generating the idle symbols. These four bits are generated as described below, using an auxiliary generating polynomial, g(x):

$$g(x) = x^3 \hat{} x^8$$

The four bits $Sy_n[3:0]$ shall be generated using the bit $Scr_n[0]$ and g(x) as in the following equations:

$$Sy_n[0] = Scr_n[0]$$
$$Sy_n[1] = g(Scr_n[0]) = Scr_n[3] \hat{} Scr_n[8]$$
$$Sy_n[2] = g^2(Scr_n[0]) = Scr_n[6] \hat{} Scr_n[16]$$
$$Sy_n[3] = g^3(Scr_n[0]) = Scr_n[9] \hat{} Scr_n[14] \hat{} Scr_n[19] \hat{} Scr_n[24]$$

By construction, the four bits $Sy_n[3:0]$ are derived from elements of the same maximum-length shift register sequence of length 2^{33-1} as $Scr_n[0]$, but shifted in time by varying delays. The associated delays are all large and different so that there is no apparent correlation among the bits.

164.3.3.2.3 Generation of $Sc_n[3:0]$

Bits $Sc_n[3:0]$ shall be generated as follows:

$$Sc_n[3:0] = Sy_n[3:0]$$

164.3.3.2.4 Generation of scrambled bits $Sd_n[3:0]$

From scrambler bits $Sc_n[3:0]$ and $TXD_n[3:0]$, bits $Sd_n[3:0]$ shall be generated as follows:

$$Sd_n[3] = \begin{cases} Sc_n[3]\text{^}TXD_n[3] & if\ (tx\_enable\_mii = TRUE) \\ Sc_n[3]\text{^}1 & else\ if\ \ (loc\_rcvr\_status\ =\ OK) \\ Sc_n[3] & else \end{cases}$$

$$Sd_n[2] = \begin{cases} Sc_n[2]\text{^}TXD_n[2] & if\ (tx\_enable\_mii = TRUE) \\ Sc_n[1]\text{^}1 & else\ if\ \ (loc\_lpi\_req\ =\ TRUE) \\ Sc_n[1] & else \end{cases}$$

$$Sd_n[1:0] = \begin{cases} Sc_n[1:0]\text{^}TXD_n[1:0] & if\ (tx\_enable\_mii = TRUE) \\ (Sc_n[2]\ Sc_n[0]) & else \end{cases}$$

Note that during transmission of idles, bits $Sc_n[1]$ and $Sc_n[2]$ shall be swapped compared to data transmission which can be used to reliably distinguish idle data transmission from data transmission on the receiver side.

164.3.3.2.5 Generation of ternary triplet in mode SEND_N and SEND_I

The scrambled bits $Sd_n[3:0]$ shall be converted to a ternary triplet (TA_n, TB_n, TC_n) using the 4B3T algorithm using a running disparity value, shown in table 164-1. The 4B3T coding is DC-free. To achieve this, the difference between the number of transmitted "+1" and "-1" symbols is limited. The running disparity is reflecting this actual difference and depending on the running disparity the next symbol coding is chosen. The same ternary symbol encoding is used while in SEND_I and SEND_N.

$Sd_n[3:0]$	**Disparity = 1**		**Disparity = 2**		**Disparity = 3**		**Disparity = 4**	
	Ternary Triplet	**Disparity Change**	**Ternary Triplet**	**Disparity Change**	**Ternary Triplet**	**Disparity Change**	**Ternary Triplet**	**Disparity Change**
0000	+0+	2	0-0	-1	0-0	-1	0-0	-1
0001	0-+	0	0-+	0	0-+	0	0-+	0
0010	+-0	0	+-0	0	+-0	0	+-0	0
0011	00+	1	00+	1	00+	1	--0	-2
0100	-+0	0	-+0	0	-+0	0	-+0	0
0101	0++	2	-00	-1	-00	-1	-00	-1
0110	-++	1	-++	1	--+	-1	--+	-1
0111	-0+	0	-0+	0	-0+	0	-0+	0
1000	+00	1	+00	1	+00	1	0--	-2
1001	+-+	1	+-+	1	+-+	1	---	-3
1010	++-	1	++-	1	+--	-1	+--	-1
1011	+0-	0	+0-	0	+0-	0	+0-	0
1100	+++	3	-+-	-1	-+-	-1	-+-	-1
1101	0+0	1	0+0	1	0+0	1	-0-	-2
1110	0+-	0	0+-	0	0+-	0	0+-	0
1111	++0	2	00-	-1	00-	-1	00-	-1

Table 164-1 4B3T encoding

The ternary symbol triplet (0, 0, 0) is used as COMMA1 and COMMA2 value, it never occurs during normal 4B3T mapping. This can also be used to synchronize the receiver's demultiplexer triplet boundary during training:

Delimiter	(TA_n, TB_n, TC_n)
COMMA1	(0, 0, 0)
COMMA2	(0, 0, 0)

Table 164-2 Comma values

The DISPRESET3 triplet, together with the following fourth symbol group (which always has a disparity of 1), shall be used to bring back the running disparity to a defined value. The DISPRESET3 symbol triplet is always changing the running disparity value to 1. Taking the disparity of the following fourth symbol group into account, which is always having a disparity of 1, the resulting running disparity value is 2 after transmission of the complete delimiter, thus being back the initial running disparity again. The following coding shall be used for the DISPRESET3 symbol triplet:

Symbol Triplet	Disparity = 1	Disparity = 2	Disparity = 3	Disparity = 4
DISPRESET3	(-1, 0, 1)	(-1, 0, 0)	(-1, 0, -1)	(-1, -1, -1)

Table 164-3 Disparity reset

The fourth symbol group (SSD4/ESD4/ESD_ERR4) shall be encoded as follows (all have disparity of +1):

Delimiter	(TA_n, TB_n, TC_n)
SSD4	(1, 1, -1)
ESD4	(1, -1, 1)
ESD_ERR4	(-1, 1, 1)

Table 164-4 Delimiters

164.3.3.2.6 Generation of ternary triplet in mode SEND_Z

The ternary triplet (TA_n, TB_n, TC_n) shall be a zero vector (0, 0, 0) when tx_mode = SEND_Z.

164.3.3.2.7 Generation of symbol sequence

A ternary triplet (TA_n, TB_n, TC_n) shall be sent in the order:

TA_n	TB_n	TC_n	TA_{n+1}	TB_{n+1}	TC_{n+1}	...

164.3.4 PCS Receive

164.3.4.1 PCS Receive overview

The PCS Receive function shall conform to the PCS Receive state diagram in figure 164-6, and associated state variables.

A JAB state machine as shown in figure 164-7, shall be implemented to prevent any mis-detection of ESD that would make the PCS Receive state machine lock up in the DATA state. The maximum dwelling time in DATA state shall be less than the period specified for rcv_max_timer. When rcv_max_timer expires, the PCS Receive state machine is reset and transition to IDLE state is forced.

In figure 164-6, there are a total of five states after SSD4 detection before the DATA state; meanwhile, there are also five states before the IDLE state (including the DATA state) that perform DATA decoding. As a result, the depth of data flush-in delay line is the same as the flush-out delay line ensuring correct packet reception at the MII.

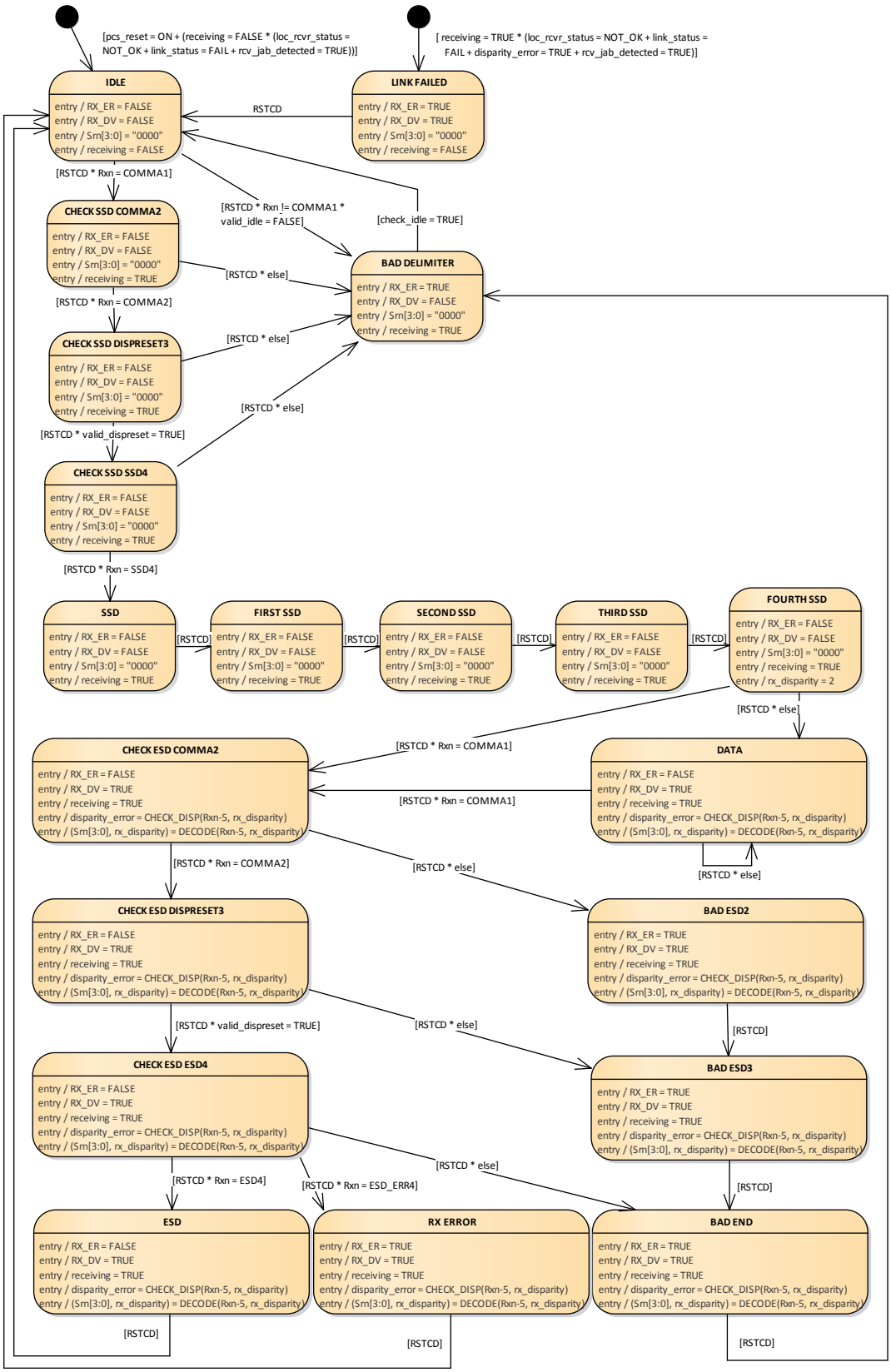


Figure 164-6 PCS Receive state diagram

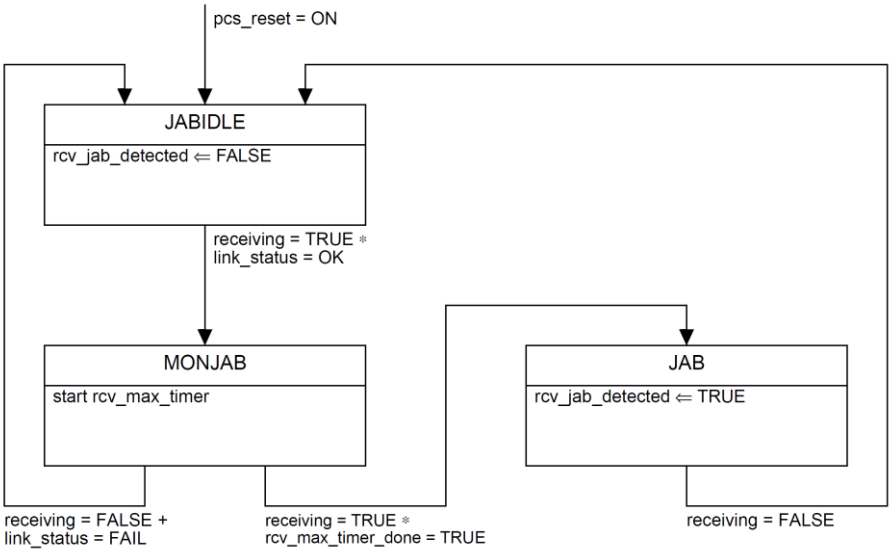


Figure 164-7 JAB state diagram

The variables, functions, and timers used in figure 164-6 and figure 164-7 are defined as below. For the definition of IDLE, COMMA1, COMMA2, DISPRESET3, SSD4, ESD4 and ERR_ESD4, see 164.3.3.2.5.

164.3.4.1.1 Variables

pcs_reset	The pcs_reset parameter set by the PCS Reset function. Values: ON or OFF
link_status	The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive. Values: OK or FAIL
receiving	Generated by the PCS Receive function; if set as TRUE, it indicates that the PCS is in Data mode. Values: TRUE or FALSE
loc_rcvr_status	The loc_rcvr_status parameter set by the PMA Receive function and passed to the PCS via the PMA_RXSTATUS.indication primitive. Values: OK or NOT_OK
RX_ER	The RX_ER signal of the MII as specified in 22.2.2.10.
RX_DV	The RX_DV signal of the MII as specified in 22.2.2.7.
RXD[3:0]	PCS decoded data synchronous to RX_CLK.
Rx_n	Received symbol triple generated by PCS Receive at time n.
rx_symb_triplet	A triplet of ternary symbols generated by the PCS Receive function before ternary triplet decoding.

Value: A triplet (RA_n, RB_n, RC_n) of ternary receive symbols. Each of the ternary symbols may take one of the values {–1, 0, +1}.

rx_symb_vector — A vector of ternary symbols received by the PMA and passed to the PCS via the PMA_UNITDATA.indication primitive.
Value: single ternary symbol

rx_disparity — PCS local variable containing the calculated running disparity at receiver side. After PCS Reset the initial value shall be set to 2.
Values: 1 to 4, depending on running disparity.

disparity_error — The disparity_error is set by the 4B3T decoder in the receiver, when a rx_symb_triplet is received that this not allowed according to the running disparity calculated in the decoder.

rcv_jab_detected — Variable set as TRUE when in JAB state as shown in JAB state diagram in figure 164-7 else it is set FALSE.
Values: TRUE or FALSE

$Sr_n[3:0]$ — Output from 4B3T decoder to descrambler.

164.3.4.1.2 Functions

valid_idle — The function checks whether or not the decoded data bits $Sr_n[1:0]$ are equal to the expected $Sd_n[1:0]$ values from the local descrambler ($Sr_n[3]$ cannot be used in comparison since it carries rem_rcvr_status and $Sr_n[2]$ cannot be used in comparison since it carries rem_lpi_req).

check_idle — The check_idle function indicates a reliable detection of the idle data stream.
Values: TRUE or FALSE

valid_dispreset — The rx_symb_triplet is one of the DISPRESET3 triplets as specified in 164.3.3.2.5. It returns a Boolean value indicating whether or not one of the four DISPRESET3 triplets has been received.

DECODE — In the PCS Receive process, this function takes as its arguments the value of rx_symb_triplet and rx_disparity and returns the corresponding $Sr_n[3:0]$ as well as the updated rx_disparity. DECODE follows the rules outlined in 164.3.4.2 and the inverse encoding rules stated in table 164-1.

$Sr_n[3:0] = inverse\_table_{4B3T}(Rx_n)$

rx_disparity = rx_disparity + disparity of currently received Rx_n

CHECK_DISP — The CHECK_DISP function checks, if the currently received triple ternary symbol is allowed for the current rx_disparity.

$disparity\_error = (Rx_n != table_{4B3T}(inverse\_table_{4B3T}(Rx_n), rx\_disparity)$

164.3.4.1.3 Timer

RSTCD — Receive Symbol Tripled Conversion Done, synchronized with PCS receive clock RX_CLK.

rcv_max_timer — A timer used to determine the maximum amount of time the PHY Receive state machine stays in DATA state. The timer shall expire TBD (suggested are 2 ms ± 100 µs, transmission of 1500 bytes take approx. 1.2 ms, if jumbo frames should also be handled we have to increase this time) after being started. The condition rcv_max_timer_done becomes true upon timer expiration.

164.3.4.2 PCS Receive symbol decoding

When PMA Receive indicates normal operation and sets loc_rcvr_status = OK, the PCS Receive function checks the symbol sequences and searches for SSD or receive error indicator. The receiver de-interleaves the sequences of rx_symb_vector to rx_symb_triplet accordingly.

The received symbols, rx_symb_vector, are de-interleaved to generate rx_symb_triplet (RA_n, RB_n, RC_n). To achieve correct operation, PCS Receive uses the knowledge of the encoding rules that are employed in the idle mode (the triplet (0, 0, 0) will never occur, if this triplet is being received, then the symbol synchronization in the de-interleaving block needs to be adjusted). PCS Receive generates the sequence of symbols and indicates the reliable acquisition of the descrambler state by setting the parameter scr_status to OK.

The received ternary triplets (RA_n, RB_n, RC_n) are decoded to generate signals RXD[3:0], RX_DV, and RX_ER at the MII. The decoder shall also generate the disparity_error signal for the PCS Receive state machine when a ternary triplet is received that is not allowed according to the current running disparity value. Each time a ternary triplet is received, the running disparity is updated. This is done using the current running disparity and adding the disparity change value as specified in table 164-1 for the currently received ternary triplet.

PCS Receive sets RX_DV = TRUE when it receives SSD, and sets RX_DV = FALSE when it receives ESD or ESD with error.

PCS Receive shall set RX_ER = TRUE when it receives bad ESDs, ERR_ESD, or bad SSDs. When the state machine reaches the IDLE state, RX_ER gets reset to FALSE.

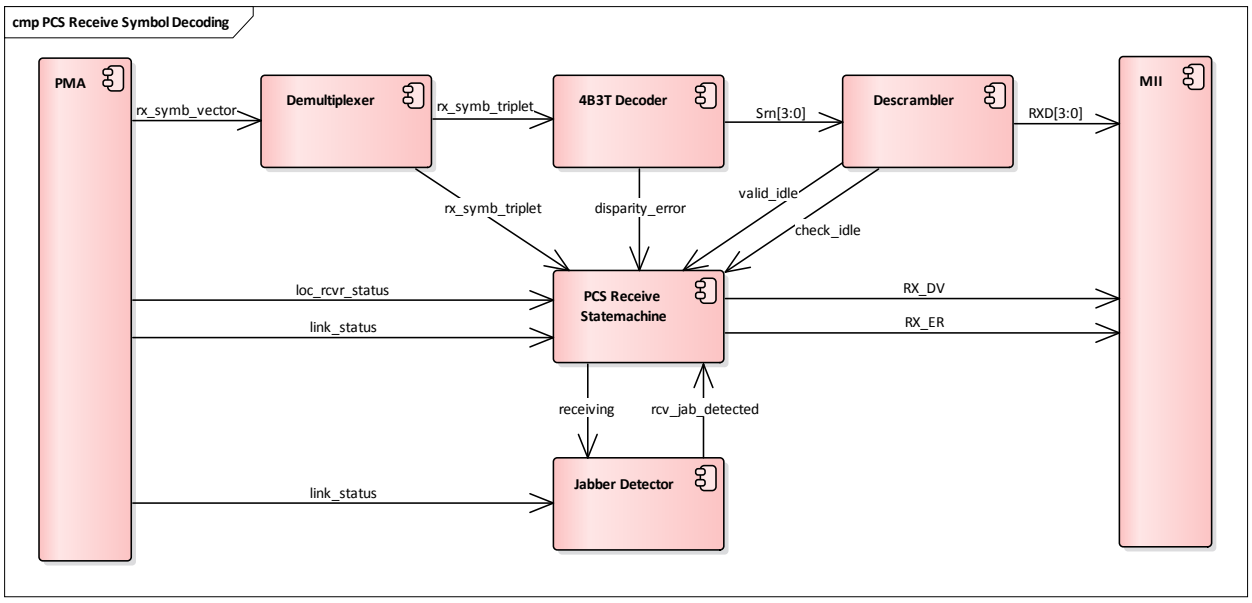


Figure 164-8 PCS Data receive symbol decoding

164.3.4.3 PCS Receive descrambler polynomial

The PHY shall descramble the data stream and return the proper sequence of code-groups to the decoding process for generation of RXD<3:0> to the MII. For side-stream descrambling, the MASTER PHY shall employ the following receiver descrambler generator polynomial:

$$g'_M(x) = 1 + x^{20} + x^{33}$$

and the SLAVE PHY shall employ the following receiver descrambler generator polynomial:

$$g'_S(x) = 1 + x^{13} + x^{33}$$

164.3.4.4 PCS Receive automatic polarity detection

An automatic polarity detection and correction shall be implemented on the receive side of both, master and slave PHY.

Polarity can be automatically detected in a recursive process: one assumption of polarity is made first and the descrambler synchronization is monitored within a certain period to determine whether such an assumption is correct; if not, the same procedure is repeated with a different polarity assumption and vice versa.

Receive polarity detection and correction can be done simultaneously at the earliest link up stages. Link up starts with the MASTER PHY sending symbols to the SLAVE PHY. If a polarity flip is detected, the SLAVE changes the sign of its received signals (RA_n, RB_n, RC_n) to correct the polarity. There is no change in the polarity of the transmit signal. After the SLAVE PHY has started transmission, the MASTER PHY can use the same method for determining its receive polarity.

164.3.5 PCS Loopback

The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, is set to a one (or PCS loopback mode is enabled by a similar functionality if MDIO is not implemented). In this mode, the PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII. Additionally, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII shall not result in the transmission of data on the network medium. The PCS loopback data flow is illustrated in figure 164-9.

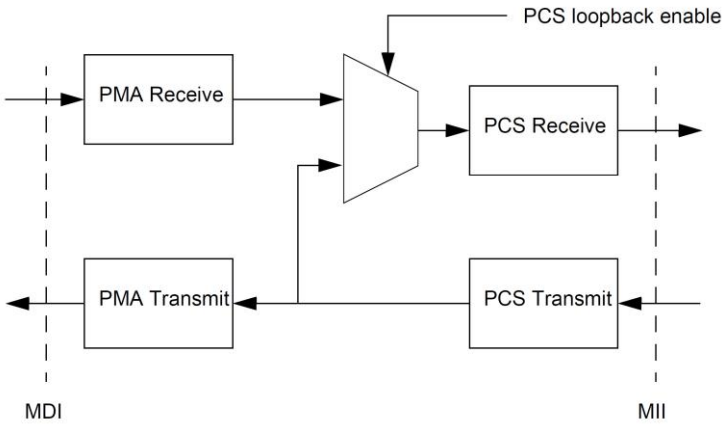


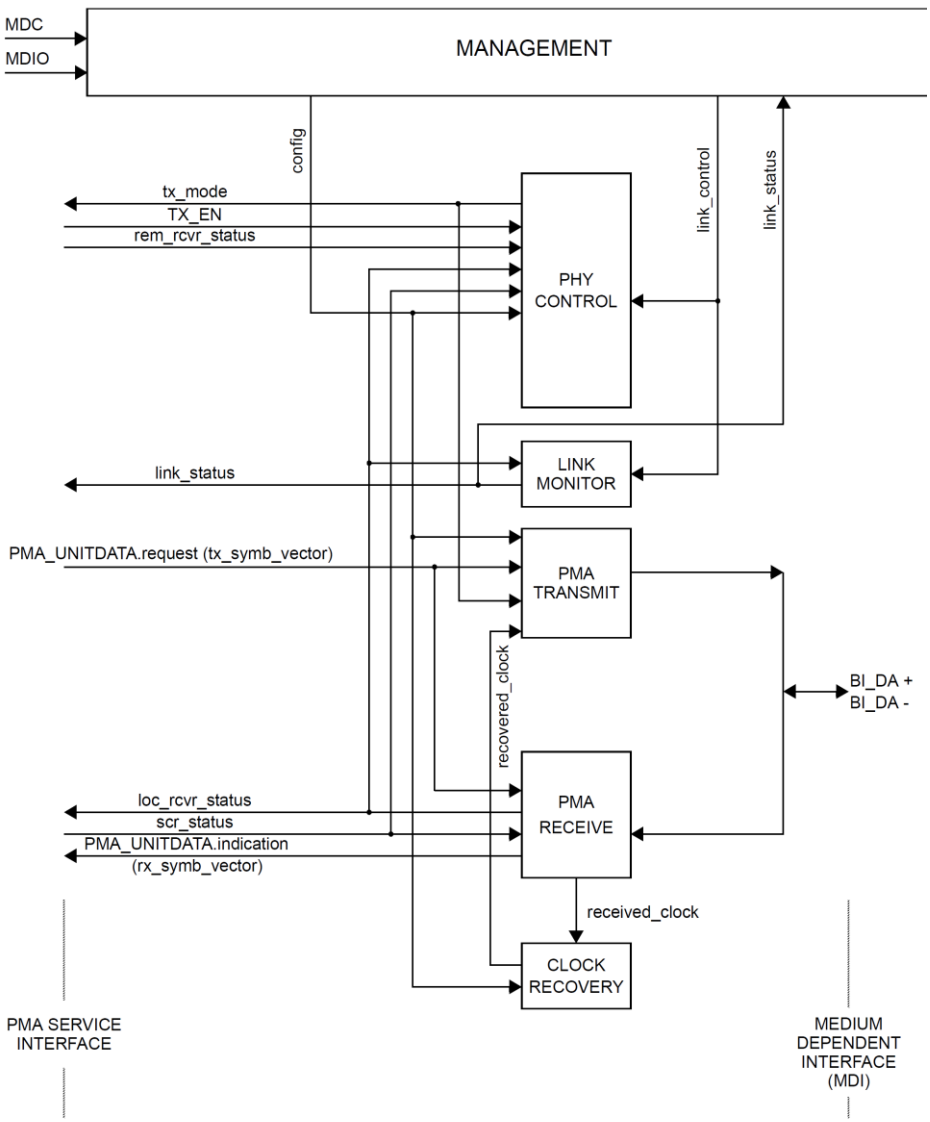
Figure 164-9 PCS Loopback data flow

The MAC compares the packets sent through the MII Transmit function to the packets received from the MII Receive function to validate the functionality of 10BASE-T1L PCS functions.

164.4 Physical Medium Attachment (PMA) Sublayer

The PMA couples messages from the PMA service interface specified in 164.2.1 onto the 10BASE-T1L physical medium, and provides the link management and PHY Control functions. The PMA provides full duplex communications to and from medium employing 3-level Pulse Amplitude Modulation (PAM3). The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 164.8.

PMA functions are illustrated in figure 164-10.



NOTE: The recovered_clock arc shown indicates delivery of the recovered clock back to PMA TRANSMIT for loop timing.

Figure 164-10 PMA functional block diagram

164.4.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power on (see 36.2.5.1.3).
b) The receipt of a request for reset from the management entity.

PMA Reset shall set pcs_reset = ON while any of the above reset conditions hold true. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

164.4.2 PMA Transmit function

Figure 164-11 illustrates the signal flow of the 10BASE-T1L PMA Transmit function. During transmission, PMA_UNITDATA.request conveys to the PMA using tx_symb_vector the value of the symbols to be sent over the single transmit pair.

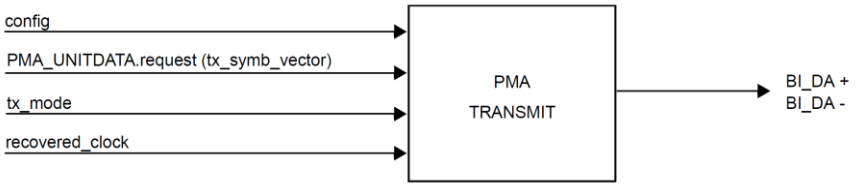


Figure 164-11 PMA Transmit

A single transmitter is used to generate the PAM3 signal BI_DA on the wire, using the transmit clock, TX_TCLK (see 164.5.4.5). When the config parameter is set to MASTER, the PMA Transmit Function derives the TX_TCLK from a local clock source. When the config parameter is set to SLAVE, the PMA Transmit Function derives the TX_TCLK from the recovered clock.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

164.4.3 PMA Receive function

Figure 164-12 illustrates the signal flow of the 10BASE-T1L PMA Receive function.

The 10BASE-T1L PMA Receive function comprises a single receiver (PMA Receive) for PAM3 modulated signals on a single balanced pair, BI_DA. PMA Receive has the ability to translate the received signals on the single pair into the PMA_UNITDATA.indication parameter rx_symb_vector. It detects ternary symbol sequences from the signals received at the MDI and presents these sequences to the PCS Receive function. The parameter loc_rcvr_status is generated by PMA Receive to indicate the status of the receive link at the local PHY. This variable indicates to the PCS Transmitter, PCS Receiver, PMA PHY Control function and Link Monitor whether the status of the overall received link is ok or not. Signal scr_status is generated by the PCS Receiver to indicate the status of the descrambler to the local PHY. It conveys the information on whether the scrambler has achieved synchronization or not to the PMA receive function.

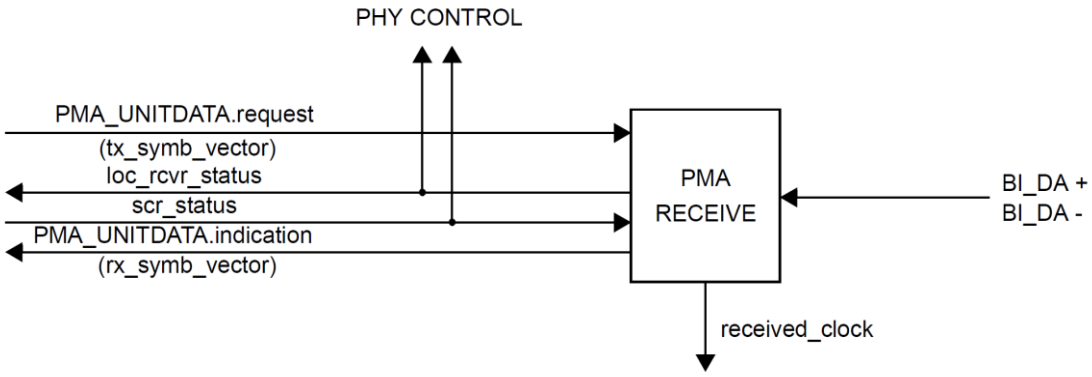


Figure 164-12 PMA Receive

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = Fail and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5.

164.4.4 PHY Control function

For the 10BASE-T1L PHY, FORCE mode or AUTONEG mode can be used to achieve link acquisition between two 10BASE-T1L link partners. Using FORCE mode, PMA_CONFIG is pre-determined to be MASTER or SLAVE via management control during initialization or via default hardware set-up. Using AUTONEG mode, PMA_CONFIG is determined during the auto-negotiation process.

The PHY Control functions block governs the control actions needed to bring the PHY into the 10BASE-T1L mode of operation so that frames can be exchanged with the link partner. PMA PHY Control also generates the signals that control PCS and PMA sublayer operations. It determines whether the PHY operates in the normal mode, enabling data transmission over the link segment, or whether the PHY sends idle data. PHY Control shall comply with the state diagram shown in Figure 164-13. PHY Control sets tx_mode to SEND_N (transmission of normal MII Data Stream, Control Information, or Idle Data), SEND_I (transmission of Idle Data), or SEND_Z (transmission of zero symbol vectors).

There shall be two startup sequences, depending on which training time is needed during the startup. If there is no predetermined configuration available, the maximum time, until link_status = OK is reached, shall be less than TBD (suggested are 3000 ms). If there is a predetermined configuration available (a set of valid filter coefficient is available), the maximum time from power_on = FALSE to link_status = OK shall be less than 100 ms.

Note: Fast startup is expected to be limited to very short link segment length only, where a predetermined configuration is available and where the change in ambient conditions has no significant influence on the available predetermined configuration or filter coefficient set.

164.4.5 Link Monitor function

Link Monitor operation, as shown in state diagram of Figure 164-14, shall be provided to support PHY Control. Variable link_control is set to ENABLE through management control during the PHY initialization or via default hardware set-up.

164.4.6 PMA clock recovery

This PMA function recovers the clock from the received stream. It is coupled to the receiver in order to provide for the SLAVE PHY a clock synchronous to the transmit clock of the MASTER PHY. PMA clock recovery outputs are also used as input variables for other PMA functions.

164.4.7 State variables

164.4.7.1 State diagram variables

pma_reset — Allows reset of all PMA functions.
Values: ON or OFF
Set by: PMA Reset.

link_control — This variable is generated by management or set by default.
Values: ENABLE or DISABLE.

config — The config parameter is set by management, set by default or set by auto-negotiation and passed to the PMA and PCS.
Values: MASTER or SLAVE.

link_status — This variable is generated by the PMA to indicate the status of the link.
Values: OK or FAIL.

loc_rcvr_status — Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive function for the local PHY.
Values: OK: The receive function for the local PHY is operating reliably.
NOT_OK: Operation of the receive function for the local PHY is unreliable.

rem_rcvr_status — Variable set by the PCS Receive function to indicate whether correct operation of the receive function for the remote PHY is detected or not.
Values: OK: The receive function for the remote PHY is operating reliably.
NOT_OK: Reliable operation of the receive function for the remote PHY is not detected.

scr_status — The scr_status parameter as communicated by the PMA_SCRSTATUS.request primitive.
Values: OK: The descrambler has achieved synchronization.
NOT_OK: The descrambler is not synchronized.

tx_mode — PCS Transmit sends code-groups according to the value assumed by this variable.
Values: SEND_N: This value is continuously asserted when transmitting data, control information or idle during normal operation.
SEND_I: This value is continuously asserted when transmitting idle data during training.
SEND_Z: This value is asserted when transmission of zero code-groups is to take place.

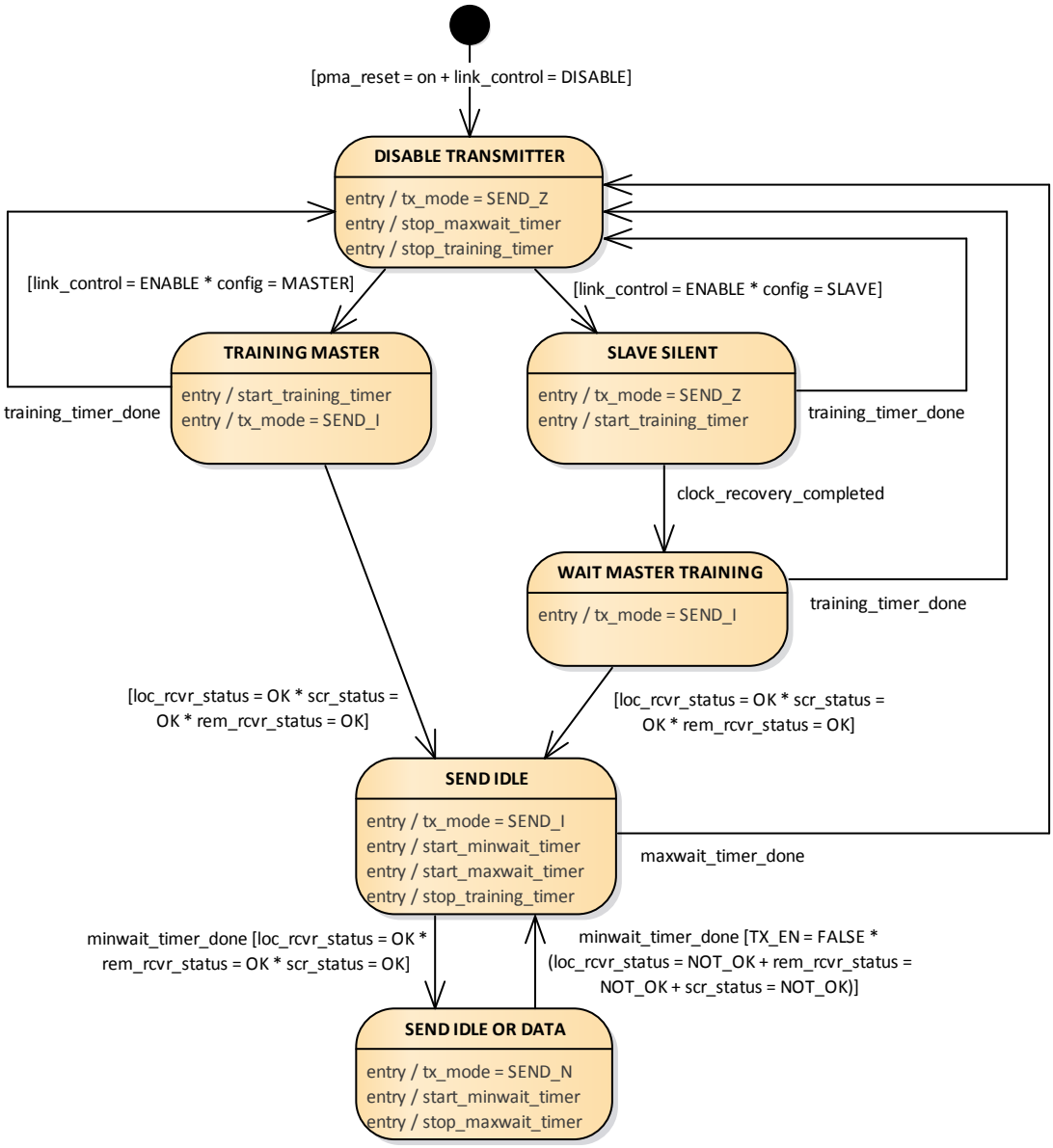


Figure 164-13 PHY Control state diagram

Note: The slave PHY stays in SLAVE SILENT state until the recovered clock is stable, so that the slave PHY can enable its transmitter to send idle data. Depending on the PHY implementation this can help to speed up the training process, as the slave PHY can already start the transmission before the equalizer training is finished. Alternatively the slave PHY can wait until loc_rcvr_status = OK, but this will add some extra time needed for the filter training within the slave PHY.

164.4.7.2 Timers

training_timer — A timer used to limit the maximum allowed training time of the receiver. The timer shall expire TBD (suggested are 3000 ms ± 30 ms, which is the expected maximum training time) after being started.

maxwait_timer — A timer used to limit the amount of time during which a receiver dwells in the SEND IDLE state. The timer shall expire TBD (suggested are 200 ms ± 2 ms, this is the maximum time the PHY should try to recover a failed link, e.g. during a power disturbance, before a complete retraining is started) after being started.

minwait_timer — A timer used to determine the minimum amount of time the PHY Control stays in the SEND IDLE or DATA states. The timer shall expire TBD (suggested are 20 µs ± 1 µs, this timer limits the toggle rate between "SEND IDLE" and "SEND IDLE OR DATA" states and allows stabilization of the status variables, the timer is chosen, in a way that a toggling to "SEND IDLE" and back does not destroy more than one 64 byte telegram) after being started.

Note: After a disturbance on the link segment, e.g. when the current consumption on a powered link segment is quickly changed, the PHYs may not immediately drop the link, but need to try to recover the link for some time, before doing a complete restart. Therefore the maxwait_timer allows the PHYs to stay for some time in the SEND IDLE state before going to the DISABLE TRANSMITTER state.

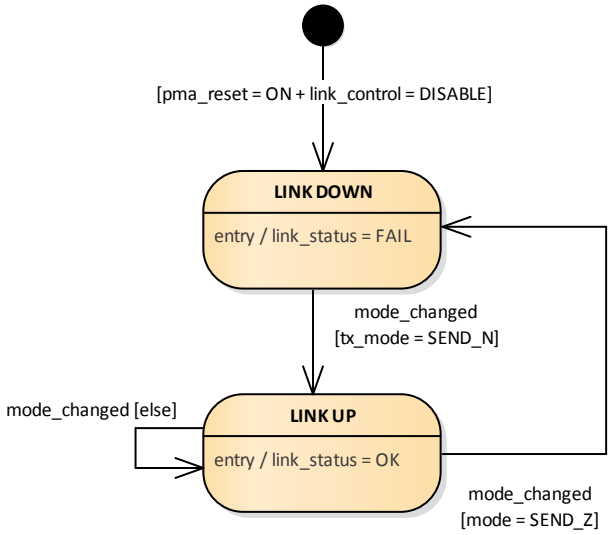


Figure 164-14 PHY Link Monitor state diagram

164.5 PMA electrical specifications

This sub clause defines the electrical characteristics of the PMA for a 10BASE-T1L Ethernet PHY.

164.5.1 EMC tests

EMC tests need to be discussed within the group.

Direct Power Injection (DPI) and 150 Ω emission tests for noise immunity and emission as per 164.5.1.1 and 164.5.1.2 may be used to establish a baseline for PHY EMC performance. These tests provide a high degree of repeatability and a good correlation to immunity and emission measurements. Additional tests may be needed to verify EMC performance in various configurations, applications, and conditions.

164.5.1.1 Immunity – DPI test

In a real application radio frequency (RF) common mode (CM) noise at the PHY is the result of electromagnetic interference coupling to the cabling system. Additional differential mode (DM) noise at the PHY is generated from the CM noise by mode conversion of all parts of the cabling system and the MDI. The sensitivity of the PMA's receiver to RF CM noise may be tested according to the DPI method of IEC 62132-4, and may need to comply with more stringent requirements as agreed upon between customer and supplier.

164.5.1.2 Emission – Conducted emission test

The emission of the PMA transmitter to its electrical environment may be tested according to the 150 Ω direct coupling method of IEC 61967-4, and may need to comply with more stringent requirements as agreed upon between customer and supplier.

164.5.2 Test modes

The test modes described in this sub clause shall be provided to allow testing of the transmitter waveform, transmitter distortion, transmitter jitter, and transmitter droop. The test modes can be enabled by setting bits 1.xxxx.xx:xx (10BASE-T1L PMA/PMD Test Control Register) of the PHY Management register set as described in 45.2.1.xxx. If MDIO is not implemented a similar functionality shall be provided by another interface. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

a) Test mode 1 – Transmitter output voltage, timing jitter, rise and fall times test mode
b) Test mode 2 – Transmitter output droop test mode

When test mode 1 is enabled, the PHY shall repeatedly transmit the data symbol sequence (+1, –1). See 164.5.4.5 for transmit clock requirements.

When test mode 2 is enabled, the PHY shall transmit ten "+1" symbols followed by ten "–1" symbols. This sequence is repeated continually.

164.5.3 Test fixture

The test fixture shown in figure 164-15, or its equivalent, is being used in the stated respective tests for measuring the transmitter specifications. The tolerance of the termination resistor shall be ± 0.1 %. All the transmitter tests are defined at the MDI.

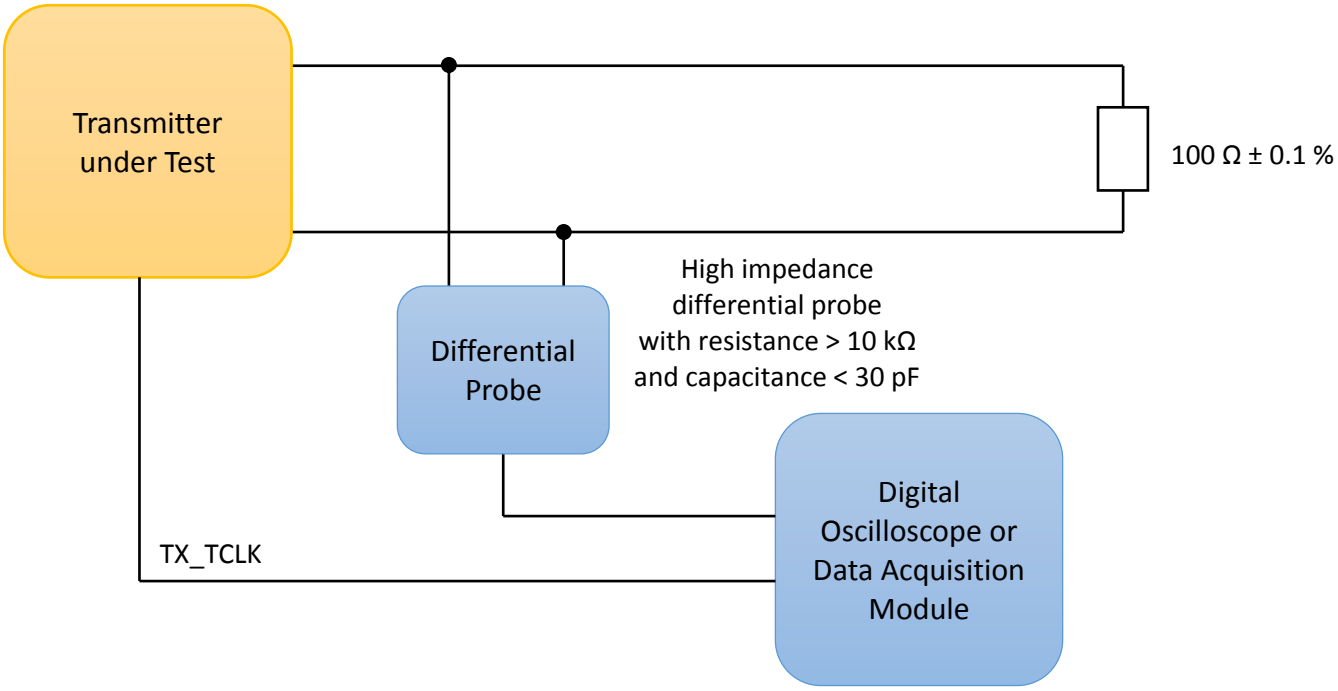


Figure 164-15 Test fixture

To allow an easy synchronization of the measurement equipment, the PHY shall provide access to the symbol rate clock TX_TCLK, which times the transmitted symbols. For a MASTER PHY this is the output of the (divided) clock oscillator, for the SLAVE PHY this is the recovered clock.

164.5.4 Transmitter electrical specifications

The PMA shall operate with AC coupling to the MDI. Where a load is not specified, the transmitter shall meet the requirements of this section with a 100 Ω ± 0.1 % resistive differential load connected to the transmitter output.

164.5.4.1 Transmitter output voltage

Transmitter output voltage shall be tested using test mode 1 in combination with the test fixture shown in figure 164-15. The transmitter output voltage shall be 2.4 V ± 5 % peak-to-peak in using normal driving levels and 1.0 V ± 5 % peak-to-peak using reduced driving levels. See also 164.5.4.6 for a normalized test pattern. Transmitter output voltage can be set using the management interface or by hardware default set-up. Additionally auto-negotiation can be used to find a common transmitter output voltage for the two PHYs.

Fixed transmitter driving levels can be selected by setting bits 1.xxxx.xx:xx (10BASE-T1L PMA/PMD Control Register) of the PHY Management register set as described in 45.2.1.xxx. If MDIO is not implemented a similar functionality shall be provided by another interface. Default setting is to use auto-negotiation.

Note: Using reduced driving levels reduces the power consumption of the PHY and allows the use of the PHY in intrinsically safe link segments, but reduces also the maximum possible link segment length. A transmitter output amplitude of 1 V peak-to-peak instead of 2.4 V peak-to-peak reduces the transmit power of the PHY by approx. 8 dB, thus allowing only a shorter link segment length assuming the same noise tolerance.

164.5.4.2 Transmitter output droop

Transmitter output droop shall be tested using test mode 2 in combination with the test fixture shown in figure 164-15. The transmitter output droop shall be less than TBD (suggested are 20 %) taking the inner TBD (suggested are 9 bit times) of the TBD (suggested are 10 bit times) pulse duration. See also 164.5.4.6 for a normalized test pattern.

This test is currently specified for 10 bit time long pulse durations. Maximum pulse length in a 4B3T coded system would be 5 bit times. We could also go to 5 Bit times, and then specifying a maximum of 10 % droop instead of 20 %. Taking 10 bit times could make the measurement easier as there is a higher deviation visible.

164.5.4.3 Transmitter timing jitter

The transmitter symbol-to-symbol jitter shall be tested using test mode 1 in combination with the test fixture shown in figure 164-15. The maximum jitter at the transmitter side shall be less than ± 10 ns symbol-to-symbol jitter (even if we adopted this already, likely we should change this to a smaller jitter tolerance, e.g. 2.5 ns or even 1 ns as it is an echo cancelled system, needs further investigation).

164.5.4.4 Transmitter rise and fall times

The transmitter rise and fall times shall be tested using test mode 1 in combination with the test fixture shown in figure 164-15. The nominal rise time of the signal shall be TBD (suggested are 53.333 ns ± 10 %) for a -1 to +1 and the nominal fall time of the signal shall be TBD (suggested are 53.333 ns ± 10 %) for a +1 to -1 transition. As the rise and fall times are specified between 10 % and 90 % of the signal amplitude, assuming a linear transition between 0 % and 100 %, this equals to a time of TBD (suggested is half of a symbol time).

Below 10 % and above 90 % of the signal amplitude a lower slew rate is acceptable, to consider the lower speed of the output driver when operating near to its supply rails. See also 164.5.4.6 for a normalized test pattern.

Needs to be checked, how this is done in other standards. Reason for the specification of the rise and fall time is, that especially taking short link segments into account, the clock regulation needs some defined rise/fall times (if there would be a sharp edge only and no pulse distortion over the link segment, then the clock regulation would get quite unstable, as there is only a small range for regulation (at one point everything is ok and just slipping the sample point a little, there would be a bit error).

164.5.4.5 Transmit clock frequency

The symbol transmission rate of the MASTER PHY shall be within the range 7.5 MBd ± 50 ppm.

164.5.4.6 Normalized test patterns

The following test patterns can be used for the transmitter tests.

Figure 164-16 and table 164-5 show a simple test pattern for test mode 1. The pattern includes a ± 5 % amplitude tolerance, ± 10 ns symbol-to-symbol jitter and the specified rise and fall times including tolerances. The test pattern is normalized, which means that the limit values have to be multiplied with

2.4 V, when using normal transmitter driving levels or with 1.0 V, when using reduced transmitter driving levels.

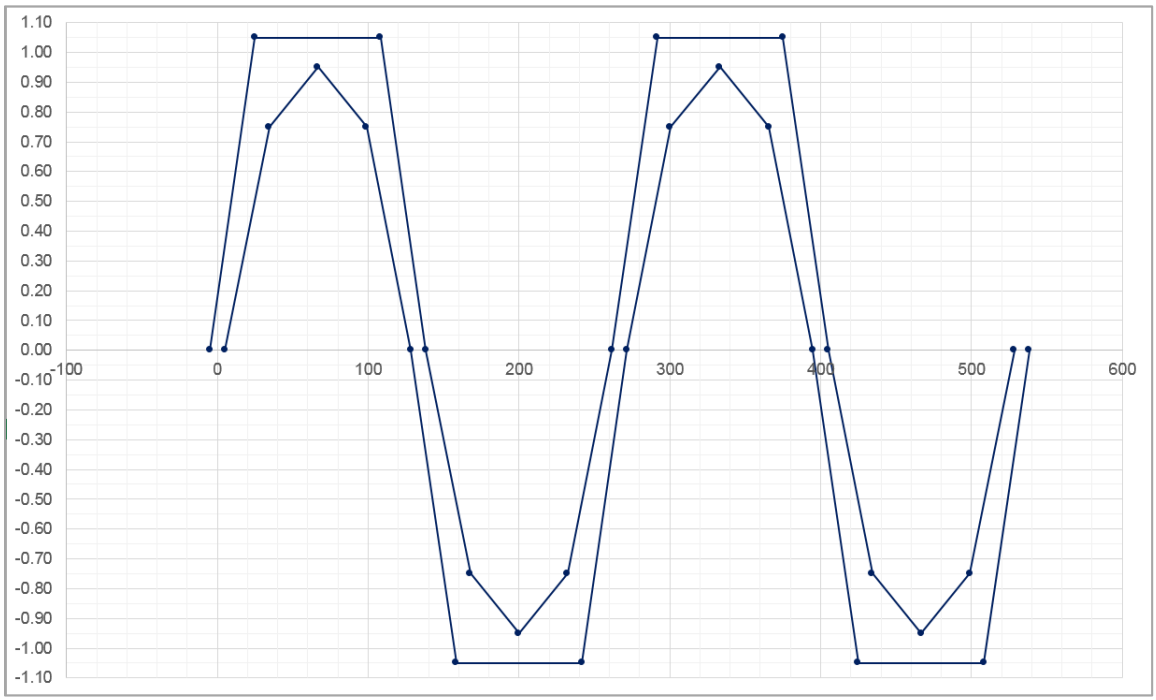


Figure 164-16 Test mode 1 limits

Limit 1 Time [ns]	Limit 1 Normalized Amplitude	Limit 2 Time [ns]	Limit 2 Normalized Amplitude
-5.000	0.00	5.000	0.00
25.000	1.05	34.333	0.75
108.333	1.05	66.667	0.95
138.333	0.00	99.000	0.75
167.667	-0.75	128.333	0.00
200.000	-0.95	158.333	-1.05
232.333	-0.75	241.667	-1.05
261.667	0.00	271.667	0.00
291.667	1.05	300.333	0.75
375.000	1.05	333.333	0.95
405.000	0.00	365.666	0.75
434.333	-0.75	395.000	0.00
466.667	-0.95	425.000	-1.05
499.000	-0.75	508.333	-1.05
528.333	0.00	538.333	0.00

Table 164-5 Test mode 1 limits

Figure 164-17 and table 164-6 shows a simple test pattern for test mode 2. The pattern includes a ± 5 % amplitude tolerance, ± 10 ns symbol-to-symbol jitter, the specified rise and fall times including tolerances as well as the allowed signal droop. The test pattern is normalized, which means that the limit values have

to be multiplied with 2.4 V, when using normal transmitter driving levels or with 1.0 V, when using reduced transmitter driving levels.

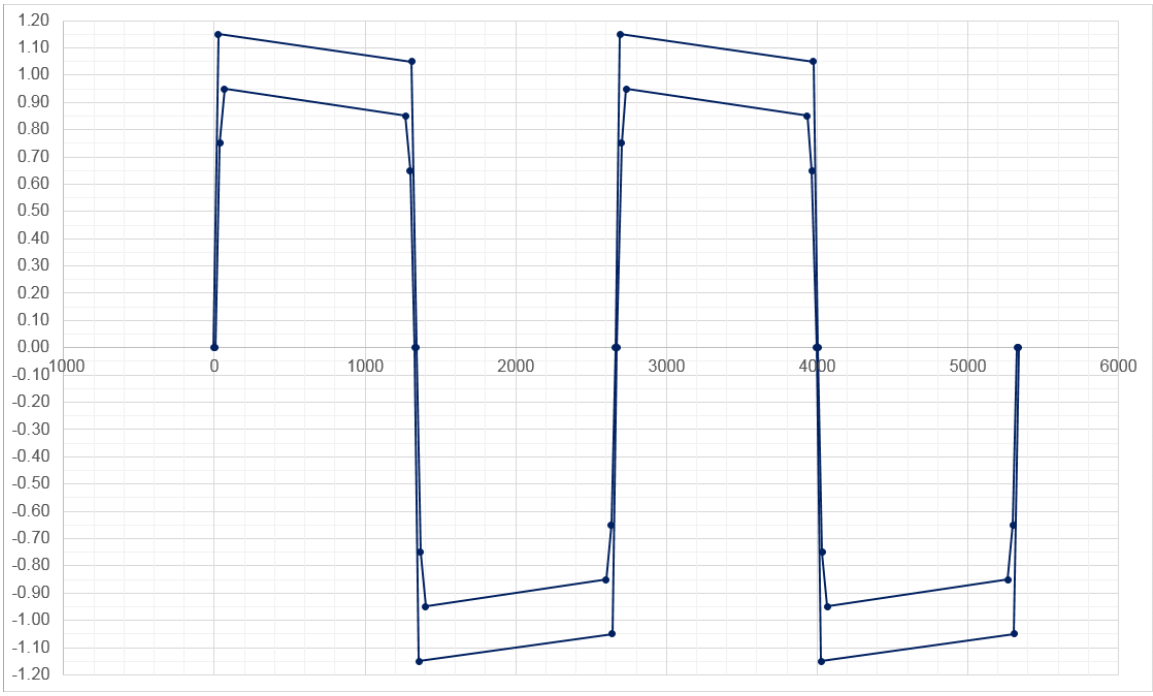


Figure 164-17 Test mode 2 limits

Limit 1 Time [ns]	Limit 1 Normalized Amplitude	Limit 2 Time [ns]	Limit 2 Normalized Amplitude
-5.000	0.00	5.000	0.00
25.000	1.15	34.333	0.75
1308.333	1.05	66.667	0.95
1338.333	0.00	1266.667	0.85
1367.667	-0.75	1299.000	0.65
1400.000	-0.95	1328.333	0.00
2600.000	-0.85	1358.333	-1.15
2632.333	-0.65	2641.667	-1.05
2661.667	0.00	2671.667	0.00
2691.667	1.15	2701.000	0.75
3975.000	1.05	2733.333	0.95
4005.000	0.00	3933.333	0.85
4034.333	-0.75	3965.667	0.65
4066.667	-0.95	3995.000	0.00
5266.667	-0.85	4025.000	-1.15
5299.000	-0.65	5308.333	-1.05
5328.333	0.00	5338.333	0.00

Table 164-6 Test mode 2 limits

164.5.5 Receiver electrical specifications

The PMA shall meet the Receive function specified in PMA Receive function and the electrical specifications of this section. The single balanced pair cabling system used in test configurations shall be within the limits specified in 164.7.

164.5.5.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of Transmitter Electrical Specifications and have passed through a link specified in 164.7, shall be received with a bit error ratio less than 10^{-9}.

164.5.5.2 Receiver frequency tolerance

The receiver feature shall properly receive incoming data with a symbol rate within the range 7.5 MBd ± 50 ppm.

164.5.5.3 Alien crosstalk noise rejection

This specification is provided to verify the DUT's tolerance to alien crosstalk noise using two separate tests. The first test is performed with a noise source consisting of a 10BASE-T1L compliant transmitter sending idle symbols (e.g. a MASTER PHY in training mode). The level of the noise at the MDI is nominally TBD (suggested are 20 mV, needs further analysis) peak-to-peak.

The second test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwidth of TBD (suggested are 10 MHz) and magnitude of TBD (suggested are -64 dBm/Hz, needs further analysis). The receive DUT is connected to these noise sources through a resistive network, as shown in figure 164-18, with a link segment as defined in 164.7. The noise is added at the MDI of the DUT. The BER shall be less than 10^{-9}, and to satisfy this specification the frame error ratio is less than 10^{-6} for 125 octet packets measured at MAC/PLS service interface.

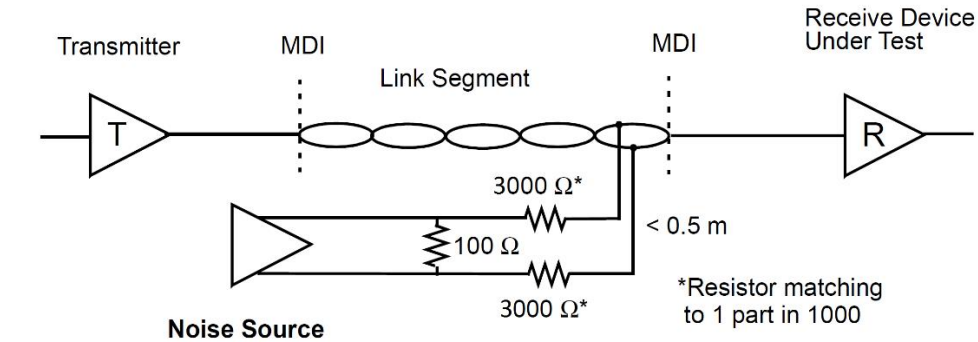


Figure 164-18 Alien crosstalk noise test (needs further analysis)

Note: If the output level is too high for the noise generator the resistor divider network may be adopted to allow for a lower noise generator output level. The noise signal fed into the receiver shall have a magnitude of TBD (suggested are

-106 dBm/Hz, needs further analysis) with a bandwidth of TBD (suggested are 10 MHz) taking the 100 ohm termination within the PHY into account.

We need to discuss, which tests we want to specify here (if the tests make sense or if there are better tests to use). There is not too much headroom to the specified values, testing this with the current evaluation boards (as the worst-case IL of a link segment is approx. 26 dB @ 3.75 MHz over 1000 m, the resulting signal amplitude at the receiver side is approx. 60 mV between two PAM-3 symbol levels).

164.5.6 Transmitter peak differential output

When measured with 100 Ω ± 0.1 % termination, transmit differential signal at MDI shall be less than TBD (suggested are 2.76 V peak-to-peak) for the normal driving levels and TBD (suggested are 1.15 V peak-to-peak) for the reduced driving levels including the signal droop. This limit applies to all transmit modes including SEND_I and SEND_N modes.

The maximum values are based on the droop test limits, specified in figure 164-17, we could also think about having tighter tolerances here, as the maximum pulse length is only 5 bit times using a 4B3T encoding.

164.5.7 PMA Local Loopback

The PMA local loopback function is optional. If supported, the PMA shall be placed in local loopback mode when the PMA local loopback bit in MDIO register 1.0.0, defined in 45.2.1.1, is set to a one (or PMA loopback mode is enabled by a similar functionality if MDIO is not implemented). When the PHY is in the PMA local loopback mode the PMA Receive function utilizes the echo signals from the unterminated MDI and decodes these signals to pass the data back to the MII Receive interface. The data flow of the external loopback is shown in figure 164-19.

A MAC Client may compare the packets sent through the MII Transmit function to the packets received from the MII Receive function to validate the 10BASE-T1L PCS and PMA functions.

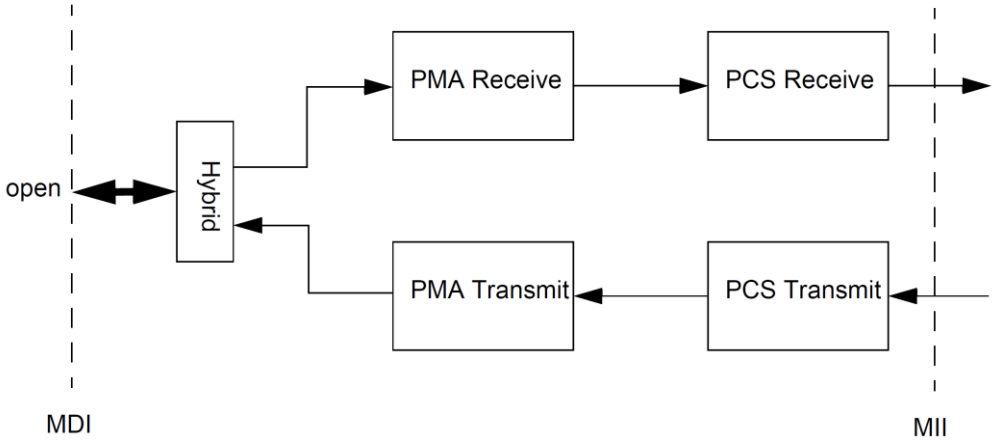


Figure 164-19 PMA loopback

164.6 Management interface

10BASE-T1L uses the management interface as specified in Clause 45. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended.

164.6.1 MASTER-SLAVE configuration

MASTER-SLAVE assignment for each link configuration is necessary for establishing the timing control of each PHY. In 10BASE-T1L, one PHY shall be configured as MASTER and one PHY shall be configured as SLAVE to operate. In the case where both PHYs are configured to be MASTER or both to be SLAVE, operation is undefined.

To Do: Define AUTONEG parameters and FORCE MODE options.

164.6.2 PHY initialization

Both PHYs sharing a link segment are capable of being MASTER or SLAVE. A forced assignment scheme or an auto-negotiation process is employed depending on the use case of the PHY. This process is conducted at the power-up or reset condition. The station management systems can manually configure the 10BASE-T1L PHY to be MASTER or to be SLAVE (before the link acquisition process starts) or a hardware set-up using bootstrap options can be implemented.

When MDIO is implemented, MASTER/SLAVE mode can be selected by setting bits 1.xxxx.xx:xx (10BASE-T1L PMA/PMD Control Register) of the PHY Management register set as described in 45.2.1.xxx. If MDIO is not implemented, a similar functionality shall be provided by another interface. Default setting is to use auto-negotiation.

164.6.3 PMA and PCS MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA and PCS. When MDIO is implemented, mapping of MDIO register bits to PMA and PCS control/status variables is shown in Table 164-7. If no MDIO is implemented, a similar functionality shall be implemented to access the needed variables.

Register Name	Register/Bit Number	Control/Status Variable
PMA/PMD Control 1	1.0.15	pma_reset
PMA/PMD Control 1	1.0.0	PMA loopback
PCS Control 1	3.0.15	pcs_reset
PCS Control 1	3.0.14	PCS loopback
PMA/PMD Status 1	1.1.2	link_status

Table 164-7 MDIO Register bit mapping

164.7 Link segment characteristics

To Do: This chapter just reflects the link segment characteristics, where the 10BASE-T1L PHY is based on so far. The complete chapter will be rewritten later on.

The 10BASE-T1L PHY is designed to operate over a single balanced pair cabling system. The single balanced pair cable supports an effective data rate of 10 Mb/s in each direction simultaneously.

The link segment for a 10BASE-T1L PHY system is defined as in figure 164-20, which consists of up to 1000 m of single balanced pair cabling, with up to ten in-line connectors and two mating connectors.

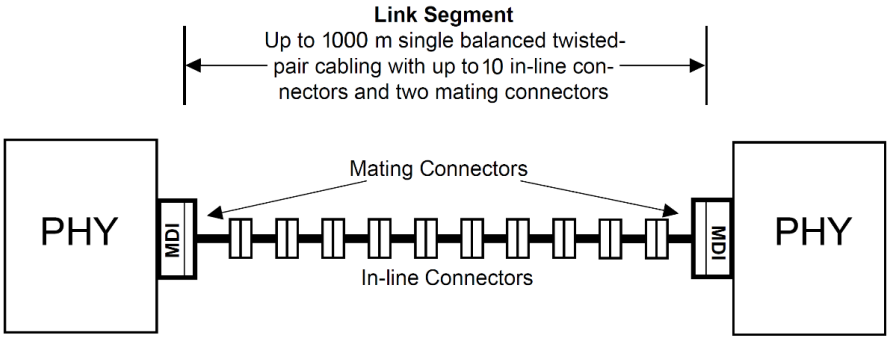


Figure 164-20 10BASE-T1L link segment definition

164.7.1 Cabling system characteristics

The cabling system used in figure 164-20 to support the 10BASE-T1L PHY is comprised of a single balanced pair cable up to 1000 m in length with associated connectors, and with impedance in the range of 80 Ω to 120 Ω (nominal 100 Ω) to support a data rate of 10 Mb/s in each direction simultaneously.

The transmission parameters contained in this specification are chosen to enable reliable operation over a single balanced pair cable link segment. The transmission parameters of the link segment include insertion loss, return loss, … additional parameters need to be added.

164.7.1.1 Characteristic impedance

The characteristic impedance of the cable and any mated MDI connector shall be 100 Ω ± 20 %.

164.7.1.2 Insertion loss

The insertion loss of the link segment shown in figure 164-20 when measured with a 100 Ω termination shall be less than that contained in equation (164-2) for a frequency between 100 kHz and 20 MHz:

$$Insertion\ Loss\ (f)[dB] \leq m \cdot \left(1.23 \cdot \sqrt{f} + 0.01 \cdot f + \frac{0.2}{\sqrt{f}}\right) + n \cdot 0.02 \cdot \sqrt{f} \qquad (164\text{-}1)$$

where m is the length in 100 m steps, n is the number of in-line connectors and f is the frequency in MHz.

The maximum insertion loss for a 1000 m link segment including 10 in-line connectors therefore shall be:

$$Insertion\ Loss\ (f)[dB] \leq 12.5 \cdot \sqrt{f} + 0.1 \cdot f + \frac{2}{\sqrt{f}} \qquad (164\text{-}2)$$

where f is the frequency in MHz.

Note: The insertion loss model fits to a shielded AWG18 cable using a foam PE insulation therefore providing low dielectric losses. Typically these cables have a temperature range for up to 75 °C. Cables for a temperature range of up to 90 °C typically use a solid wire insulation and therefore have significantly higher dielectric losses. Measurements show, that these cables within the interesting frequency range typically have at least two times the insertion loss of a foam PE insulated cable, thus reducing the maximum possible length of a link segment using such a cable to typically 500 m.

164.7.1.3 Return loss

The return loss of the link segment in figure 164-20 shall meet or exceed equation (164-3) for all frequencies from 100 kHz to 20 MHz (with 100 Ω reference impedance).

$$Return\ Loss \geq 14\ dB \qquad (164\text{-}3)$$

Note: Using a short cable (with no insertion loss) with a characteristic impedance of 80 ohms, will cause reflections on both ends, leading to a return loss of 14 dB.

To Do: Describe other relevant link segment parameters.

164.7.2 Noise environment

To Do: Describe the relevant noise environment parameters.

164.8 MDI specification

This section defines the MDI for 10BASE-T1L.

164.8.1 MDI connectors

The mechanical interface to the balanced cabling is a 3-pin connector (BI_DA+, BI_DA-, and SHIELD) or alternatively a 2-pin connector with an additional mechanical shield connection which conforms to the link segment specification defined in 164.7.

For industrial applications also a four pin M8 (acc. to IEC 61076-2-101) and M12 (acc. to IEC 61076-2-104) or a four pin 7/8” connector may be used (pinout has to be defined) as long as it conforms to the requirements of the link segment defined in 164.7.

Alternatively for applications with lower environmental requirements a standard RJ45 connector may be used. In this case pin 4 (BI_DA+) and pin 5 (BI_DA-) of the RJ45 connector shall be used (pinout needs to be discussed by the group, pin 4 and 5 in RJ45 connectors typically provide best EMC behavior).

164.8.2 MDI return loss

The MDI return loss (RL) shall meet or exceed equation 164-4 for all frequencies from TBD to TBD (suggested are 100 kHz to 20 MHz, but needs further analysis/discussions) (with 100 Ω ± 0.1 % reference impedance) at all times when the PHY is transmitting data or control symbols.

$$MDI\ Return\ Loss(f)\ \geq TBD \qquad (164\text{-}4)$$

Suggested is, but needs further analysis:

$$MDI\ Return\ Loss(f)\ \geq \begin{cases} 20\ dB & for\ 0.1\ MHz\ \leq f\ \leq 1\ MHz \\ 20\ dB\ -16\ dB \cdot log_{10}\left(\frac{f_{MHz}}{1\ MHz}\right) & for\ 1\ MHz\ < f\ \leq 20\ MHz \end{cases}$$

These values are based on the MDI return loss presentation held in Berlin meeting as a first base, there is need for further analysis/discussions.

164.8.3 MDI fault tolerance

For industrial applications the wire pair of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential or positive voltages of up to TBD (suggested are 60 V dc, see note below) with the source current limited to TBD (suggested are 1200 mA, see note below), as per Table 164-7, for an indefinite period of time. Normal operation shall resume after the short circuit(s) is/are removed.

For automotive applications the wire pair of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential or positive voltages of up to TBD (suggested are 50 V dc, see other automotive specs) with the source current limited to TBD (suggested are 150 mA, see other automotive specs), as per Table 164-7, for an indefinite period of time. Normal operation shall resume after the short circuit(s) is/are removed.

The wire pair of the MDI shall also withstand without damage high-voltage transient noises and ESD per application requirements.

BI_DA+	**BI_DA-**
No fault	No fault
BI_DA-	BI_DA+
Ground	No fault
No fault	Ground
+50/60 V dc	No fault
No fault	+50/60 V dc
Ground	+50/60 V dc
+50/60 V dc	Ground

Table 164-7 Fault conditions

Note: Typically industrial control circuits are SELV/PELV limited to a maximum voltage of 60 V. The maximum current is limited by the 50 ohm termination resistors in each signal line. Depending on the internal structure of the PHY IC additional external clamping diodes could be necessary. Due to the AC signal coupling the maximum current is only applied while charging the signal coupling capacitors.

164.9 Environmental specifications

164.9.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1 (for IT, industrial and motor vehicle applications), to IEC 61010-1 (for industrial applications only, if required by the given application) and to ISO 26262 (for motor vehicle applications only, if required by the given application). All equipment subject to this clause may be additionally required to conform to any applicable local, state, or national standards or as agreed to between the customer and supplier.

164.9.2 Network safety

To Do.

164.9.2.1 Environmental safety

To Do.

164.9.2.2 Electromagnetic compatibility

To Do.

164.10 Delay constraints

Every 10BASE-T1L PHY associated with MII shall comply with the bit delay constraints for full duplex operation. The delay for the transmit path, from the MII input to the MDI, shall be less than TBD (suggested are 3.2 µs (32 bit times), current implementation on evaluation board takes about 20 bit times maximum). The delay for the receive path, from the MDI to the MII output, shall be less than TBD (suggested are 6.4 µs (64 bit times), current implementation on evaluation board takes about 50 bit times maximum, as there are no high latency encoders/decoders included within the PHY this allows to have a quite low latency).

Informative Annex

A.1 Intrinsically safe applications

Intrinsically safe systems can be based on a 10BASE-T1L PHY, if the constraints described within this annex are taken into account.

When using a PHY IC within a PHY intended for the use in intrinsically safe applications, external termination resistors, outside of the PHY IC are recommended to be able to adopt the termination resistors in accordance with the used intrinsically safe concept and to limit the energy to/from the intrinsically safe link segment in case of a failure.

This would mean, that for such applications, separate pins for the differential transmit outputs and the differential receive inputs are recommended within a PHY IC.

The differential receive inputs should be high impedance, to allow external series resistors, to limit the energy being provided from/to the receive inputs to/from the intrinsically safe link segment in case of an internal failure of the PHY IC.

Further information about how to use a 10BASE-T1L PHY within intrinsically safe applications can be found in IEC 60079-0, IEC 60079-11 and other relevant national and international standards.

The figures A-1 and A-2 below show in principle two possible implementations on how to feed power onto an intrinsically safe link segment. The circuits should only be seen as examples. It is in the responsibility of the hardware designer to fulfill all relevant standards (especially IEC 60079-0 and 60079-11, but also others), when implementing devices for the use within intrinsically safe applications.

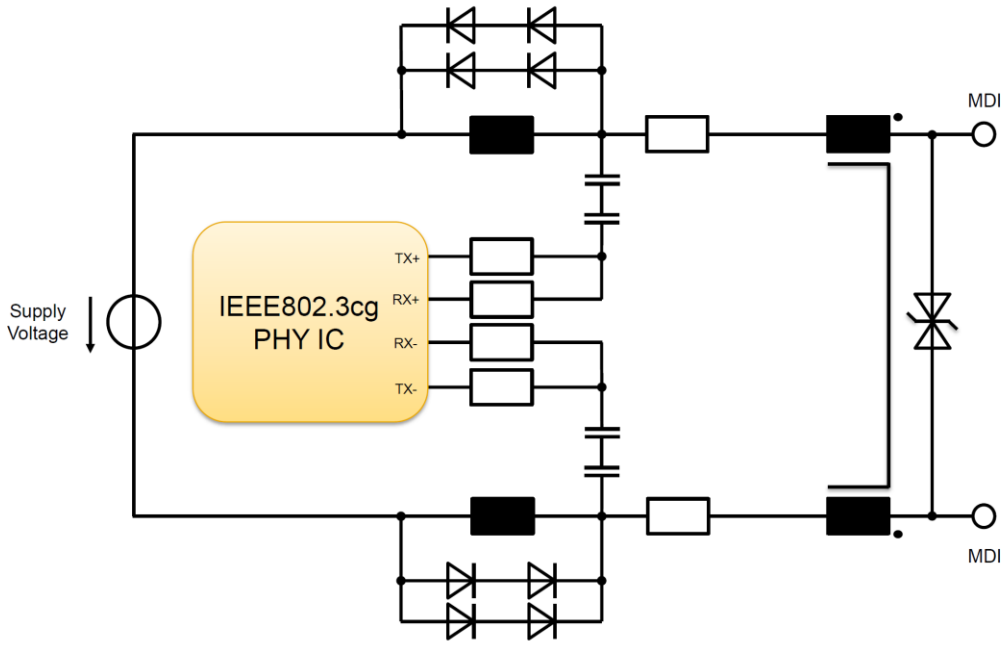


Figure A-1 First possible implementation on intrinsically safe power feeding side

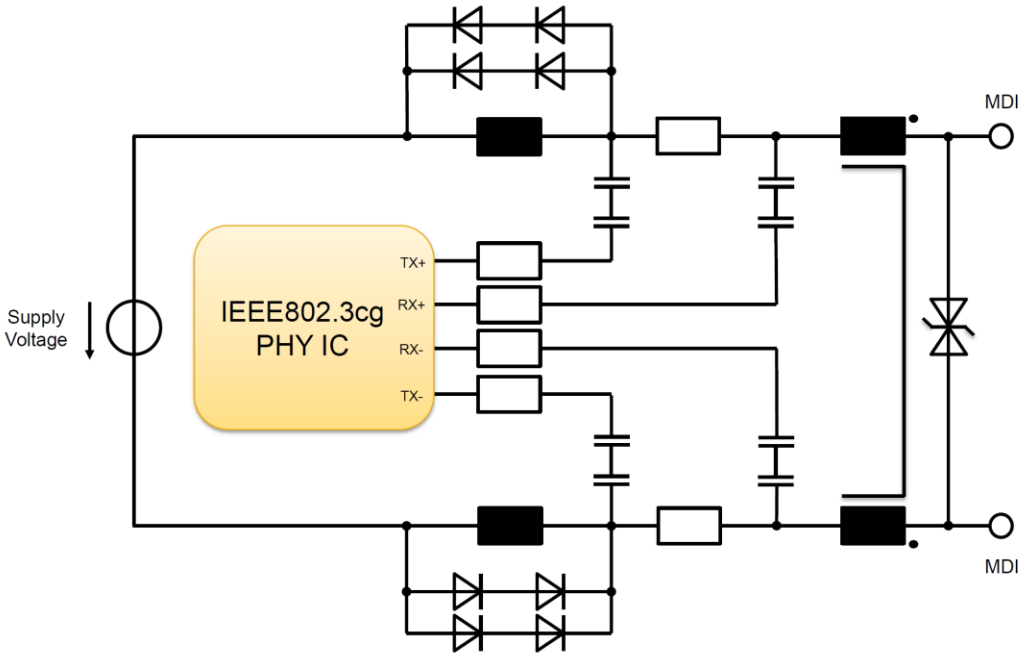


Figure A-2 Second possible implementation on intrinsically safe power feeding side

Note: Likely the second version is easier to implement within a PHY IC as the hybrid within the PHY IC needs not to be adopted to different external resistor values.

The figure A-3 below shows in principle a possible implementation on how to decouple the power from an intrinsically safe link segment. The circuit should only be seen as example. It is in the responsibility of the hardware designer to fulfill all relevant standards (especially IEC 60079-0 and 60079-11, but also others), when implementing devices for the use within intrinsically safe applications.

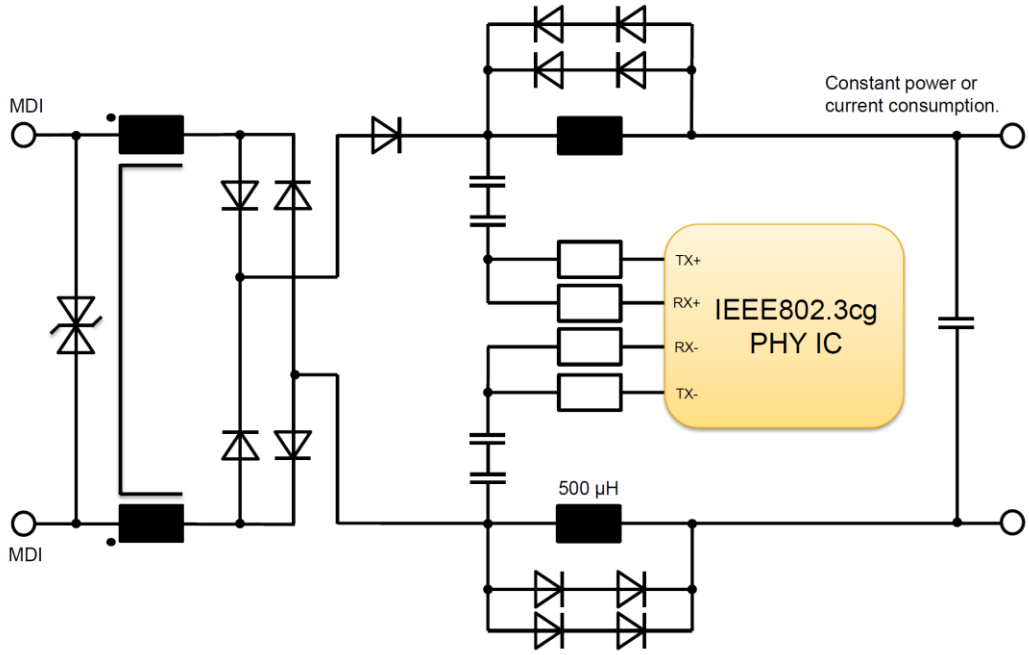


Figure A-3 Possible implementation for power decoupling from an intrinsically safe link segment