Evaluating the ADN4680E 250 Mbps, Half-Duplex, Quad M-LVDS Transceivers

FEATURES

- Easy evaluation of the ADN4680E 250 Mbps, half-duplex, quad M-LVDS transceivers
- Board layout optimized for high speed signaling
- Matched track lengths on M-LVDS differential pairs with controlled 100 Ω differential impedance
- Matched track lengths on high speed DIx and ROx logic signals with controlled 50 Ω impedance to GND
- SMA jacks for connecting to high speed DIx and ROx logic signals and M-LVDS Ax and Bx signals
- Optional screw terminal connectors for accessing the ROx, $\overline{REx}$, DEx, and DIx logic signals
- Power and ground connections through screw terminal blocks
- Jumper-selectable global power down via the ENP pin
- Jumper-selectable driver enable, receiver enable, and fail-safe for each transceiver via the $\overline{REx}$, DEx, and FSx pins
- Test points for measuring all signals and multiple ground points to facilitate probing of multiple signals
- 100 Ω termination resistors across Ax and Bx signals to simulate a terminated bus

EQUIPMENT NEEDED

- A 4 channel oscilloscope
- A signal generator
- A 3.0 V to 3.6 V power supply

EVALUATION KIT CONTENTS

- EVAL-ADN4680EEBZ

GENERAL DESCRIPTION

The EVAL-ADN4680EEBZ allows quick and easy evaluation of the ADN4680E 250 Mbps, half-duplex, quad multipoint, low voltage differential signaling (M-LVDS) transceivers. The EVAL-ADN4680EEBZ allows the input and output functions of each transceiver to be exercised without the need for external components. Subminiature A (SMA) connectors provide convenient connections for high speed logic and the M-LVDS bus signals. Screw terminal blocks are available to access power, ground, and digital signals. Jumper options allow control of each transceivers driver and receiver enable pins, each transceivers fail-safe functionality, and the global power-down mode.

The EVAL-ADN4680EEBZ is optimized for high speed signaling. The differential M-LVDS signal traces on the board are routed as a length matched 100 Ω differential pair. The DIx digital input and ROx receiver output are also length matched and routed with a controlled 50 Ω impedance to ground. The EVAL-ADN4680EEBZ features a solid ground and power plane for optimum power integrity.

The EVAL-ADN4680EEBZ has a footprint for the ADN4680E transceivers in a 7 mm × 7 mm, 48-lead LFCSP.

For full details on the ADN4680E, see the ADN4680E data sheet, which must be used in conjunction with this user guide when using the EVAL-ADN4680EEBZ.

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REVISION HISTORY

9/2021 —Revision 0: Initial Version

EVAL-ADN4680EEBZ EVALUATION BOARD PHOTOGRAPH

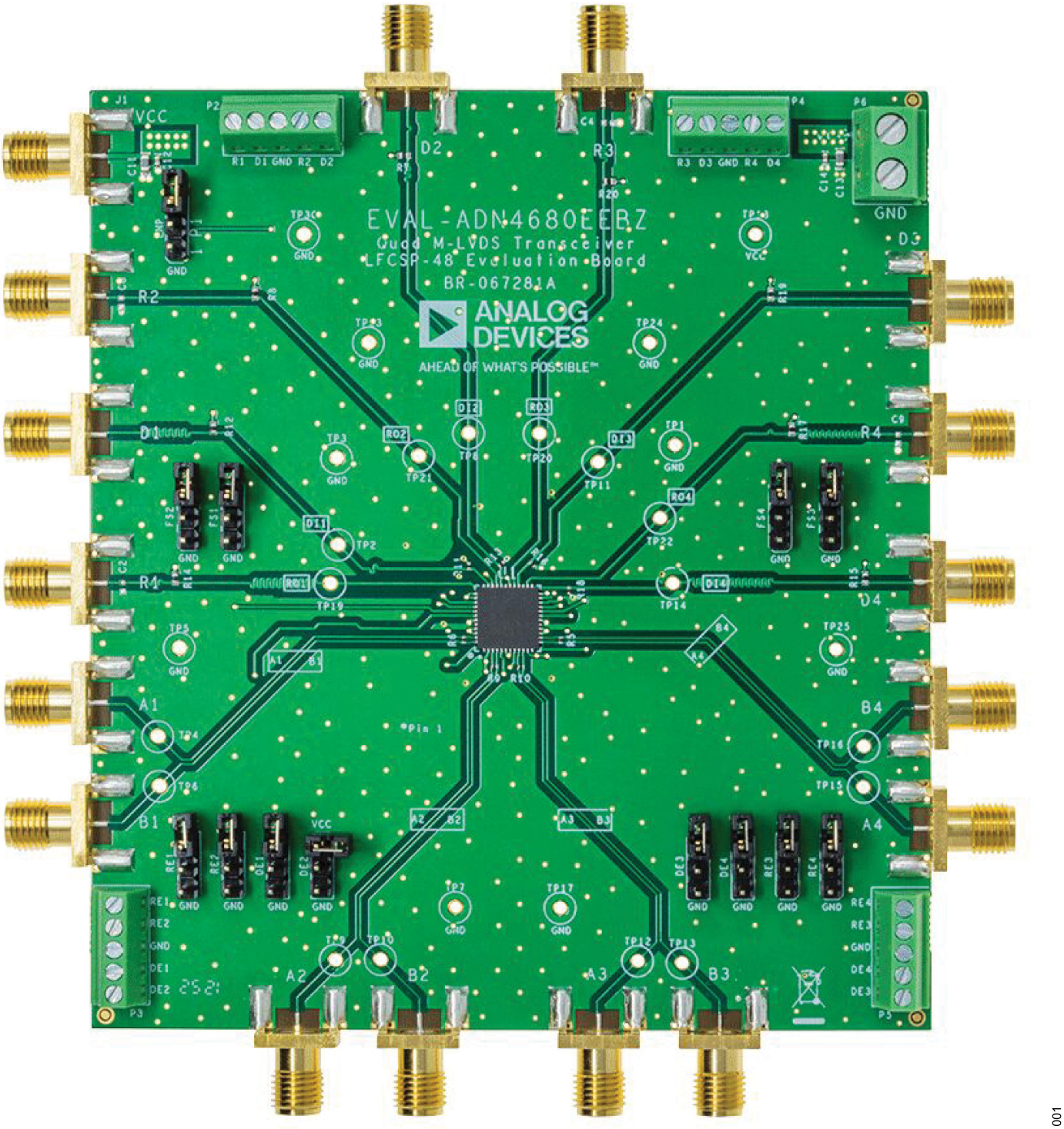

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Figure 1.

EVALUATION BOARD CONFIGURATION

SETTING UP THE EVALUATION BOARD

The EVAL-ADN4680EEBZ allows the ADN4680E to be quickly and easily evaluated. The EVAL-ADN4680EEBZ allows all of the input and output functions to be exercised without the need for external components. Jumper configurations are shown in Jumper Connections.

The EVAL-ADN4680EEBZ is powered by connecting a 3.3 V power supply to either the J1 VCC SMA connector or the VCC and GND connections of the P6 screw terminal block. The supply current is typically 8 mA with all drivers and receivers disabled. The C11 and C13, 10 µF decoupling capacitors and the C12 and C14, 100 nF decoupling capacitors are fitted at the VCC connectors. Several 100 nF decoupling capacitors are included at the supply pins of the ADN4680E.

Each half-duplex transceiver of the ADN4680E contains both a driver and receiver that can be individually enabled or disabled via jumper options. Each driver can be enabled or disabled via the DE1 to DE4 jumpers. Connect these jumpers to VCC to enable the respective driver, and connect these jumpers to GND to disable the respective driver. Similarly, each receiver can be enabled or disabled via the $\overline{RE1}$ to $\overline{RE4}$ jumpers. Connect these jumpers to GND to enable the respective receiver, and connect these jumpers to VCC to disable the respective receiver. The DE1 to DE4 and $\overline{RE1}$ to $\overline{RE4}$ signals can also be accessed via the P3 and P5 screw terminal blocks for dynamic control via a processor or a signal generator.

Each of the four receivers of the ADN4680E can be individually configured for Type 1 or Type 2 operation, using the FS1 to FS4 jumpers. Connecting an FSx jumper to GND configures the respective receiver for Type 1 operation, while removing the FSx jumper or connecting the FSx jumper to VCC configures that receiver for Type 2 operation.

The ADN4680E features a global device enable pin, ENP, that can be accessed via the P1 jumper. When this jumper is connected to GND, all drivers and receivers are disabled in a low power shutdown state. When this jumper is connected to VCC, the state of each transceiver is controlled via the DE1 to DE4 and $\overline{RE1}$ to $\overline{RE4}$ pins.

The ADN4680E high speed digital input signals, DI1 to DI4, and receiver output signals, RO1 to RO4, are routed on length matched traces with a 50 Ω characteristic impedance to GND. The DI1 to DI4 traces are terminated to GND with 50 Ω resistors, R11, R13, R16, and R18, respectively. The RO1 to RO4 traces include an optional placeholder for a load capacitor at C2, C8, C4, and C9, respectively. For optimum signal integrity, the DI1 to DI4 input signals and RO1 to RO4 output signals can be accessed via dedicated SMA connectors, D1 to D4 and R1 to R4. Alternatively the P2 and P4 screw terminal connectors can be used for easy wire connections to a microprocessor. The connections to the P2 and P4 screw terminal block are made via 0 Ω resistors, which can be removed to eliminate any stub lengths along the interconnect.

The M-LVDS input and output signals, A1 to A4 and B1 to B4, are accessed via SMA connectors. These A1 and B1, A2 and B2, A3 and B3, and A4 and B4 signals are routed as four length matched differential pairs with a differential characteristic impedance of 100 Ω. These signals are terminated at the Ax and Bx pins of the ADN4680E with 100 Ω resistors, R6, R9, R10, and R5, respectively.

An example evaluation of the ADN4680E driver and receiver is shown in Figure 2. A signal generator is connected via the D1 SMA connector to DI1 with an input signal of 125 MHz, a 50% duty cycle, and a swing of between 0 V and 3.3 V. The ENP jumper, P1, is connected to VCC to set the enable global device power-up. The DE1 jumper is set to VCC, and the RE2 jumper is set to GND, to enable the driver of Transceiver 1 and the receiver of Transceiver 2, respectively. The DE2 jumper is set to GND to disable the driver of Transceiver 2 to avoid bus contention. Jumper FS2 is set to GND to set the receiver of Transceiver 2 to Type 1 operation. The A1 SMA connector is connected to the A2 SMA connector, and the B1 SMA connector is connected to B2 SMA connector. In addition, oscilloscope probes are connected to DI1 (TP2), A2 (TP9), B2 (TP10), and RO2 (TP21).

EVALUATION BOARD CONFIGURATION

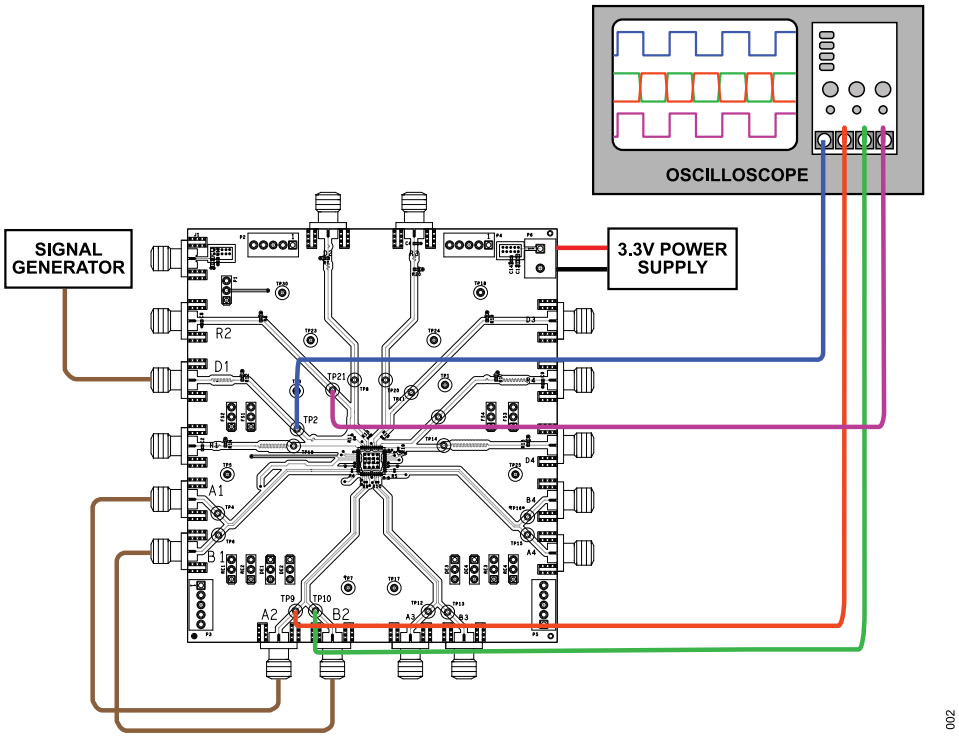

Figure 2. Example Evaluation of the ADN4680E Driver and Receiver

INPUT AND OUTPUT CONNECTIONS

Table 1 details the digital input connections, Table 2 details the digital output connections, and Table 3 details the M-LVDS input and output connections.

Table 1. Digital Input Connections

Connection	DI1	DI2	DI3	DI4	DE1	DE2	DE3	DE4	$\overline{RE1}$	$\overline{RE2}$	$\overline{RE3}$	$\overline{RE4}$
SMA Connector	D1	D2	D3	D4	None	None	None	None	None	None	None	None
Terminal Connector	P2 via R12	P2 via R7	P4 via R19	P4 via R15	P3	P3	P5	P5	P3	P3	P5	P5
Test Point	TP2	TP8	TP11	TP14	None	None	None	None	None	None	None	None
Termination Resistor	R11	R13	R16	R18	None	None	None	None	None	None	None	None

Table 2. Digital Output Connections

Connection	RO1	RO2	RO3	RO4
SMA Connector	R1	R2	R3	R4
Terminal Connector	P2 via R14	P2 via R8	P4 via R20	P4 via R17
Test Point	TP19	TP21	TP20	TP22
Load Capacitor	C2	C8	C4	C9

Table 3. M-LVDS Input and Output Connections

Connection	A1	B1	A2	B2	A3	B3	A4	B4
Test Point	TP4	TP6	TP9	TP10	TP12	TP13	TP15	TP16
Termination Resistor	R6		R9		R10		R5	

EVALUATION BOARD CONFIGURATION

JUMPER CONNECTIONS

Table 4 details the jumper configurations.

Table 4. Jumper Configurations

Jumper	Position	Description
ENP	VCC	Connects the ENP pin of the ADN4680E to VCC, which enables global power-up for the device. The state of each transceiver is determined by the DE1 to DE4 and $\overline{RE1}$ to $\overline{RE4}$ pins.
	GND	Connects the ENP pin of the ADN4680E to GND, which disables all transceivers on the device into a low power mode.
FS1	VCC	Connects the FS1 pin of the ADN4680E to VCC, which sets the RO1 receiver for Type 2 operation, supporting fail-safe.
	GND	Connects the FS1 pin of the ADN4680E to GND, which sets the RO1 receiver for Type 1 operation for maximum noise margin.
FS2	VCC	Connects the FS2 pin of the ADN4680E to VCC, which sets the RO2 receiver for Type 2 operation, supporting fail-safe.
	GND	Connects the FS2 pin of the ADN4680E to GND, which sets the RO2 receiver for Type 1 operation for maximum noise margin.
FS3	VCC	Connects the FS3 pin of the ADN4680E to VCC, which sets the RO3 receiver for Type 2 operation, supporting fail-safe.
	GND	Connects the FS3 pin of the ADN4680E to GND, which sets the RO3 receiver for Type 1 operation for maximum noise margin.
FS4	VCC	Connects the FS4 pin of the ADN4680E to VCC, which sets the RO4 receiver for Type 2 operation, supporting fail-safe.
	GND	Connects the FS4 pin of the ADN4680E to GND, which sets the RO4 receiver for Type 1 operation for maximum noise margin.
$\overline{RE1}$	VCC	Connects the $\overline{RE1}$ pin of the ADN4680E to VCC, which disables the RO1 receiver, placing it in a high impedance state.
	GND	Connects the $\overline{RE1}$ pin of the ADN4680E to GND, which enables the RO1 receiver if the ENP jumper is connected to VCC.
	Disconnected	Disconnects the $\overline{RE1}$ pin from VCC or GND, which allows the $\overline{RE1}$ pin to be controlled from the $\overline{RE1}$ connection on the P3 screw terminal block.
$\overline{RE2}$	VCC	Connects the $\overline{RE2}$ pin of the ADN4680E to VCC, which disables the RO2 receiver, placing it in a high impedance state.
	GND	Connects the $\overline{RE2}$ pin of the ADN4680E to GND, which enables the RO2 receiver if the ENP jumper is connected to VCC.
	Disconnected	Disconnects the $\overline{RE2}$ pin from VCC or GND, which allows the $\overline{RE2}$ pin to be controlled from the $\overline{RE2}$ connection on the P3 screw terminal block.
$\overline{RE3}$	VCC	Connects the $\overline{RE3}$ pin of the ADN4680E to VCC, which disables the RO3 receiver, placing it in a high impedance state.
	GND	Connects the $\overline{RE3}$ pin of the ADN4680E to GND, which enables the RO3 receiver if the ENP jumper is connected to VCC.
	Disconnected	Disconnects the $\overline{RE3}$ pin from VCC or GND, which allows the $\overline{RE3}$ pin to be controlled from the $\overline{RE3}$ connection on the P5 screw terminal block.
$\overline{RE4}$	VCC	Connects the $\overline{RE4}$ pin of the ADN4680E to VCC, which disables the RO4 receiver, placing it in a high impedance state.
	GND	Connects the $\overline{RE4}$ pin of the ADN4680E to GND, which enables the RO4 receiver if the ENP jumper is connected to VCC.
	Disconnected	Disconnects the $\overline{RE4}$ pin from VCC or GND, which allows the $\overline{RE4}$ pin to be controlled from the $\overline{RE4}$ connection on the P5 screw terminal block.
DE1	VCC	Connects the DE1 pin of the ADN4680E to VCC, which enables the A1 and B1 transmitter if the ENP jumper is connected to VCC.
	GND	Connects the DE1 pin of the ADN4680E to GND, which disables the A1 and B1 transmitter, placing it in a high impedance state.

EVALUATION BOARD CONFIGURATION

Table 4. Jumper Configurations

Jumper	Position	Description
	Disconnected	Disconnects the DE1 pin from VCC or GND, which allows the DE1 pin to be controlled from the DE1 connection on the P3 screw terminal block.
DE2	VCC	Connects the DE2 pin of the ADN4680E to VCC, which enables the A2 and B2 transmitter if the ENP jumper is connected to VCC.
	GND	Connects the DE2 pin of the ADN4680E to GND, which disables the A2 and B2 transmitter, placing it in a high impedance state.
	Disconnected	Disconnects the DE2 pin from VCC or GND, which allows the DE2 pin to be controlled from the DE2 connection on the P3 screw terminal block.
DE3	VCC	Connects the DE3 pin of the ADN4680E to VCC, which enables the A3 and B3 transmitter if the ENP jumper is connected to VCC.
	GND	Connects the DE3 pin of the ADN4680E to GND, which disables the A3 and B3 transmitter, placing it in a high impedance state.
	Disconnected	Disconnects the DE3 pin from VCC or GND, which allows the DE3 pin to be controlled from the DE3 connection on the P5 screw terminal block.
DE4	VCC	Connects the DE4 pin of the ADN4680E to VCC, which enables the A4 and B4 transmitter if the ENP jumper is connected to VCC.
	GND	Connects the DE4 pin of the ADN4680E to GND, which disables the A4 and B4 transmitter, placing it in a high impedance state.
	Disconnected	Disconnects the DE4 pin from VCC or GND, which allows the DE4 pin to be controlled from the DE4 connection on the P5 screw terminal block.

EVALUATION BOARD SCHEMATIC AND LAYOUT

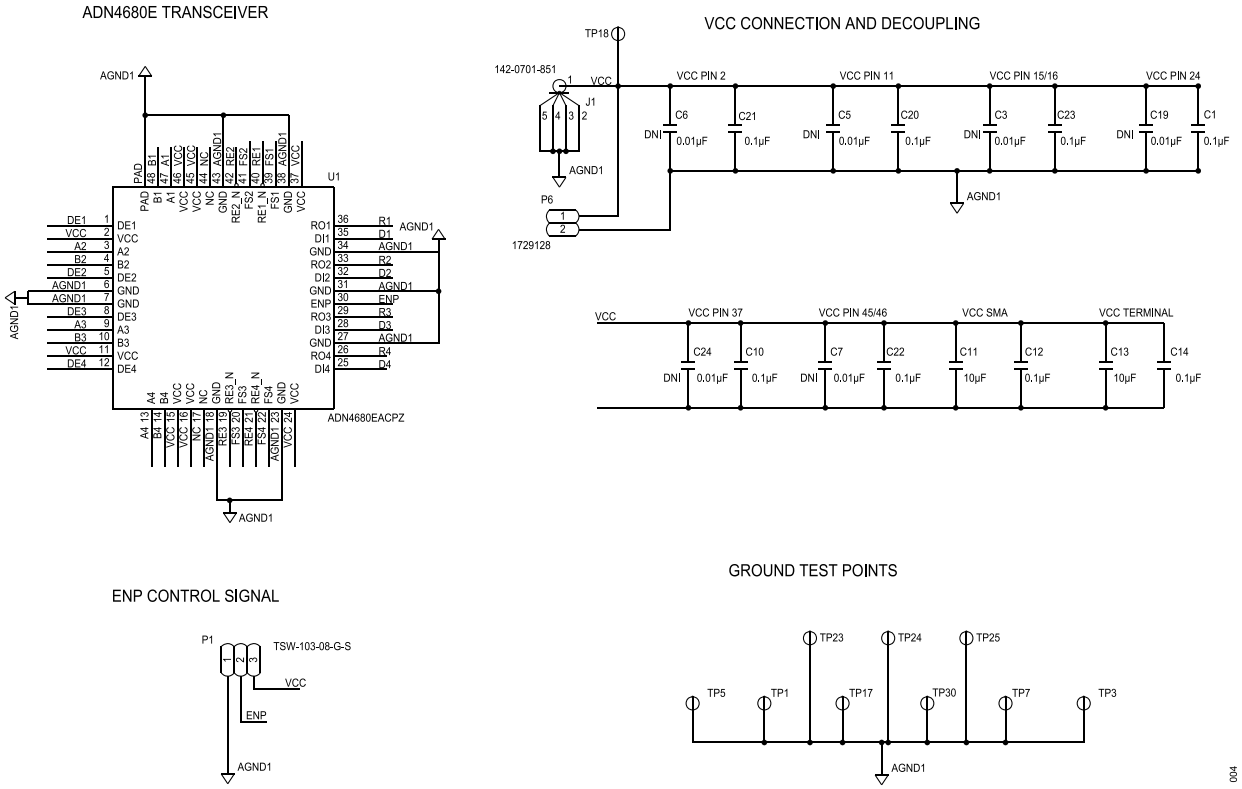

Figure 3. EVAL-ADN4680EEBZ Schematic (Page 1)

EVALUATION BOARD SCHEMATIC AND LAYOUT

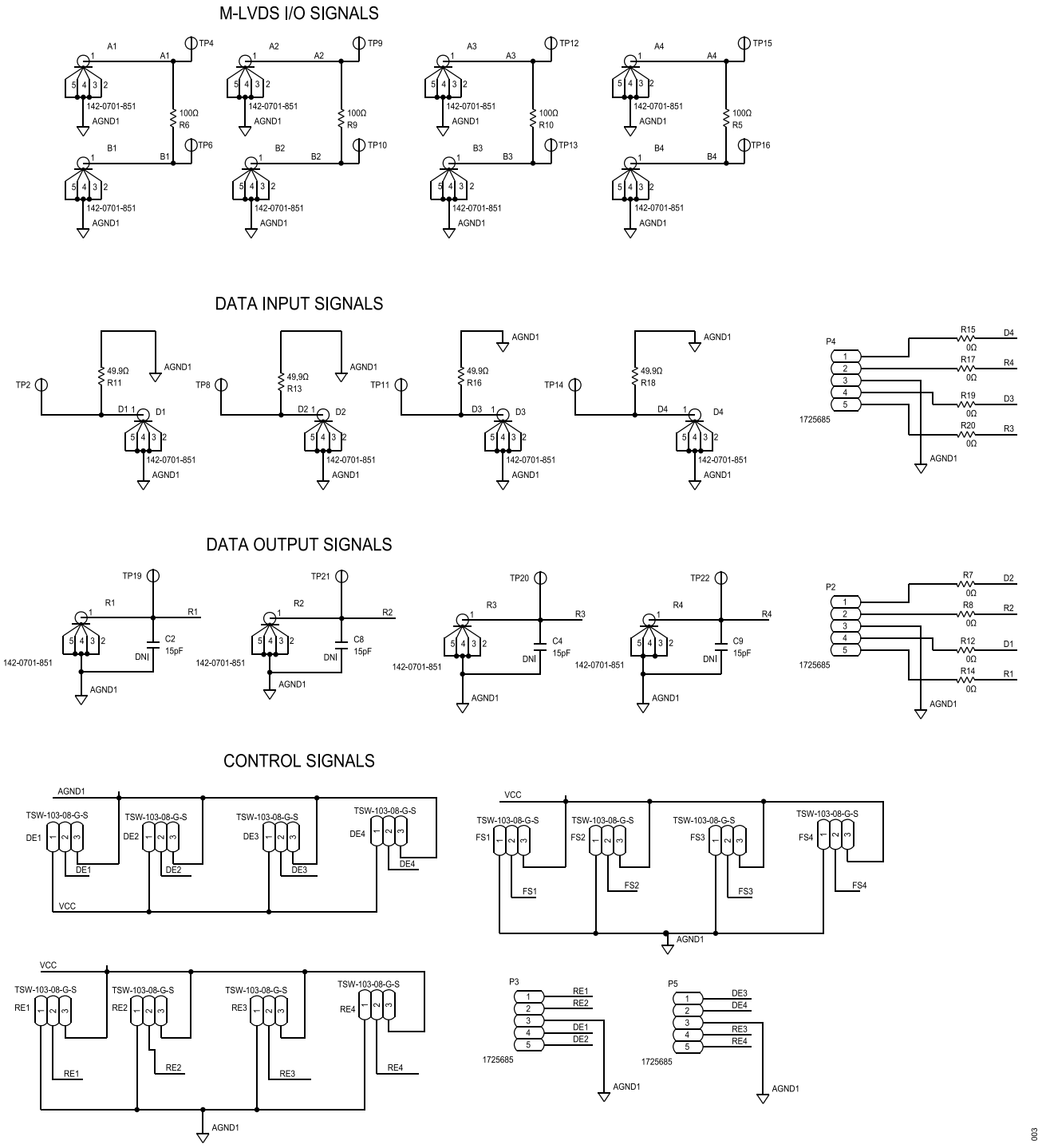

Figure 4. EVAL-ADN4680EEBZ Schematic (Page 2)

EVALUATION BOARD SCHEMATIC AND LAYOUT

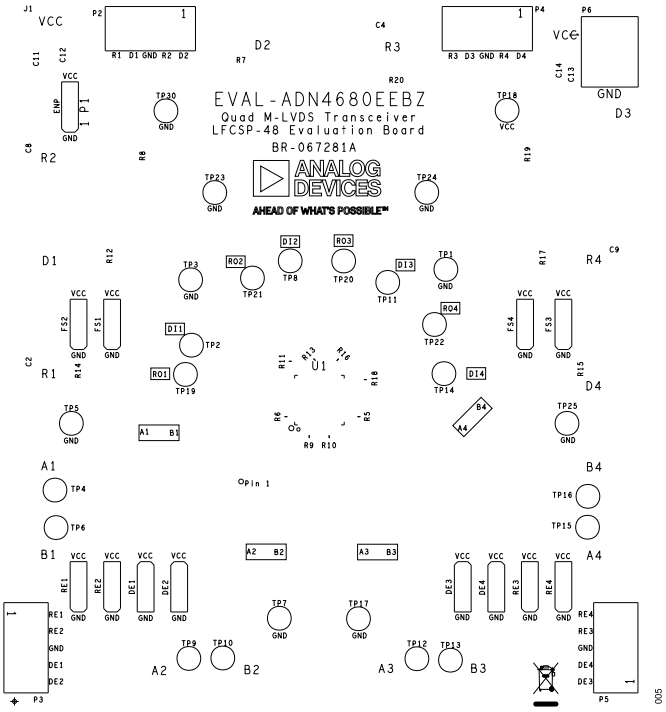

Figure 5. EVAL-ADN4680EEBZ Silkscreen

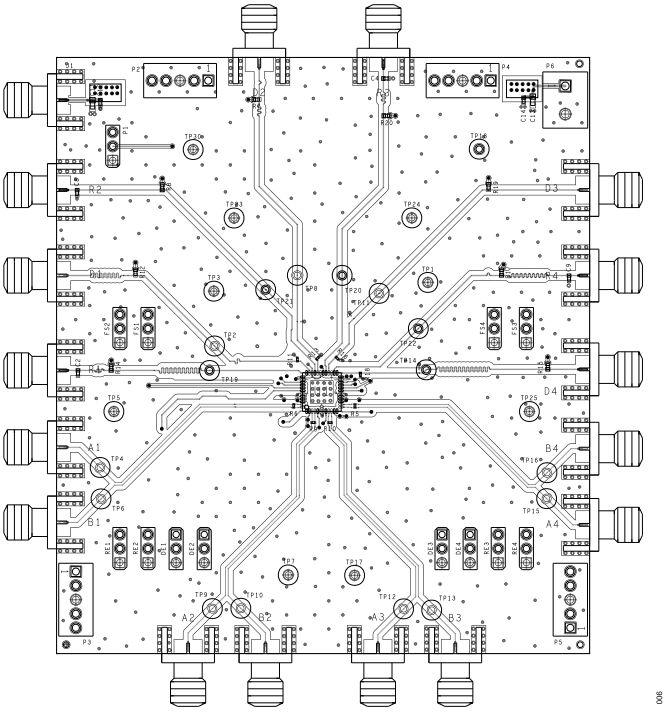

Figure 6. EVAL-ADN4680EEBZ Component Side

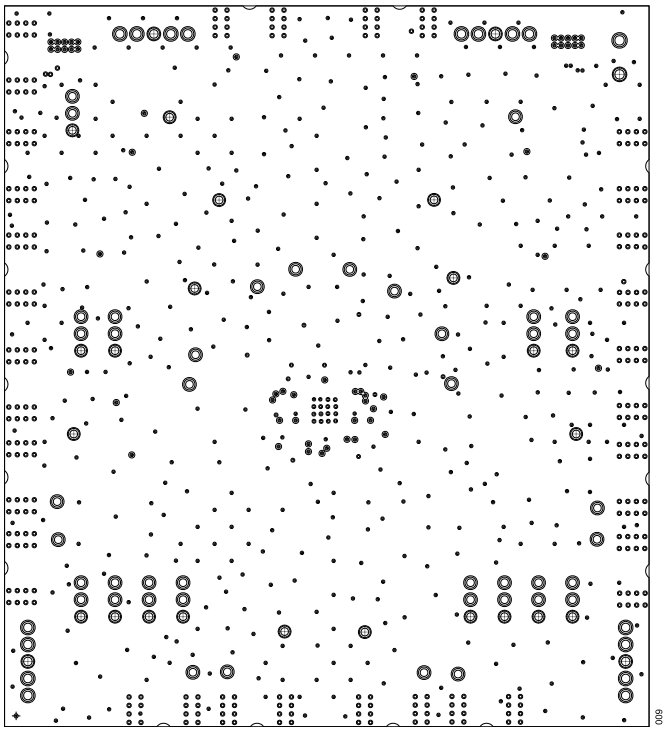

Figure 7. EVAL-ADN4680EEBZ Internal Layer 2 (GND)

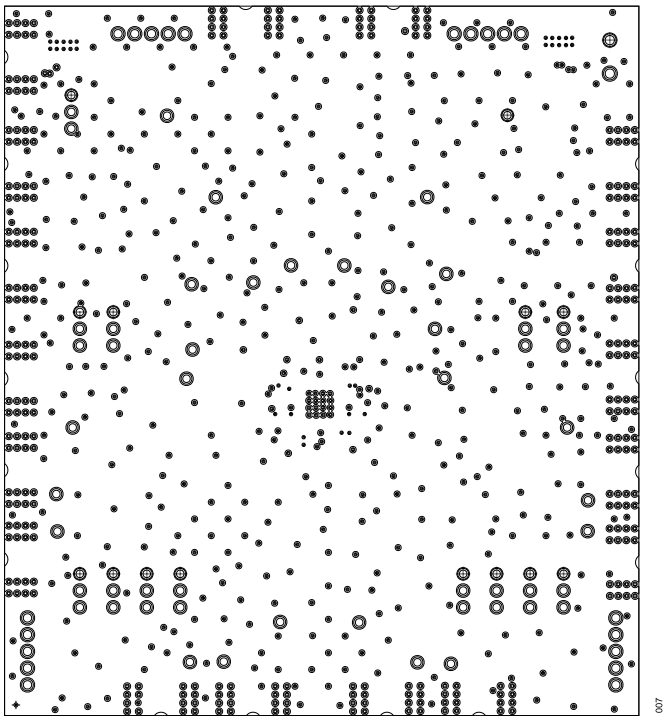

Figure 8. EVAL-ADN4680EEBZ Internal Layer 3 (VCC)

EVALUATION BOARD SCHEMATIC AND LAYOUT

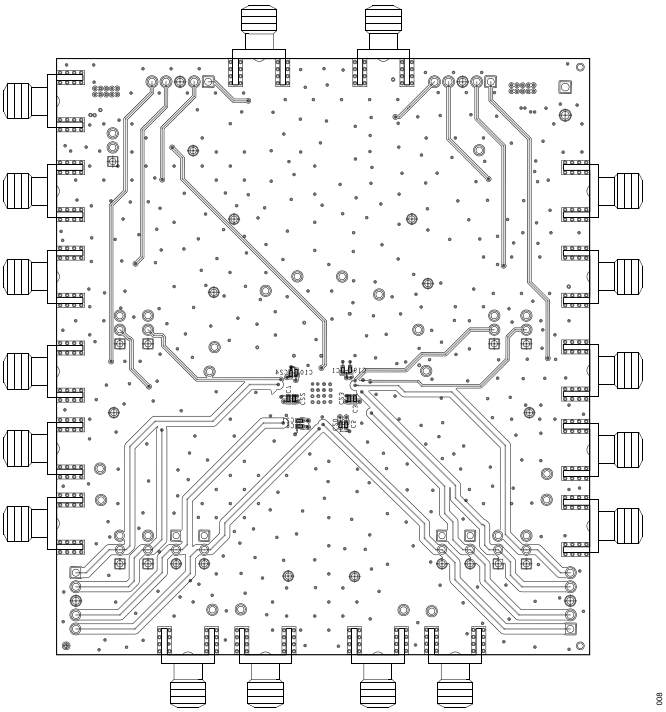

Figure 9. EVAL-ADN4680EEBZ Solder Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 5.

Quantity	Reference Designator	Description	Supplier and Part Number
17	A1 to A4, B1 to B4, D1 to D4, R1 to R4, J1	Coaxial side launch SMA connectors	Cinch Connectivity 142-0701-851
8	C1, C10, C12, C14, C20 to C23	Capacitors, 0.1 µF, 0402	AVX 0402ZD104KAT2A
2	C11, C13	Capacitors, 10 µF, 0603	TDK C1608X5R1A106M080AC
13	DE1 to DE4, FS1 to FS4, RE1 to RE4, P1	3-pin (3 × 1), 0.1 inch header and shorting blocks	Samtec TSW-103-08-G-S
4	P2 to P5	5-way terminal blocks	Phoenix Contact 1725685
1	P6	2-way terminal blocks	Phoenix Contact 1729128
4	R5, R6, R9, R10	Resistors, 100 Ω, 0201	Panasonic ERJ-1GNF1000C
4	R11, R13, R16, R18	Resistors, 49.9 Ω, 0201	Panasonic ERJ-1GNF49R9C
8	R7, R8, R12, R14, R15, R17, R19, R20	Resistors, 0 Ω, 0402	Yageo RC0402JR-070RL
26	TP1 to TP25, TP30	Test points	Mill-Max Mfg. 0319-1-15-15-18-27-04-0
1	U1	250 Mbps, half-duplex, quad M-LVDS transceivers, 48-lead LFCSP	Analog Devices, Inc., ADN4680EBCPZ
10	C2 to C9, C19, C24	Capacitors, do not install, 0402	Not applicable

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.