

CC256x QFN PCB Guidelines

ABSTRACT

This application report presents the printed circuit board (PCB) design guidelines, including placement and layout, for the CC2560, CC2564, and CC2564C QFN integrated circuits (ICs). Throughout this document CC256x is used in reference to the QFN ICs previously listed. Any variants are specifically called out.

Contents

1	Introduction	2
2	PCB Stack-Up	2
3	Placement Guidelines	3
4	Routing Guidelines	5
5	QFN Package Information	13
6	CC256x QFN EM Reference Design – PCB Layout and Assembly Drawings	14

List of Figures

1	PCB Stack-Up	2
2	Reference Design Schematics	3
3	Component Placement	3
4	LDO Capacitor Placement	4
5	DCO_LDO_OUT Instructions	5
6	<i>Bluetooth</i> [®] RF Path	6
7	BPF Specification Data	7
8	Inverted F Antenna on CC256x QFN Reference Design	7
9	Inverted F Antenna Dimensions	8
10	Crystal Trace Routing	9
11	Audio Interface Routing	10
12	Solid Ground Plane (Layer 2)	11
13	VSS_FREF Instruction	11
14	Thermal Pad Vias	12
15	QFN Package Dimensions	13
16	PCB Footprint	13
17	CC256x QFN EM Board – Top Side	14
18	CC256x QFN EM Board – Bottom Side Mirror	15
19	CC256x QFN EM Board – Layer 1	16
20	CC256x QFN EM Board – Layer 2	17
21	CC256x QFN EM Board – Layer 3	18
22	CC256x QFN EM Board – Layer 4	19

List of Tables

1	<i>Bluetooth</i> [®] BPF Requirements	6
2	Inverted F Antenna Dimensions	8

1 Introduction

The CC256x QFN IC is a *Bluetooth*® RF radio device targeted to operate on commercial platforms. The CC256x QFN reference design is based on the following requirements:

- A single-sided assembly
- A low manufacturing cost for PCBs

When designing a PCB for the CC256x QFN device, design rules and layout guidelines must be considered to achieve optimum performance.

This application report complements, and does not replace, the CC256x QFN product data sheet. TI advises the design engineer to use the data sheet and available application notes for the system design.

TI recommends that designers and users follow the design rules described in this application report to achieve performance similar to that obtained with the TI reference design. Following the given design rules minimizes the number of board spins required to achieve optimal performance.

If you have questions or cannot completely meet the guidelines described in this document, consult with your TI representative before releasing layout files to production.

1.1 Reference Documents

- [CC256x QFN Datasheet](#)
- [CC256xC QFN Datasheet](#)
- [CC256x QFN EM Reference Design](#)
- [CC256xC QFN EM Reference Design](#)
- [CC256x System Design Guide](#)
- [QFN/SON PCB Attachment Application Report](#)
- [Application Notes for Surface Mount Assembly of Amkor’s Dual Row MicroLeadFrame® \(MLF\) Packages](#)

2 PCB Stack-Up

The recommendations in this document refer to a four-layer, CC256x QFN PCB based on standard flame-retardant 4 (FR4) material, which is the technology commonly used for commercial applications (see [Figure 1](#)).

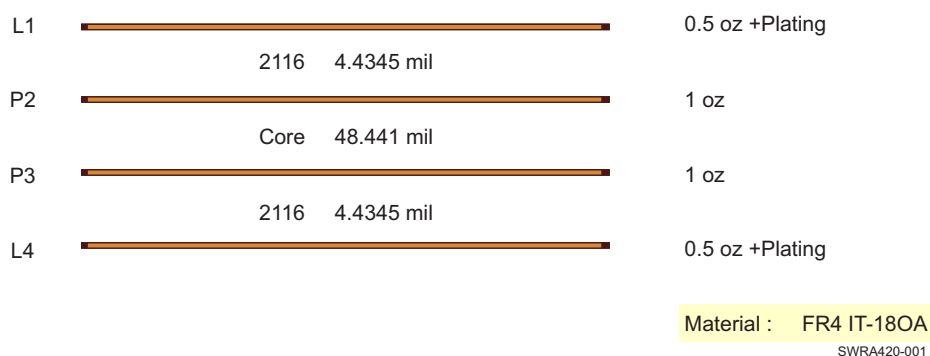


Figure 1. PCB Stack-Up

The layout recommendations for the CC256x QFN device described in this document are based on two routable layers and two solid ground layers (layer 2 and layer 4).

The pads of the QFN package are 0.6-mm pitch; therefore, when using standard routing rules to fan out, all required signals must be used. The design is based on a single-side assembly to reduce complexity and fabrication cost.

3.1 External Components

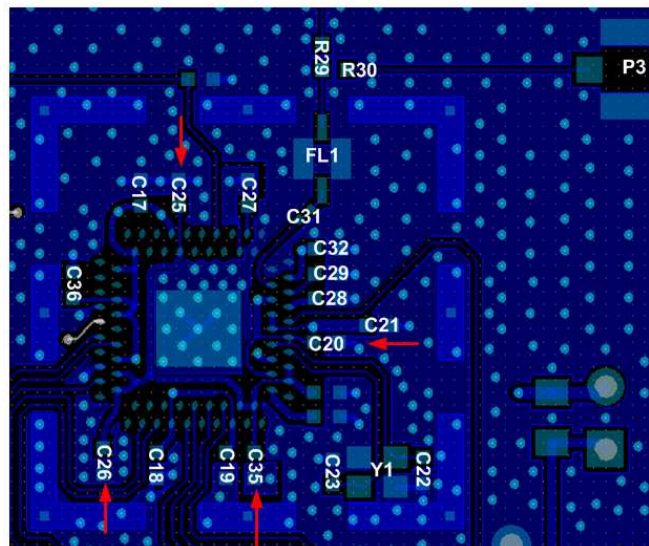
The passive components must be placed as close as possible to the CC256x QFN device. Traces must be as short as possible: The general trace width guideline is approximately 10 mils (.010 inch or 0.254 mm).

Pay special attention to the routing for these signals:

- Input/output (I/O) signals to the on-chip power-supply regulators
- Crystal I/O signals
- RF signals

3.2 Low-Dropout Capacitors

Follow these guidelines for the low-dropout (LDO) capacitors (see Figure 4):



Isolate ground for C35 on layer 1 as shown

SWRA420-004

Figure 4. LDO Capacitor Placement

- Ensure that the decoupling capacitors and traces to the capacitors that connect the LDO outputs are as short as possible.
- Ensure that the traces are wide.
- Keep the device and the capacitors together on the top side.
- Connect each capacitor ground connection directly to a solid ground layer (layer 2).
- Place the digital LDO decoupling capacitors (C25, C26, and C35) as close as possible to U5, the CC256x QFN IC relevant ball. For C35, create a small ground plane that is isolated from the ground of layer 1 and connect the capacitor ground pad to the solid ground (layer 2).
- Place the decoupling capacitor of MLDO_OUT (C20) as close as possible to U5.
- Using a via, directly connect each capacitor ground to the solid ground (layer 2). In addition, add many vias to increase the coupling to ground.

3.3 DCO_LDO_OUT

Follow these guidelines for DCO_LDO_OUT, the digital control oscillator signal (see [Figure 5](#)):

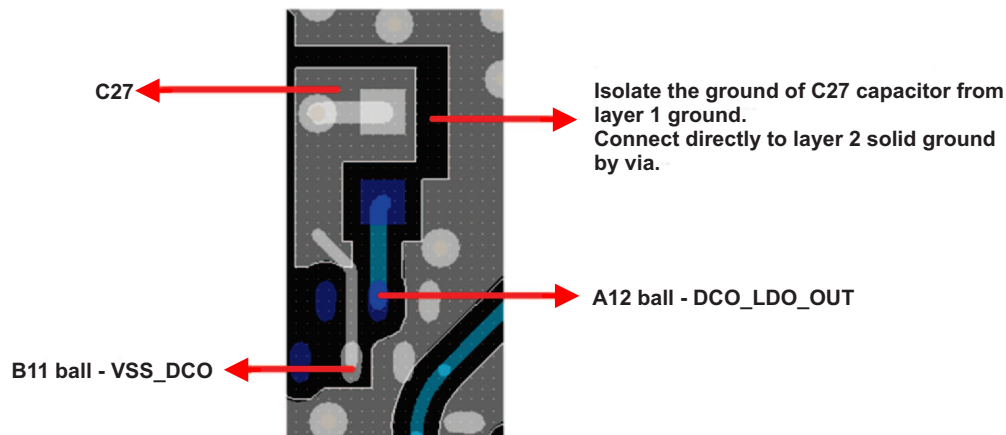


Figure 5. DCO_LDO_OUT Instructions

1. Connect capacitor (C27) directly to ball A12 (DCO_LDO_OUT).
2. Using a via, isolate the capacitor (C27) ground from the layer 1 ground and connect the capacitor (C27) ground directly to the layer 2 solid ground.

4 Routing Guidelines

4.1 RF Interface

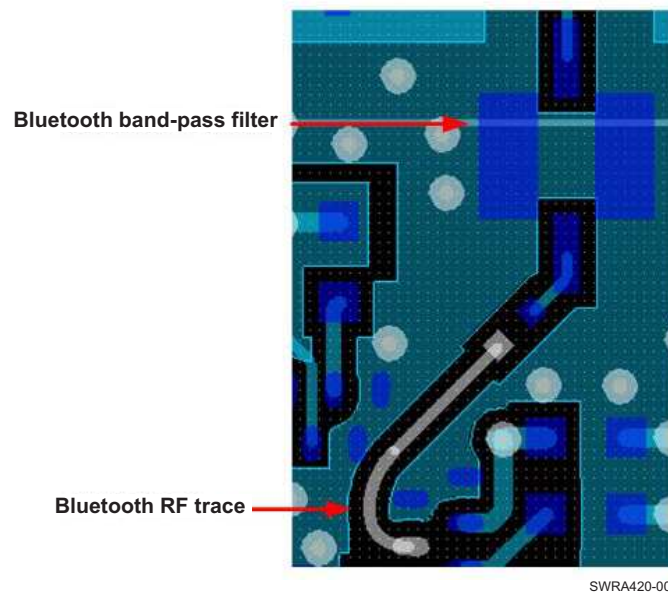
When designing the RF path, follow the placement and layout rules described in this section.

4.1.1 RF Trace

Route the *Bluetooth* RF path on the top layer (component side) and keep traces as short as possible. The *Bluetooth* RF trace must be a 50- Ω , impedance-controlled trace with reference to solid ground (layer 2). [Figure 6](#) shows the RF path. BT_RF (ball B8) is an inner ball. The RF line must be routed between the following NC pins, which are grounded for better RF isolation:

- NC_2 (A10)
- NC_3 (A11)
- NC_14 (B9)
- NC_15 (B10)

NOTE: These pins are NC at the chip level, but TI recommends grounding them on the PCB layout for better RF isolation.



SWRA420-006

Figure 6. Bluetooth® RF Path

4.1.2 Band Pass Filter

The area beneath the filter pads must be filled with ground on layer 1 and layer 2; however, the RF_IN and RF_OUT pads must be kept clear of any ground fill. The local ground beneath the filter area can be strengthened with vias to solid ground (layer 2).

Because the *Bluetooth* RF output has a DC level, a serial capacitor (C31) must be placed between the CC256x QFN RF port and the filter. Alternatively, a filter with a DC block can be used.

The BPF must meet the following minimum attenuation values to pass regulatory certification. [Table 1](#) lists the band-pass filter (BPF) rejection requirements over frequency for the CC256x QFN solution.

Table 1. Bluetooth® BPF Requirements

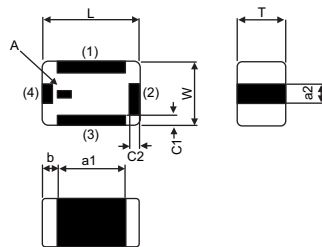
Harmonic	Center Frequency (MHz)	Minimum BPF Attenuation (dB)
Fundamental	2450	1.5
2	4900	26
3	7350	26
4	9800	19
5	12250	12
6	14700	9

Figure 7 shows the specification data for the BPF used in the reference design.

1. Characteristics (at 25°C)

Tentative part number	LFB212G45SG8C341TEMP
Nominal characteristics impedance	50 ohm
Nominal Center Frequency	2450.00 MHz
Pass Band Range (BW)	$f_0 \pm 50.00$ MHz
Insertion Loss in BW	1.42 dB typ. at 25 °C
Attenuation (absolute value)	31.9 dB typ. at 1200.00 ~1300.00 MHz 15.7 dB typ. at 2000.00 MHz 17.1 dB typ. at 3000.00 MHz 28.6 dB typ. at 3600.00 ~3800.00 MHz 34.8 dB typ. at 4800.00 ~ 5000.00 MHz 36.8 dB typ. 7200.00 ~ 7500.00 MHz
V.S.W.R. in BW	1.98 typ.
Power capacity	500 mW max.

2. Construction, Dimensions and marking

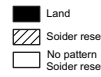
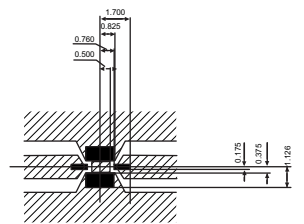


Mark	Meaning	
A	Directional Input Mark	

(in mm)			
Mark	Dimension	Mark	Dimension
L	2.00 ± 0.15	a2	$0.30 \pm 0.10 \sim 0.15$
W	1.25 ± 0.10	b	0.20 ± 0.16
T	0.95 ± 0.10	c1	$0.3 \pm 0.1 \sim 0.2$
a1	$1.60 \pm 0.10 \sim 0.16$	c2	$0.3 \pm 0.1 \sim 0.2$

TERMINAL COFIGURATION			
Terminal No.	Terminal Name	Terminal No.	Terminal Name
(1)	GND	(3)	GND
(2)	OUT	(4)	IN

3. Land pattern



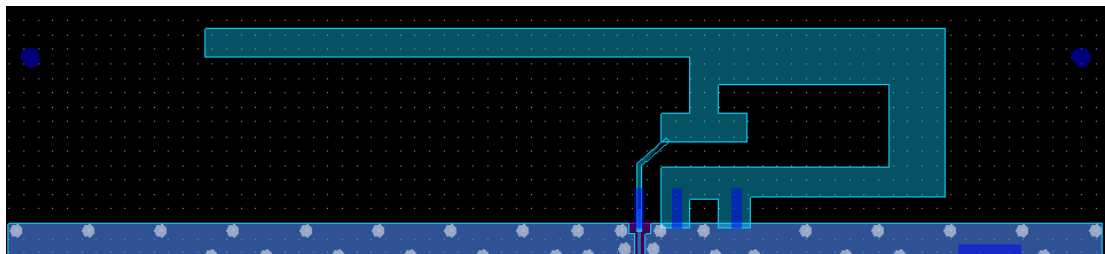
* Line width to be designed to match 50 ohm characteristic impedance. Depending on PCB material and thickness.

SWRA420-007

Figure 7. BPF Specification Data

4.1.3 Antenna

The antenna used in the reference design is a PCB-type inverted F antenna (see Figure 8). For more information on implementing the inverted F antenna design, see Design Note DN007 2.4 GHz Inverted F Antenna.



SWRA420-010

Figure 8. Inverted F Antenna on CC256x QFN Reference Design

4.1.3.1 Description of the Inverted F Antenna Design

The impedance of the inverted F antenna is matched directly to 50 Ω ; thus, external matching components are not required. However, TI recommends leaving the matching network placeholder preparation.

4.1.3.2 Implementation of the Inverted F Antenna

For optimum performance, create an exact copy of the antenna dimensions (see [Figure 9](#) and [Table 2](#)). To implement the antenna in a PCB CAD tool, the easiest approach is to import the antenna layout from a Gerber file or a .DXF file. If the antenna is implemented on a PCB that is wider than the antenna, avoid placing components or having a ground plane close to the end points of the antenna.

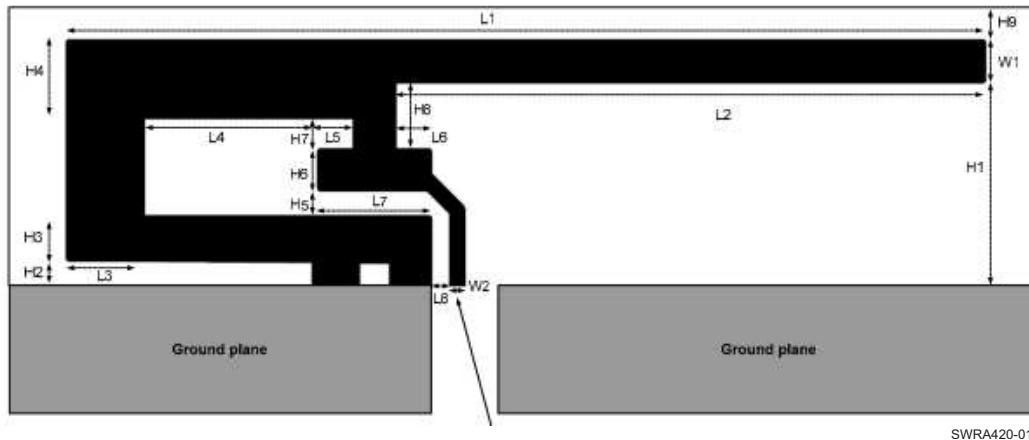


Figure 9. Inverted F Antenna Dimensions

Table 2. Inverted F Antenna Dimensions

Dimension	Measurement (mm)	Dimension	Measurement (mm)
H1	5.70 mm	W2	0.46 mm
H2	0.74 mm	L1	25.58 mm
H3	1.29 mm	L2	16.40 mm
H4	2.21 mm	L3	2.18 mm
H5	0.66 mm	L4	4.80 mm
H6	1.21 mm	L5	1.00 mm
H7	0.80 mm	L6	1.00 mm
H8	1.80 mm	L7	3.20 mm
H9	0.61 mm	L8	0.45 mm
W1	1.21 mm	—	—

4.1.4 RF Shielding Recommendations

The CC256x QFN reference design accepts RF shield with side dimensions of 0.65 inch x 0.65 inch. Although not required, the RF shield is recommended because the shield protects the CC256x *Bluetooth* from RF interference and the fast-clock crystal oscillator (26 MHz) from VHF and UHF interference. This protection optimizes the fast-clock phase noise as well as RF spurious content. The RF shield chosen for the CC256x QFN reference design is from Laird Technologies, BMI-S-202-F/BMI-S-202-C.

4.2 Clocks

Clock signal routing directly influences RF performance due to the signal trace susceptibility to noise. Therefore, the clock signal lines must be as short as possible. Clock signal traces must have a ground plane on each side of the signal trace to reduce undesired signal coupling. To reduce capacitive coupling of undesired signals into the clock line, do not route clock traces above or below other signals (especially digital signals).

4.2.1 Fast Clock – Crystal

If a crystal oscillator is used, the parasitic characteristics of the clock trace influence the oscillation. Traces must be kept as short as possible. Traces that are too wide can cause excessive capacitance and traces that are too narrow can cause parasitic inductance of the clock trace. For short clock traces, use a trace width of approximately 10 mils (0.010 inch or 0.254 mm). Keep the crystal tune capacitors (C22 and C23) close to the crystal pads.

TI recommends that you avoid crossing the crystal lines on the adjacent layers. Nevertheless, TI recommends keeping the ground plane under the crystal line to improve the return path. [Figure 10](#) shows the crystal trace routing.

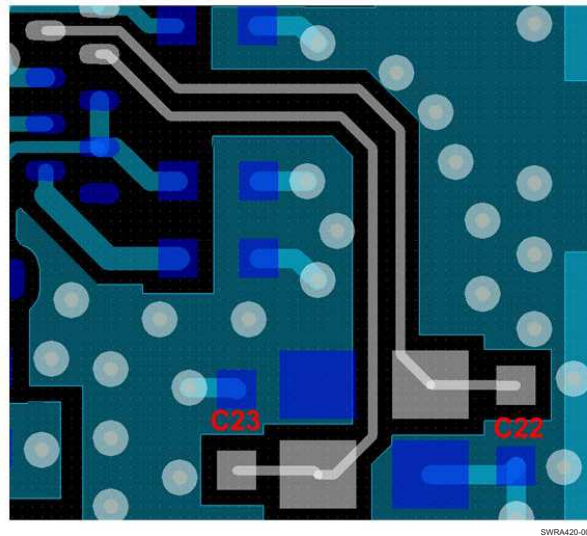


Figure 10. Crystal Trace Routing

4.2.2 Slow Clock

The slow clock signal lines must be as short as possible. Traces of slow clock signals should have a ground plane on each side of the signal trace to reduce undesired signal coupling. To reduce capacitive coupling of undesired signals into the clock line, slow clock traces must not be routed above or below other signals (especially digital signals).

4.2.3 Digital Clock Signals

The audio clock (AUD_CLK, ball B32) signal is a digital clock signal and can be source of interference for adjacent signals. Avoid laying this type of signal trace next to sensitive signals (for example, the RF path, DCO_LDO, and other LDO capacitors). Keep the traces of these signals as short as possible and maintain a maximum clearance value from other traces. Run the lines with ground on the adjacent layer to improve the return path and isolation. TI recommends running these lines as a bus interface.

4.3 Interfaces

4.3.1 Audio Lines Routing Guidelines

The digital audio lines (pulse-code modulation [PCM]) are high-speed digital lines in which the four wires (AUD_CLK, AUD_FSYNC, AUD_IN, and AUD_OUT) must be roughly the same length. These lines are high-speed digital and must be separated from DC supply lines, RF lines, and sensitive fast-clock lines and circuitry. Run the lines with ground on the adjacent layer to improve the return path and isolation. Figure 11 shows the routing for the audio interface.

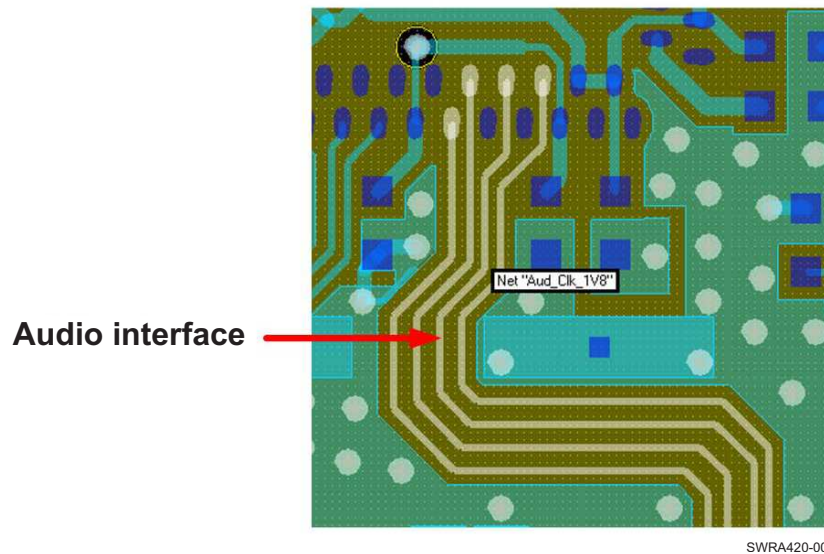


Figure 11. Audio Interface Routing

4.3.2 Universal Asynchronous Receiver-Transmitter (UART) Signal Lines

The CC256x device has a 4-wire UART connection (H4) with hardware flow control (HCI_TX, HCI_RX, HCI_RTS, and HCI_CTS). The default baud rate is 115.2 kbps with support for up to 4 Mbps.

4.4 Power Supply

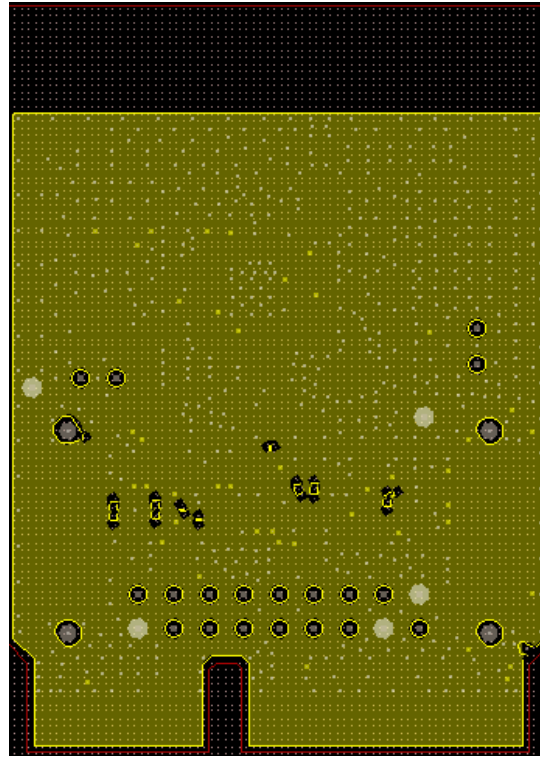
Adhere to the following requirements to supply power to the CC256x QFN device:

- Star pattern format to supply power to the different pads of the device
- Typical width of about 10 mils (.010 inch or 0.254 mm) for wide traces
- Short power supply trace length
- Decoupling capacitor placed as close as possible to the device

The most common ground return issues occur when ground returning currents have a longer return path due to placement of the DC bypass capacitor to ground.

4.5 Ground

The common ground is the solid ground plane of layer 2 (see [Figure 12](#)).

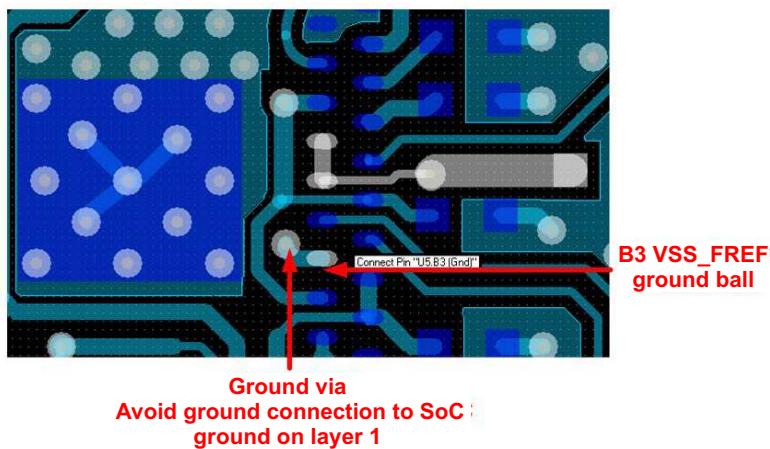


SWRA420-012

Figure 12. Solid Ground Plane (Layer 2)

4.5.1 Key VSS Ball

To optimize isolation from digital noise, avoid connecting ball B3 (VSS_FREF) to the system-on-a-chip (SoC) thermal ground. Instead connect B3 to solid ground (layer 2) directly using a via (see [Figure 13](#)).

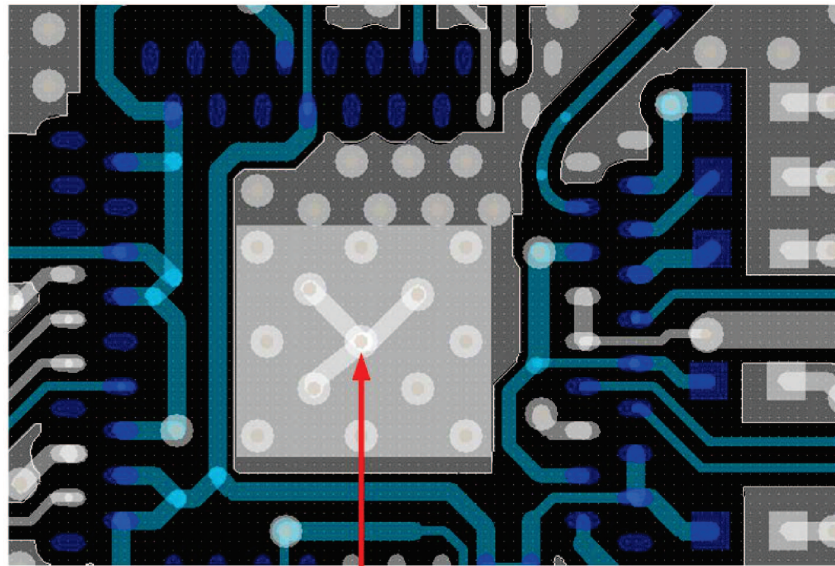


SWRA420-013

Figure 13. VSS_FREF Instruction

4.5.2 Thermal Pad Vias

To increase ground coupling, add at least 13 vias to the thermal pads of the SoC directly to the solid ground (see [Figure 14](#)).



Add at least 13 vias to ground underneath the SoC to increase the ground "coupling".

SWRA420-014

Figure 14. Thermal Pad Vias

5 QFN Package Information

Figure 15 and Figure 16 show the QFN package dimensions and PCB footprint. For more information regarding the QFN mechanical data, see the [CC256x QFN Datasheet](#).

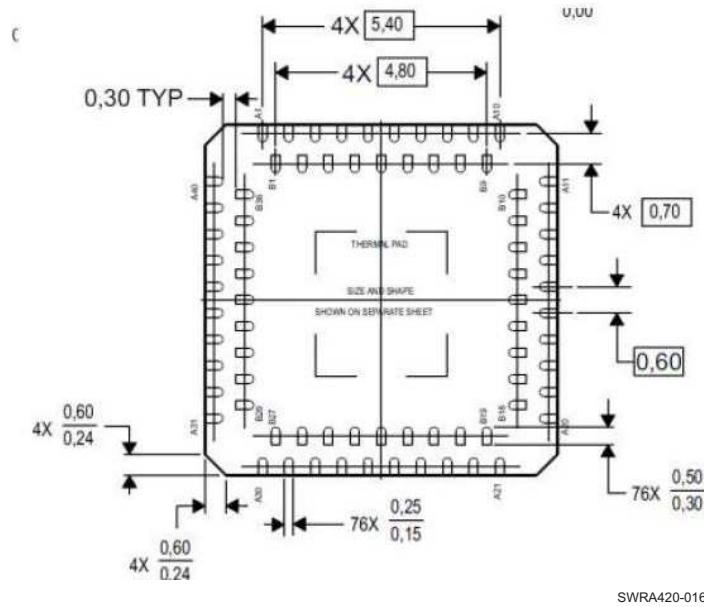


Figure 15. QFN Package Dimensions

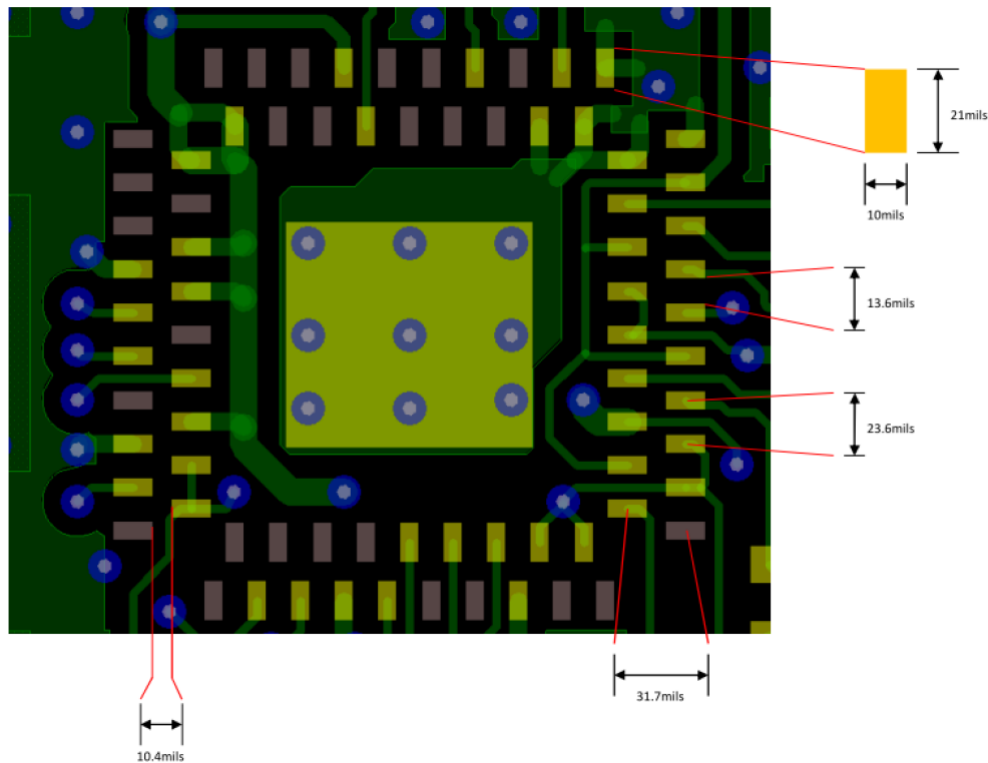


Figure 16. PCB Footprint

6 CC256x QFN EM Reference Design – PCB Layout and Assembly Drawings

Figure 17 through Figure 22 show the PCB layers and assembly drawings for the CC256x QFN EM reference design board. The CC256xC QFN EM reference design is identical to the CC26x QFN EM reference design, with the exception of silk screen changes.

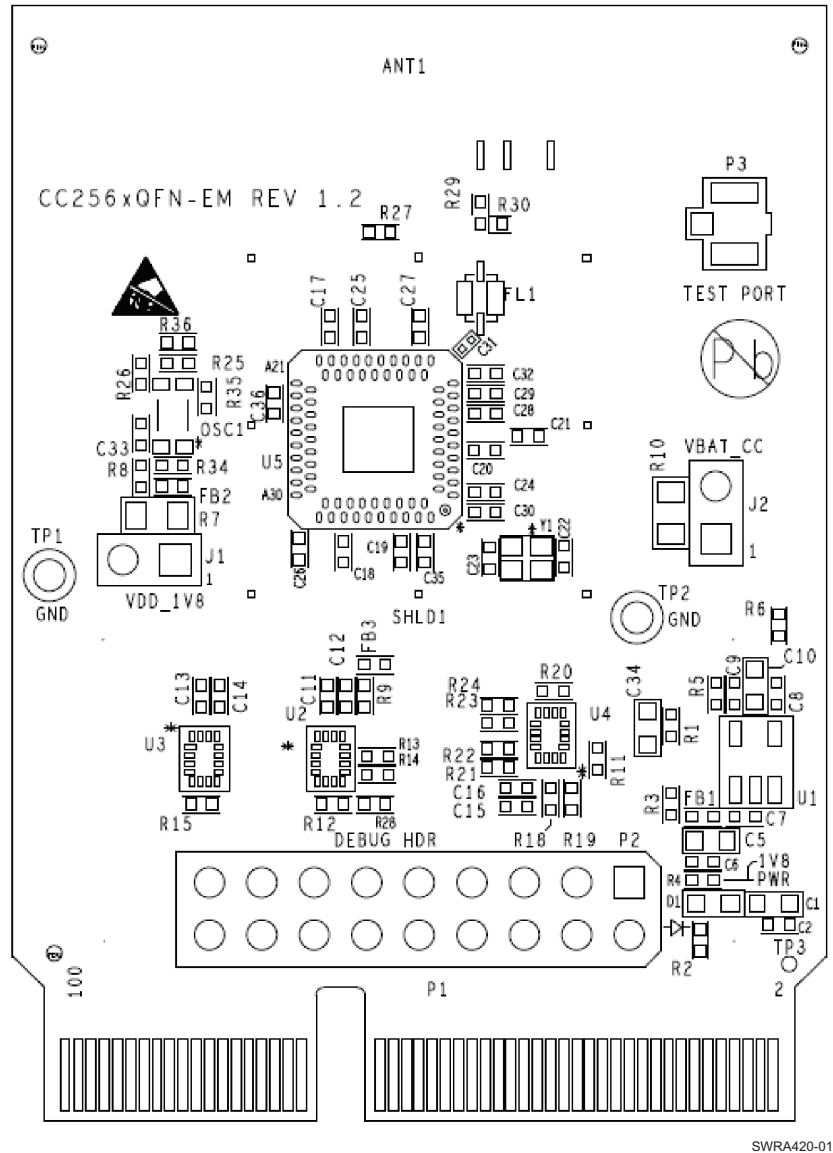
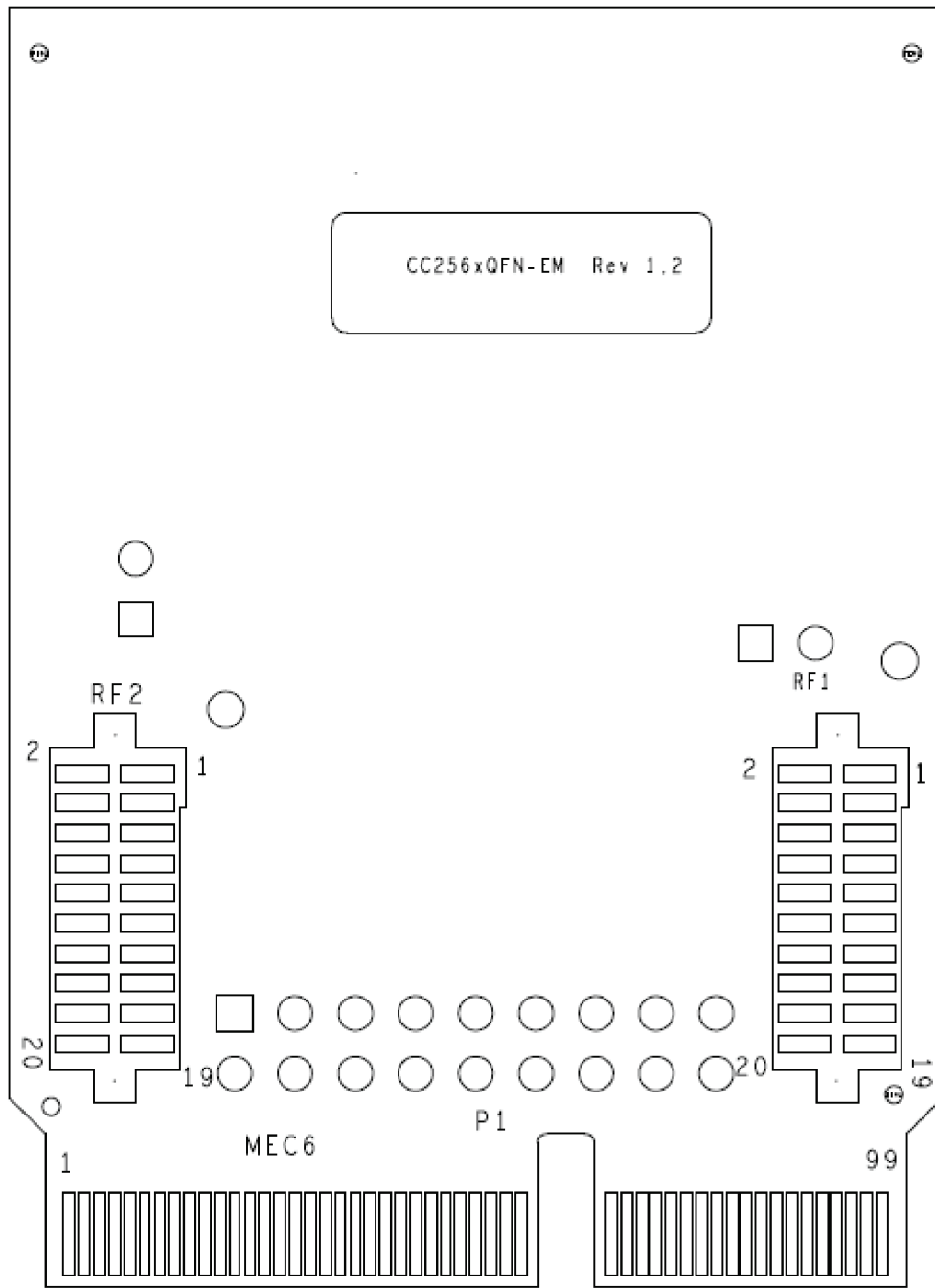
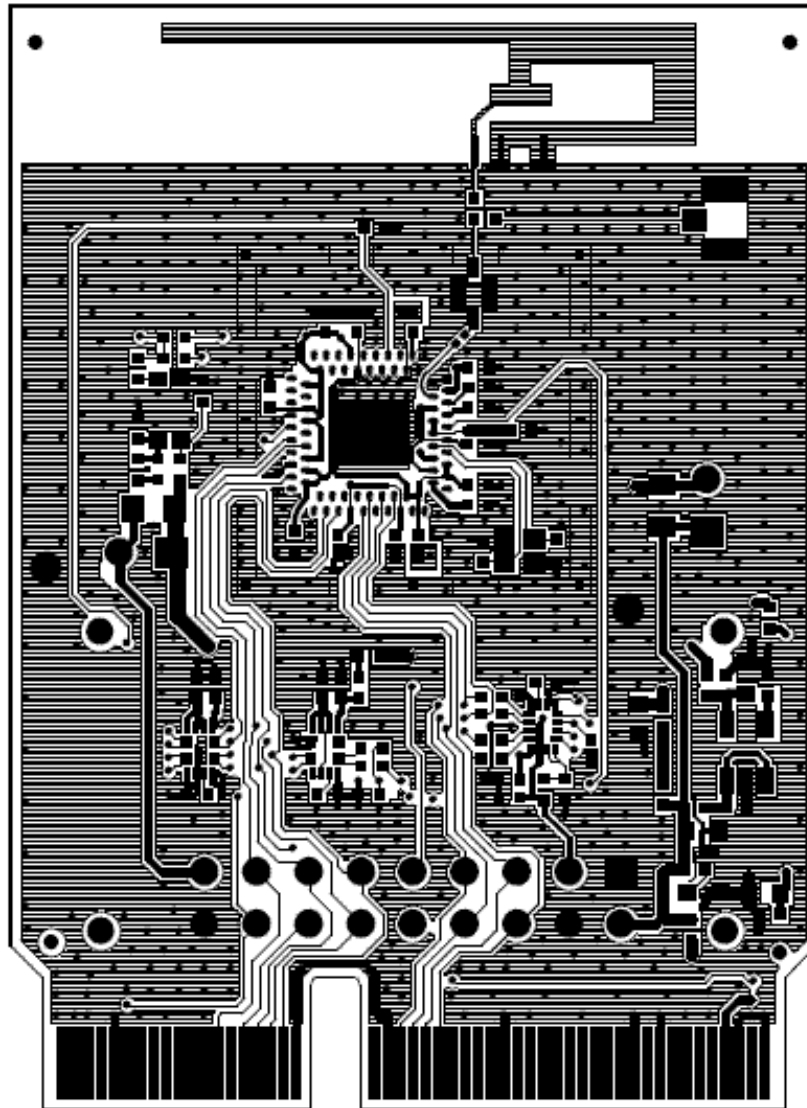


Figure 17. CC256x QFN EM Board – Top Side



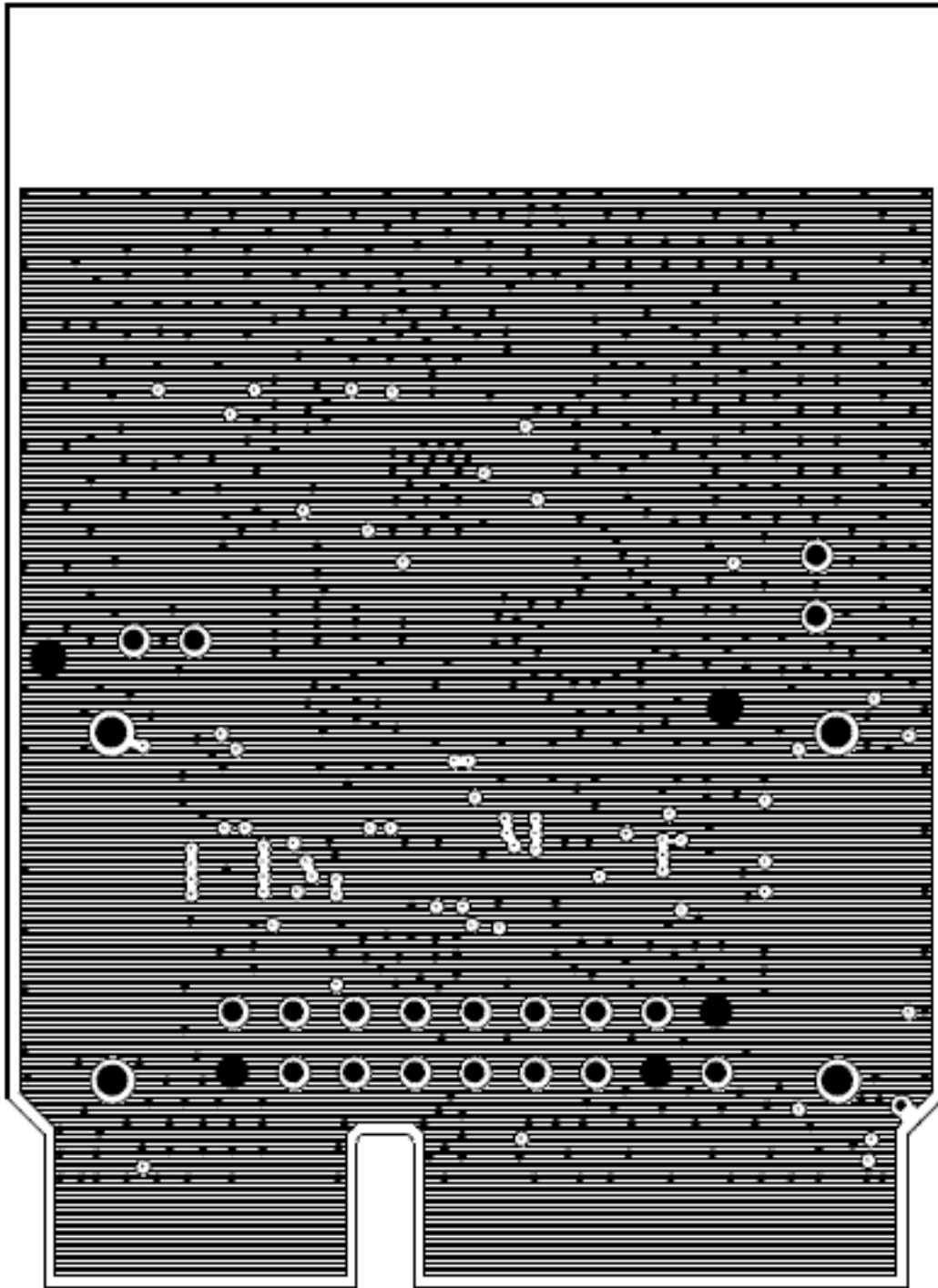
SWRA420-019

Figure 18. CC256x QFN EM Board – Bottom Side Mirror



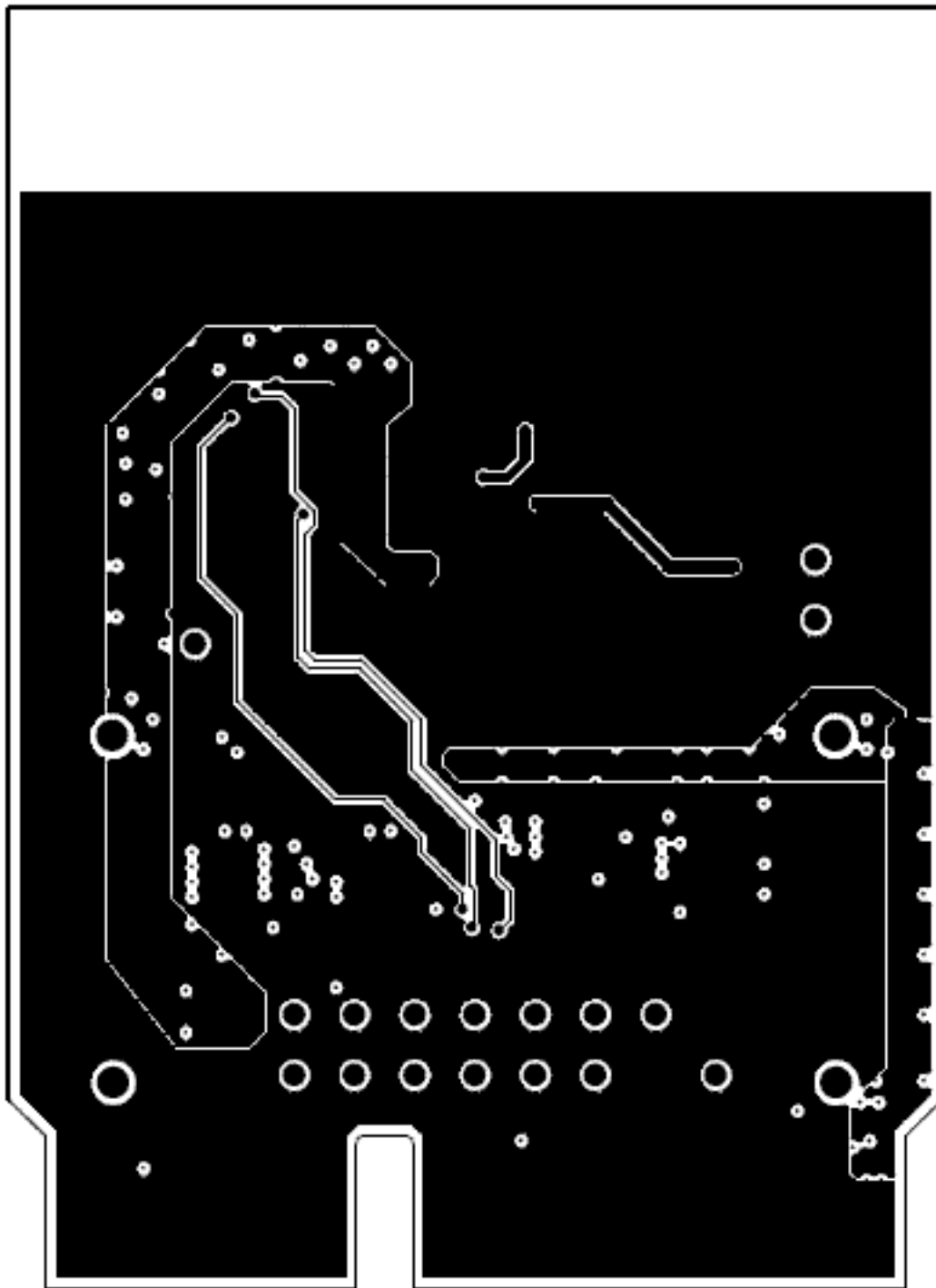
SWRA420-020

Figure 19. CC256x QFN EM Board – Layer 1



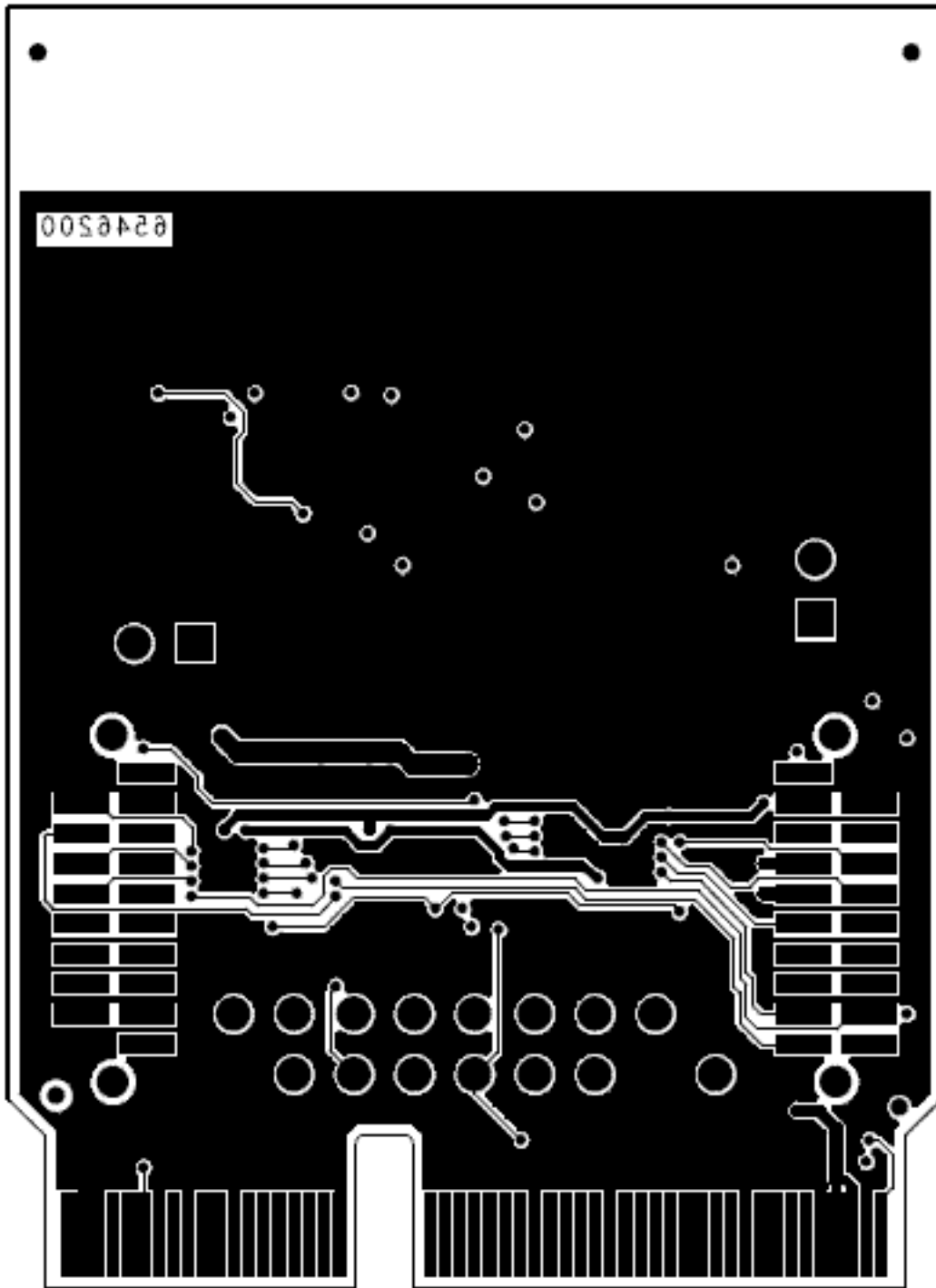
SWRA420-021

Figure 20. CC256x QFN EM Board – Layer 2



SWRA420-022

Figure 21. CC256x QFN EM Board – Layer 3



SWRA420-023

Figure 22. CC256x QFN EM Board – Layer 4

Revision History

Changes from Original (February 2013) to A Revision	Page
--	-------------

- | | | |
|---|--|---|
| • | Changed reference schematics in Section 3, Placement Guidelines | 3 |
| • | Added NC pins between which to ground the RF line in Section 4.1.1, RF Trace | 5 |
-

Changes from A Revision (March 2015) to B Revision	Page
---	-------------

- | | | |
|---|--|----|
| • | Added specific IC names to abstract..... | 1 |
| • | Added CC256xC QFN Datasheet reference to Section 1.1 | 2 |
| • | Added CC256xC QFN EM Reference Design reference to Section 1.1 | 2 |
| • | Added additional information regarding the reference design to Section 6 | 14 |
-

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com