

# 74LVT241

3.3 V octal buffer/line driver; 3-state

Rev. 5 — 8 July 2024

Product data sheet

## 1. General description

The 74LVT241 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

This device is an octal buffer that is ideal for driving bus lines. The device features two output enables ( $\overline{1OE}$ ,  $2OE$ ), each controlling four of the 3-state outputs.

## 2. Features and benefits

- 3-state buffers
- Octal bus interface
- Input and output interface capability to systems at 5 V supply
- TTL input and output switching levels
- Output capability: +64 mA/-32 mA
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- Bus-hold data inputs eliminate the need for external pull-up resistors for unused inputs
- Live insertion/extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74LVT241D</a>	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	<a href="#">SOT163-1</a>
<a href="#">74LVT241PW</a>	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	<a href="#">SOT360-1</a>
<a href="#">74LVT241BQ</a>	-40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	<a href="#">SOT764-1</a>

### 4. Functional diagram

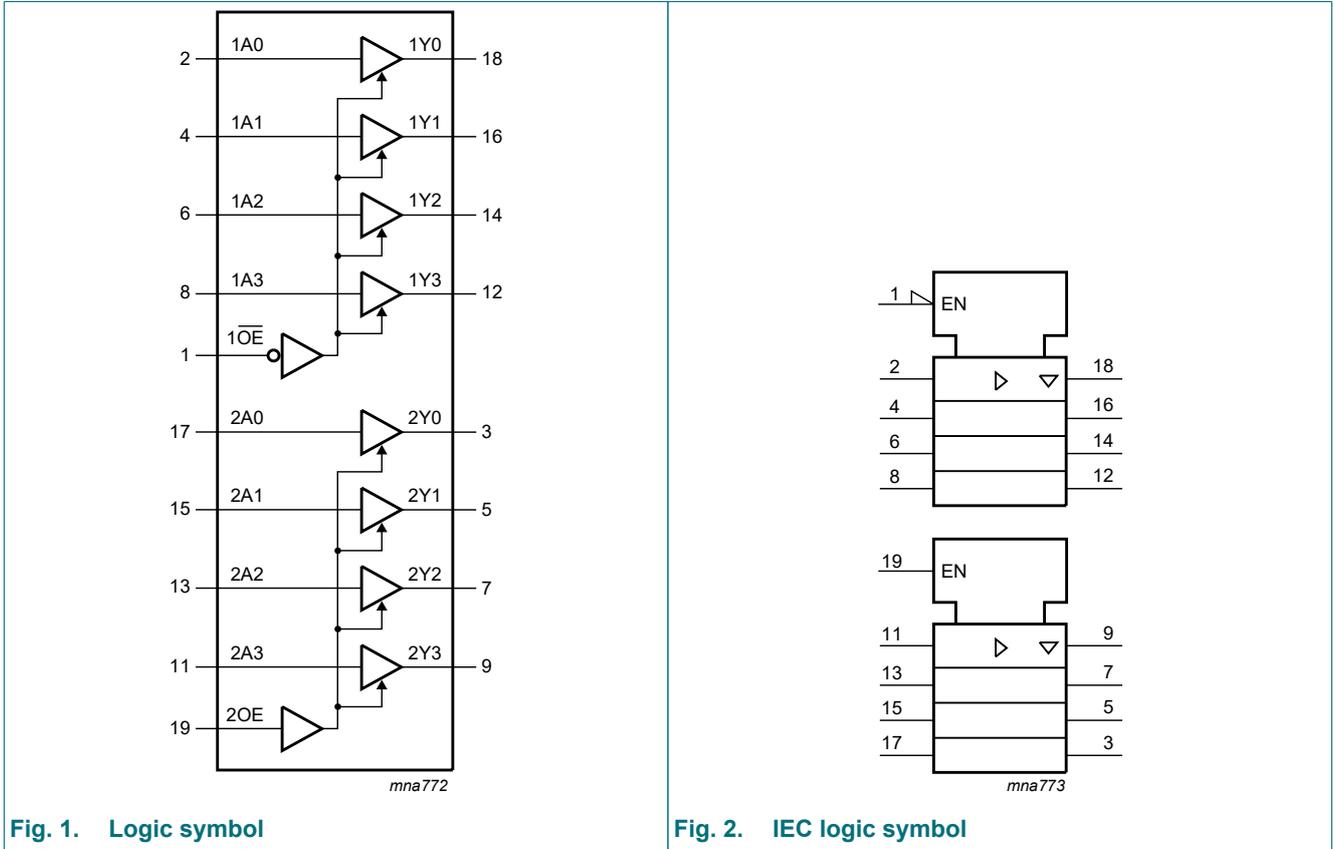
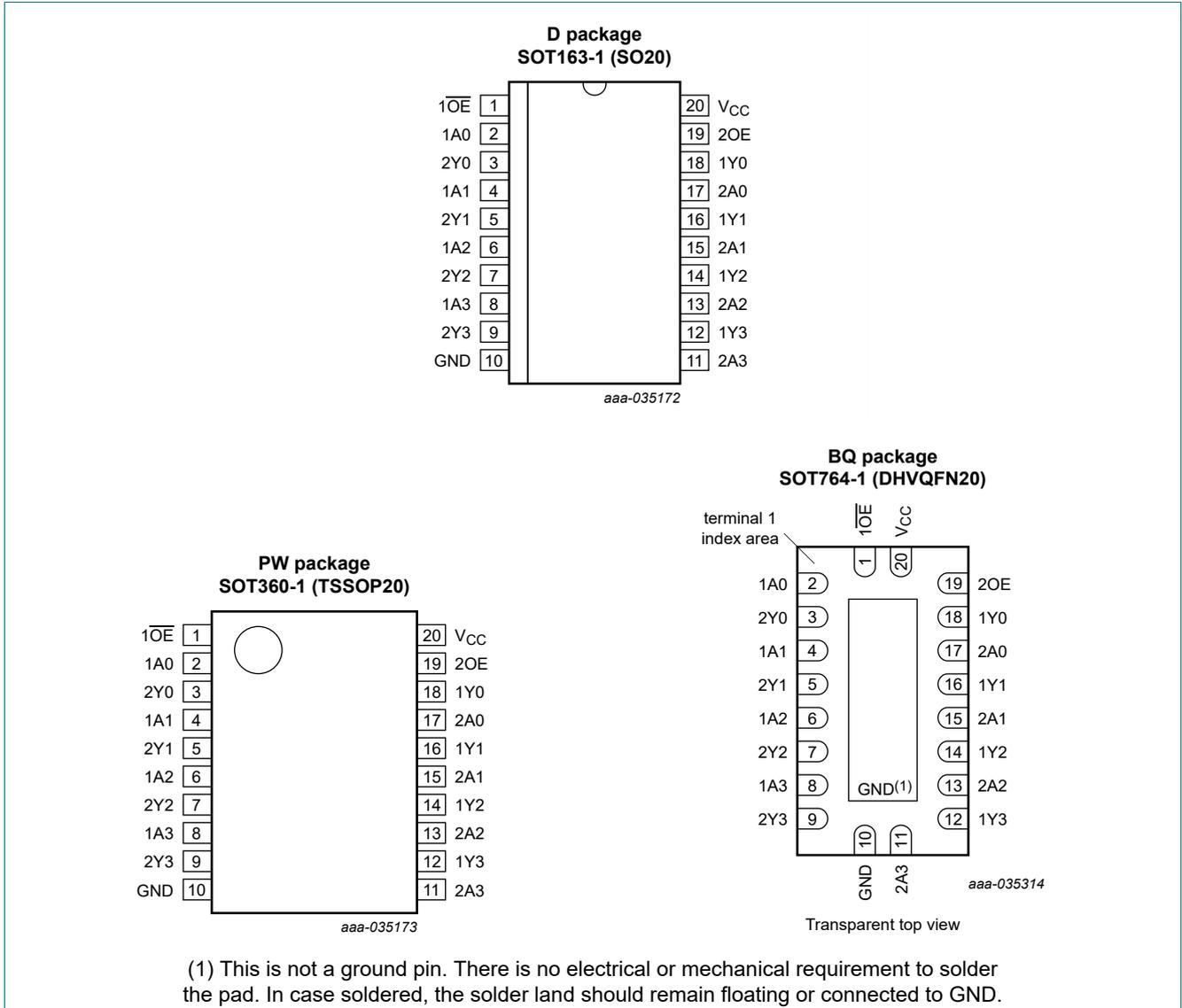


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

## 5. Pinning information

### 5.1. Pinning



## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE	1	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2A0, 2A1, 2A2, 2A3	17, 15, 13, 11	data input
GND	10	ground (0 V)
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
2Y0, 2Y1, 2Y2, 2Y3	3, 5, 7, 9	data output
2OE	19	output enable input (active HIGH)
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = Don't care; Z = High impedance "OFF" state.

Inputs				Outputs	
1OE	2OE	1An	2An	1Yn	2Yn
L	H	L	L	L	L
L	H	H	H	H	H
H	L	X	X	Z	Z

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
V <sub>I</sub>	input voltage		[1] -0.5	+7.0	V
V <sub>O</sub>	output voltage	output in OFF or HIGH state	[1] -0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
I <sub>O</sub>	output current	output in LOW state	-	128	mA
		output in HIGH state	-64	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j</sub>	junction temperature		[2] -	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		2.7	3.6	V
$V_I$	input voltage		0	5.5	V
$I_{OH}$	HIGH-level output current		-32	-	mA
$I_{OL}$	LOW-level output current		-	32	mA
		current duty cycle $\leq 50\%$ ; $f_i \geq 1$ kHz	-	64	mA
$T_{amb}$	ambient temperature	in free air	-40	+85	$^{\circ}\text{C}$
$\Delta t/\Delta V$	input transition rise and fall rate	output enabled	0	10	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V);  $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{IK}$	input clamping voltage	$V_{CC} = 2.7$ V; $I_{IK} = -18$ mA	-1.2	-0.9	-	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_{CC} = 2.7$ V to 3.6 V; $I_{OH} = -100$ $\mu\text{A}$	$V_{CC} - 0.2$	$V_{CC} - 0.1$	-	V
		$V_{CC} = 2.7$ V; $I_{OH} = -8$ mA	2.4	2.5	-	V
		$V_{CC} = 3.0$ V; $I_{OH} = -32$ mA	2.0	2.2	-	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 2.7$ V; $I_{OL} = 100$ $\mu\text{A}$		0.1	0.2	V
		$V_{CC} = 2.7$ V; $I_{OL} = 24$ mA	-	0.3	0.5	V
		$V_{CC} = 3.0$ V; $I_{OL} = 16$ mA	-	0.25	0.4	V
		$V_{CC} = 3.0$ V; $I_{OL} = 32$ mA	-	0.3	0.5	V
		$V_{CC} = 3.0$ V; $I_{OL} = 64$ mA	-	0.4	0.55	V
$I_I$	input leakage current	control and data pins				
		$V_{CC} = 0$ V or 3.6 V; $V_I = 5.5$ V	-	1	10	$\mu\text{A}$
		control pins				
		$V_{CC} = 3.6$ V; $V_I = V_{CC}$ or GND	-	0.1	$\pm 1$	$\mu\text{A}$
		data pins [2]				
		$V_{CC} = 3.6$ V; $V_I = V_{CC}$	-	0.1	1	$\mu\text{A}$
		$V_{CC} = 3.6$ V; $V_I = 0$ V	-5	-1	-	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_{CC} = 0$ V; $V_I$ or $V_O = 0$ V to 4.5 V	-	1	$\pm 100$	$\mu\text{A}$
$I_{BHL}$	bus hold LOW current	$V_{CC} = 3.0$ V; $V_I = 0.8$ V	75	150	-	$\mu\text{A}$
$I_{BHH}$	bus hold HIGH current	$V_{CC} = 3.0$ V; $V_I = 2.0$ V	-	-150	-75	$\mu\text{A}$
$I_{BHLO}$	bus hold LOW overdrive current	$V_{CC} = 3.6$ V; $V_I = 0$ V to 3.6 V [3]	500	-	-	$\mu\text{A}$
$I_{BHHO}$	bus hold HIGH overdrive current	$V_{CC} = 3.6$ V; $V_I = 0$ V to 3.6 V [3]	-	-	-500	$\mu\text{A}$
$I_{LO}$	output leakage current	$V_O = 5.5$ V; $V_{CC} = 3.0$ V; output HIGH	-	60	125	$\mu\text{A}$
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2$ V; $V_O = 0.5$ V to $V_{CC}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; 1OE, 2OE = don't care [4]	-	$\pm 1$	$\pm 100$	$\mu\text{A}$

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I <sub>oz</sub>	OFF-state output current	V <sub>CC</sub> = 3.6 V; V <sub>O</sub> = 3.0 V	-	1	5	μA
		V <sub>CC</sub> = 3.6 V; V <sub>O</sub> = 0.5 V	-5	-1	-	μA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A				
		outputs HIGH	-	0.12	0.19	mA
		outputs LOW	-	3	12	mA
		outputs disabled [5]	-	0.12	0.19	mA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 3.0 V to 3.6 V; one input = V <sub>CC</sub> - 0.6 V, other inputs at V <sub>CC</sub> or GND [6]	-	0.1	0.25	mA
C <sub>I</sub>	input capacitance	1 $\overline{\text{OE}}$ and 2OE inputs; outputs disabled; V <sub>I</sub> = 0 V or 3.0 V	-	4	-	pF
C <sub>I/O</sub>	input/output capacitance	at input/output data pins, outputs disabled; V <sub>I/O</sub> = 0 V or 3.0 V	-	8	-	pF

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

[2] Unused pins at V<sub>CC</sub> or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V<sub>CC</sub> between 0 V and 1.2 V with a transition time of up to 10 ms.

From V<sub>CC</sub> = 1.2 V to V<sub>CC</sub> = 3.3 V ± 0.3 V a transition time of 100 ms is permitted. This parameter is valid for T<sub>amb</sub> = +25 °C only.

[5] I<sub>CC</sub> with the outputs disabled is measured with outputs pulled to V<sub>CC</sub> or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND.

## 10. Dynamic characteristics

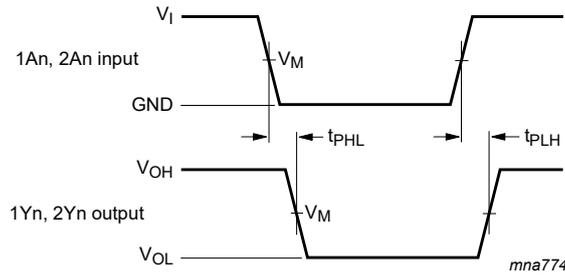
**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 6;  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ .

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t <sub>PLH</sub>	LOW to HIGH propagation delay	1An to 1Yn, 2An to 2Yn; see Fig. 3				
		V <sub>CC</sub> = 2.7 V	-	-	4.0	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V	1.0	2.8	3.8	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	1An to 1Yn, 2An to 2Yn; see Fig. 3				
		V <sub>CC</sub> = 2.7 V	-	-	4.0	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V	1.0	2.8	3.8	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	1 $\overline{O}E$ to 1Yn; see Fig. 4				
		V <sub>CC</sub> = 2.7 V	-	-	5.0	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V	1.0	3.2	4.4	ns
		2OE to 2Yn; see Fig. 5				
		V <sub>CC</sub> = 2.7 V	-	-	5.6	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V	1.0	3.8	5.1	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	1 $\overline{O}E$ to 1Yn; see Fig. 4				
		V <sub>CC</sub> = 2.7 V	-	-	4.9	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V	1.0	3.1	4.3	ns
		2OE to 2Yn; see Fig. 5				
		V <sub>CC</sub> = 2.7 V	-	-	5.4	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	1 $\overline{O}E$ to 1Yn; see Fig. 4				
		V <sub>CC</sub> = 2.7 V	-	-	5.4	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V	2.0	3.6	5.2	ns
		2OE to 2Yn; see Fig. 5				
		V <sub>CC</sub> = 2.7 V	-	-	5.0	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	1 $\overline{O}E$ to 1Yn; see Fig. 4				
		V <sub>CC</sub> = 2.7 V	-	-	4.3	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V	1.6	2.9	4.2	ns
		2OE to 2Yn; see Fig. 5				
		V <sub>CC</sub> = 2.7 V	-	-	4.3	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V	1.0	2.8	4.0	ns

[1] Typical values are measured at  $T_{amb} = 25\text{ °C}$  and  $V_{CC} = 3.3\text{ V}$ .

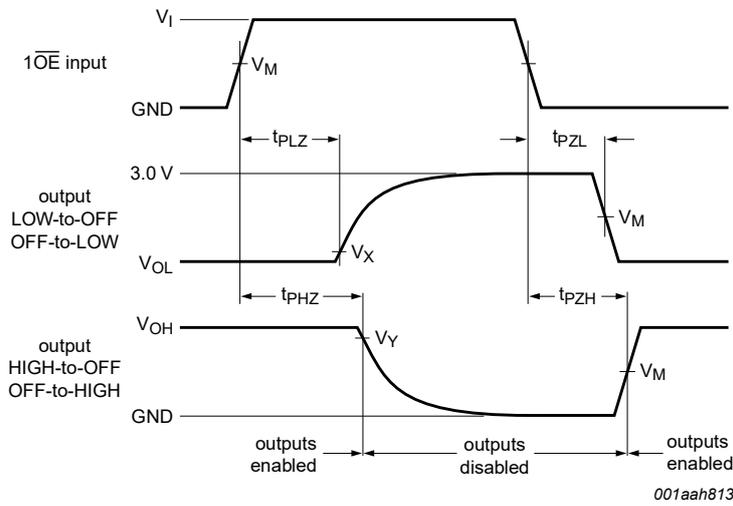
10.1. Waveforms and test circuit



See [Table 8](#) for measurement points.

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

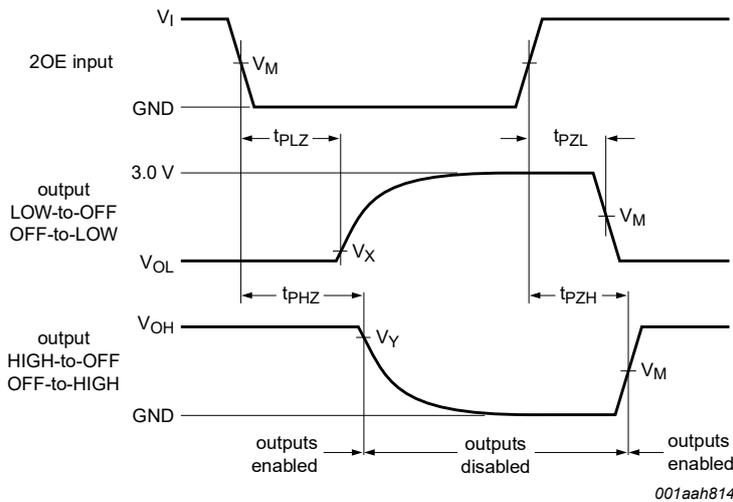
**Fig. 3. Input (1An, 2An) to output (1Yn, 2Yn) propagation delays and output transition times**



See [Table 8](#) for measurement points.

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 4. 3-state output enable and disable times**



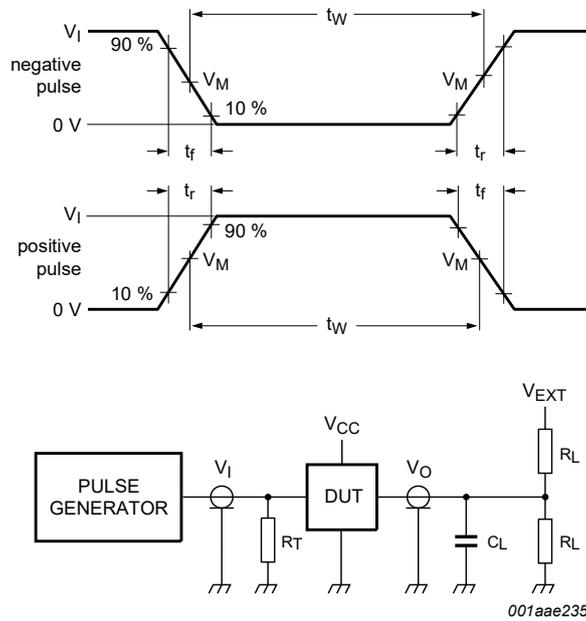
See [Table 8](#) for measurement points.

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 5. 3-state output enable and disable times**

Table 8. Measurement points

V <sub>CC</sub>	Input	Output		
	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>	V <sub>M</sub>
2.7 V to 3.6 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V	1.5 V



Test data is given in [Table 9](#).

Definitions test circuit:

R<sub>L</sub> = Load resistance;

C<sub>L</sub> = Load capacitance including jig and probe capacitance;

R<sub>T</sub> = Termination resistance should be equal to output impedance Z<sub>o</sub> of the pulse generator;

V<sub>EXT</sub> = External voltage for measuring switching times.

Fig. 6. Test circuit for switching times

Table 9. Test data

Input				Load		V <sub>EXT</sub>		
V <sub>I</sub>	f <sub>i</sub>	t <sub>w</sub>	t <sub>r</sub> , t <sub>f</sub>	R <sub>L</sub>	C <sub>L</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500 Ω	50 pF	GND	6 V	open

### 11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

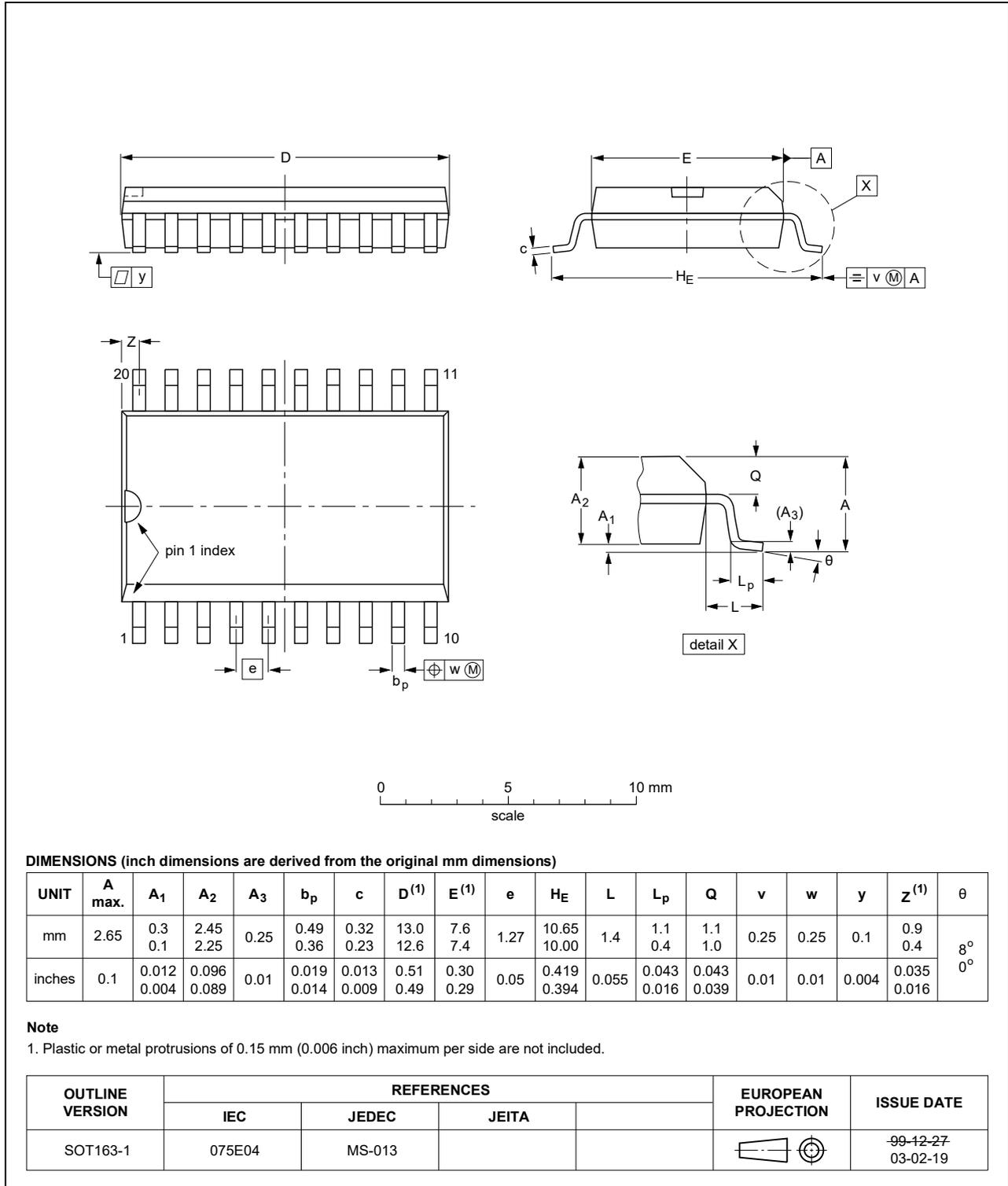


Fig. 7. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

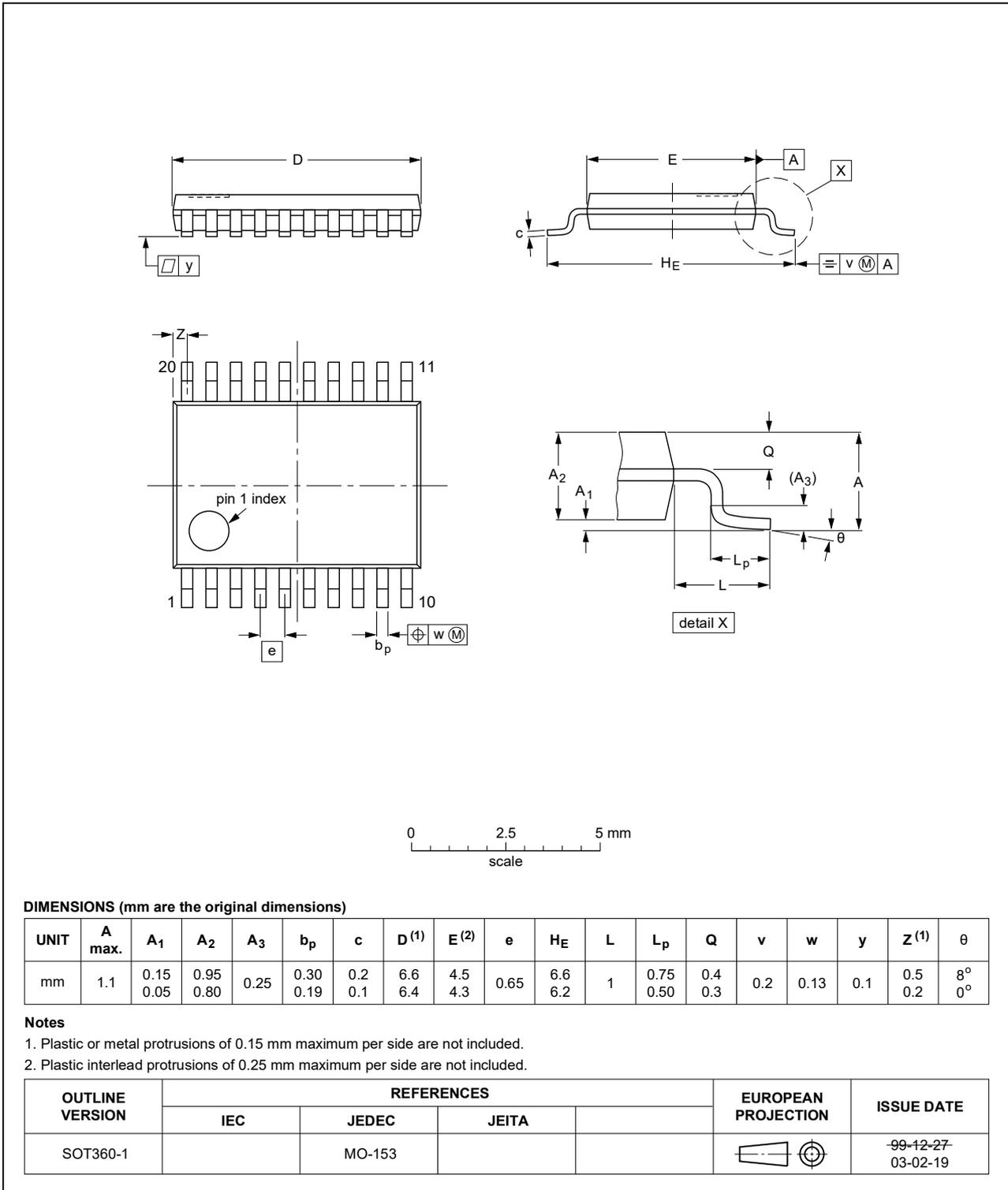


Fig. 8. Package outline SOT360-1 (TSSOP20)



## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT241 v.5	20240708	Product data sheet		74LVT241 v.4
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> <li>• <a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation removed.</li> </ul>			
74LVT241 v.4	20190327	Product data sheet		74LVT241 v.3
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Fig. 9</a>: package outline drawing SOT764-1 (DHVQFN20) updated.</li> <li>• Type number 74LVT241DB (SOT339-1) removed.</li> </ul>			
74LVT241 v.3	20080507	Product data sheet	ECN07_046	74LVT241 v.2
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• DHVQFN20 package added <a href="#">Section 3</a> and <a href="#">Section 11</a>.</li> </ul>			
74LVT241 v.2	19980219	Product specification	-	74LVT241 v.1
74LVT241 v.1	19960529	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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## Contents

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<b>1. General description</b> .....	<b>1</b>
<b>2. Features and benefits</b> .....	<b>1</b>
<b>3. Ordering information</b> .....	<b>1</b>
<b>4. Functional diagram</b> .....	<b>2</b>
<b>5. Pinning information</b> .....	<b>3</b>
5.1. Pinning.....	3
5.2. Pin description.....	4
<b>6. Functional description</b> .....	<b>4</b>
<b>7. Limiting values</b> .....	<b>4</b>
<b>8. Recommended operating conditions</b> .....	<b>5</b>
<b>9. Static characteristics</b> .....	<b>5</b>
<b>10. Dynamic characteristics</b> .....	<b>7</b>
10.1. Waveforms and test circuit.....	8
<b>11. Package outline</b> .....	<b>10</b>
<b>12. Abbreviations</b> .....	<b>13</b>
<b>13. Revision history</b> .....	<b>13</b>
<b>14. Legal information</b> .....	<b>14</b>

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