Introduction

This technical note is intended to provide information about Kionix's 2 x 2 mm LGA packages and guidelines for developing PCB land pattern layouts. These guidelines are general in nature and based on recommended industry practices. The user must apply their actual experiences and development efforts to optimize designs and processes for their manufacturing techniques and the needs of varying end-use applications. It should be noted that with the proper PCB footprint and solder stencil designs, the package will self-align during the solder reflow process.

Package Marking

- Marking font type : Arial
- Font size : 1.5 Point (0.56 mm height)
- Line space : 0.1 mm
- Text information
  - 1st line – AAZ Assembly Build Lot code
  - 2nd line – ZZ Device name

Note - All text lines shall be right justified.

Figure 1: 2 x 2 mm LGA package marking information

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Package Outline and Dimensions

Kionix's 2 x 2 mm LGA 12-pin packages come in number of thicknesses (e.g. 0.9 mm and 0.6 mm nominal thicknesses). The following diagram shows the package outline of one of the Kionix's sensors with dimensions and tolerances. **For *actual* package outline drawing of a specific part, see the corresponding product specification document.**

All dimensions and tolerances conform to ASME Y14.5M-1994.

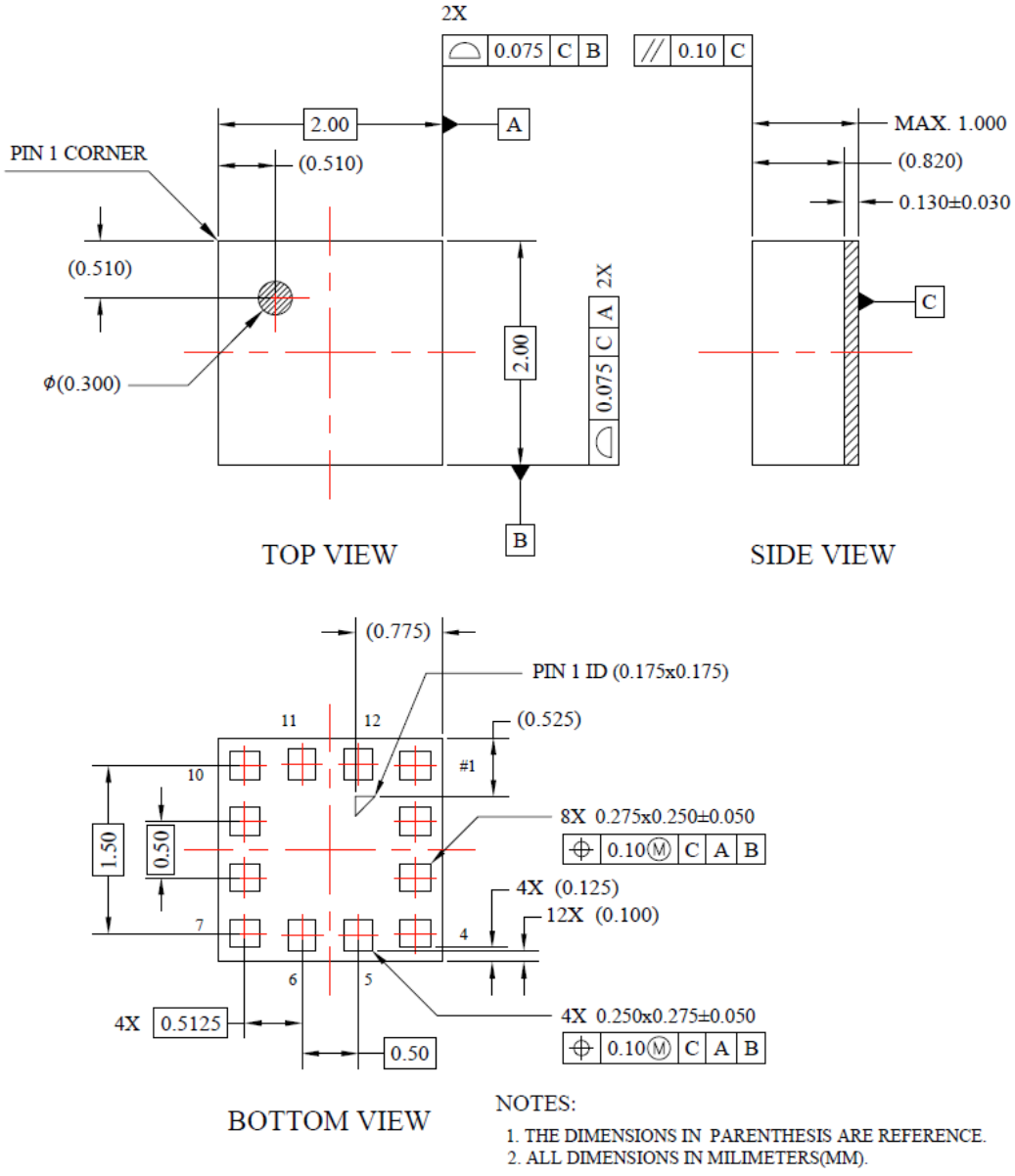
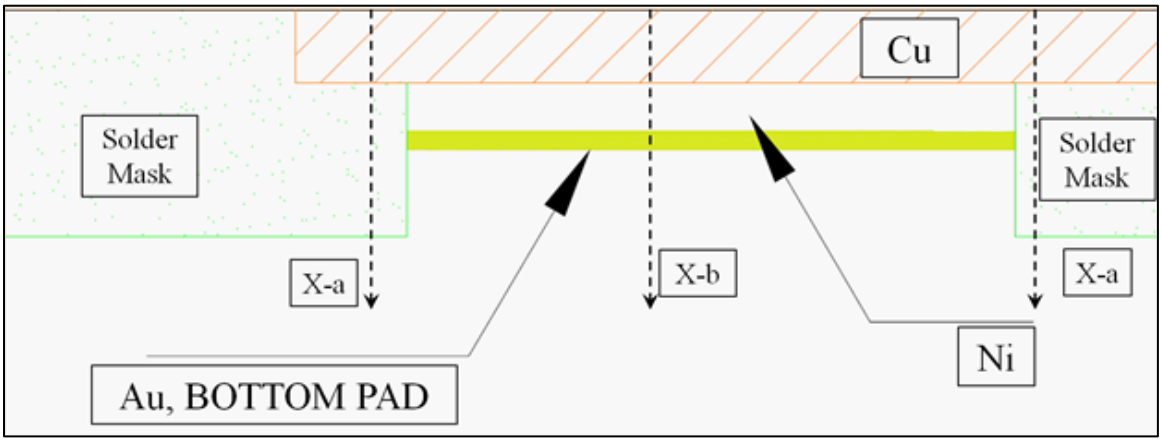


Figure 2: 12-pin 2 x 2 mm LGA package outline diagram with dimensions.

Typical LGA packages expose metal traces on the package sides, so no solder material should be allowed to contact the package sides.

Solder Pad Layer Dimensions

The solder pocket is defined by dimensions of the metal layers behind the solder pad and the solder mask around the pad.



Solder Mask (Cross Section "X-a") (µm)			
Typical Package thickness (mm)	Min	Nominal	Max
0.9	10	20	30
0.6	5	15	25

Table 1: Solder Mask (Cross Section "X-a") (µm)

Solder Pad (Cross section "X-b") (µm)			
Layer	Min	Nominal	Max
NI	3	-	12
Au	0.3	-	1.0

Table 2: Solder Pad (Cross section "X-b") (µm)

PCB Layout Recommendations

Given the above package dimensions, the following guidelines are recommended:

The PCB should be designed with NSMD (Non-Solder Mask Defined) openings for the LGA land pattern. The LGA land pattern should be an identical mirror image of the bottom pattern of the LGA package.

The pin 1 indicator triangle that is exposed on the LGA substrate does not need to be soldered to the PCB and should be left floating.

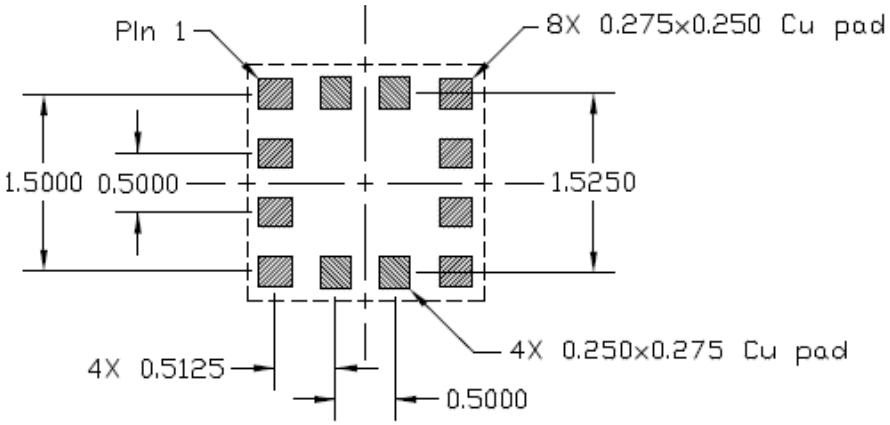


Figure 3: Example of a PCB land pattern for the 2 x 2 mm LGA package (Top view)

Note 1: Pins 1,2,3,4,7,9,10 are rotated 90° relatively to pins 5,6,11,12
Note 2: Spacing between pins 1&4 and between pins 7&10 is 1.5000mm. Spacing between pins 5&12, and between pins 6&11 is 1.5250mm.

Using a 0.0635 mm solder mask around each pad (pad dimension + 0.1270 mm), the minimum solder mask web is 0.1227 mm between I/O pads.

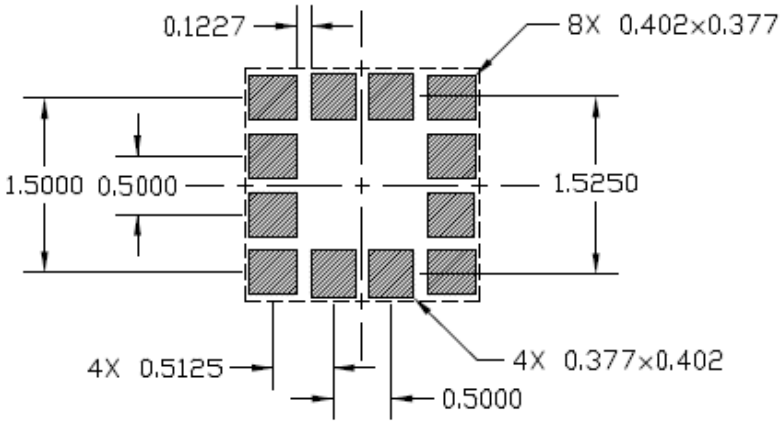


Figure 4: Example of solder mask for the 2 x 2 mm LGA package (Top view)

Solder Stencil Guidelines

A laser-cut, stainless steel stencil with electro-polished trapezoidal walls is recommended. The recommended solder stencil thickness is 0.1016 mm. The solder mask openings should be an identical mirror image of the bottom pattern of the LGA package with a 0.025mm corner radius to improve paste release.

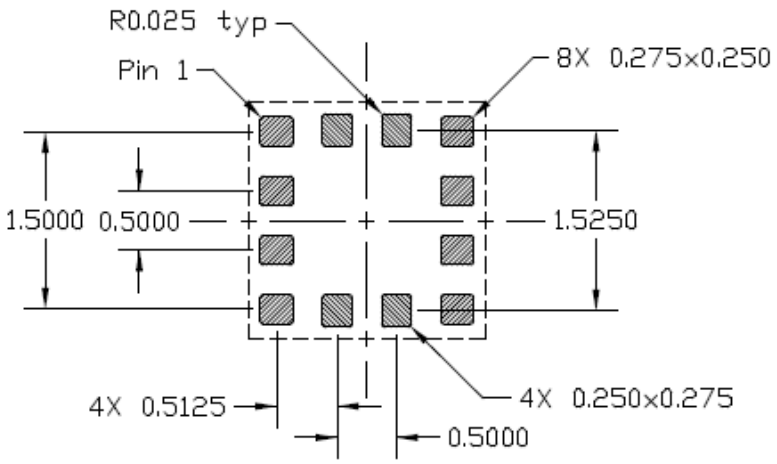


Figure 5: Example of a 12-pin 2 x 2 mm LGA solder stencil layout (Top view)

Note 1: Pins 1,2,3,4,7,9,10 are rotated 90° relatively to pins 5,6,11,12
Note 2: Spacing between pins 1&4 and between pins 7&10 is 1.5000mm. Spacing between pins 5&12, and between pins 6&11 is 1.5250mm.

PCB Via and Trace Placement

Vias are not needed for thermal dissipation, as our part doesn't generate much heat. Therefore, only electrical vias are needed. If vias are not in the land pads, then capped, plugged, tented, un-capped or un-plugged vias can be used.

To ensure optimal performance, vias and traces should not be placed on the top layer directly beneath the sensor. The sensor should be mounted over a ground plane to minimize EMI from other signals. In the case PCB assemblies are stacked, there should be a ground plane over the sensor for the same reason.

The following figures illustrate an example of proper PCB via and trace placement. Obviously, each product will present its own physical limitations for sensor placement and trace routing. Therefore, these guidelines are general in nature. Engineering judgment should be used to try to avoid metal placement directly beneath the sensor on the same layer.

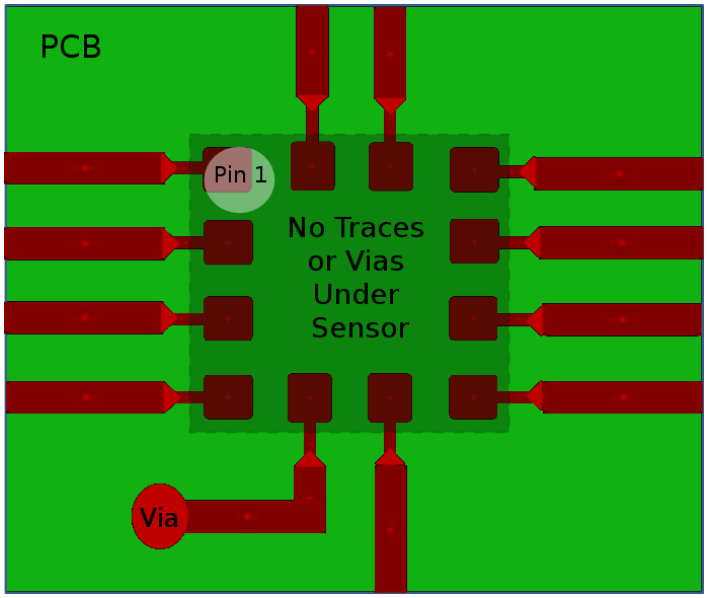


Figure 6: Via and Trace "Keep-out"
(Top View)

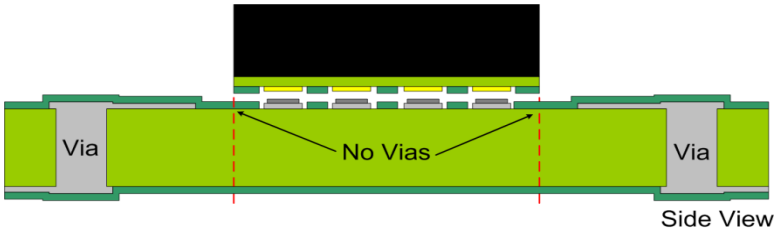


Figure 7: Via and Trace "Keep-out"
(Side View)

Tape and Reel Dimensions

The following section provides information on the tape and reel used for shipping Kionix's 2 x 2 mm LGA sensors.

Package	Tape Width	Component Pitch	Hole Pitch	Reel Diameter
LGA (2x2)	8mm	4mm	4mm	330mm

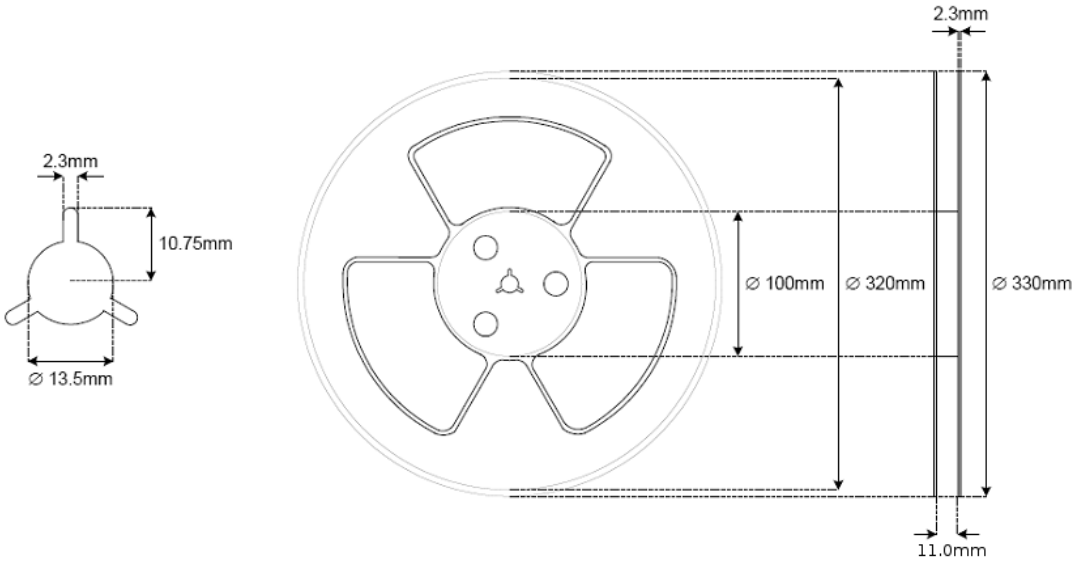


Figure 8: Dimensions of the reel

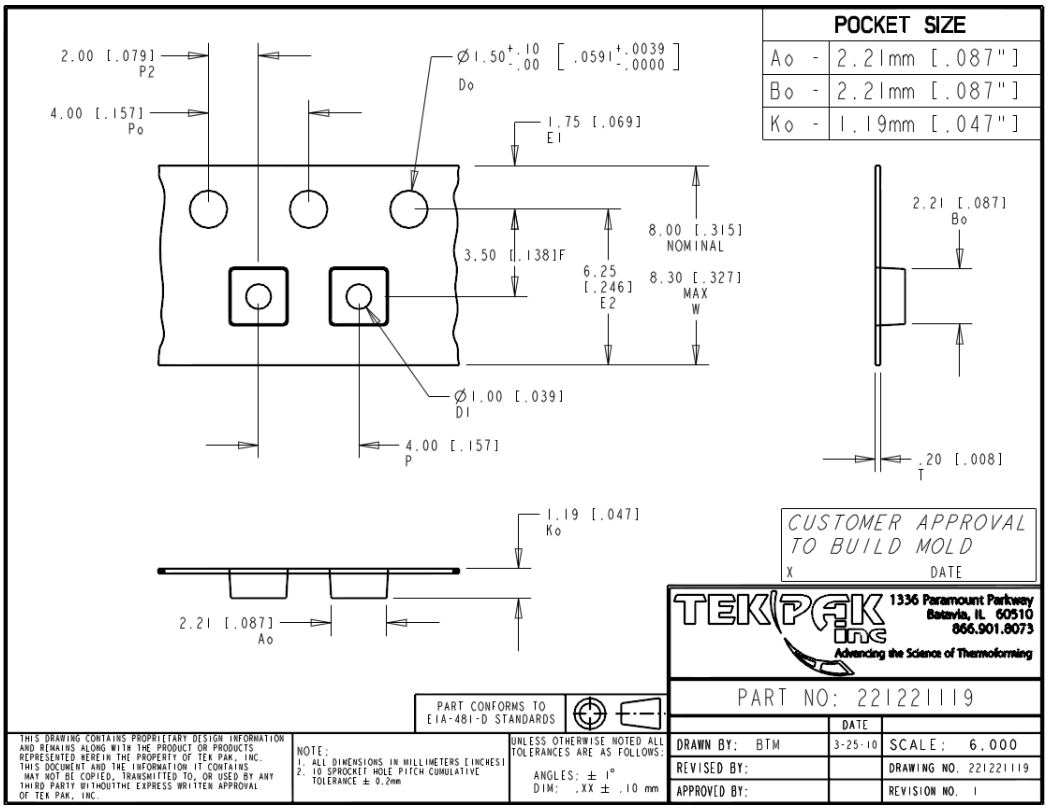


Figure 9: Carrier tape description for 2x2 mm LGA parts

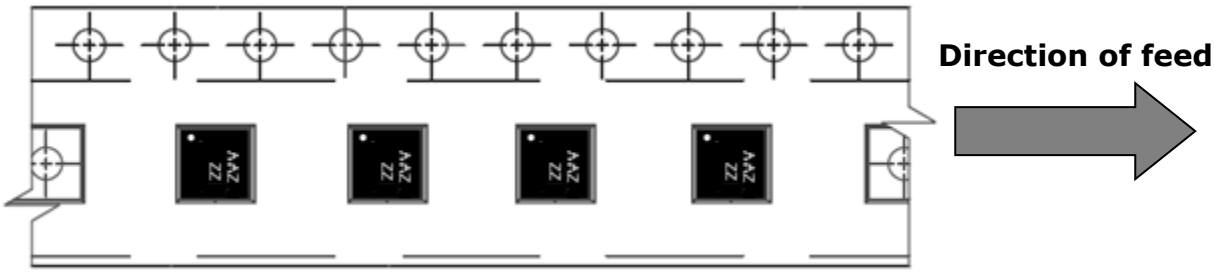


Figure 10: Orientation of the parts in the carrier tape and direction of feed

Revision History

Rev	Date	Description of Change
-	20-Apr-2012	Initial Release
1	27-Aug-2013	Added part orientation in carrier tape and direction of feed.
2	12-Jun-2014	Improved Solder Stencil Layout. Added Reel dimensions. Added Solder pad layer dimensions
3	15-Oct-2014	Added No solder on side of package recommendation.
4	02-Apr-2015	Updated package outline diagram with dimensions figure and solder stencil layout figure.
5	10-July-2015	Renamed the document
6	01-Mar-2018	Clarified that document only covers some of the available 2x2 mm LGA packages and individual product specifications needs to be consulted. Added Solder Pad Layer Dimension for 0.6mm package.
7	13-Mar-2022	Fixed component pitch value to 4mm. Update PCB Layout, Solder Stencil, and Via and Trace to current practices.
8	14-Jan-2022	Fixed component pad pitch value to 1.500mm on Figure 3, 4, and 5.
9	17-Mar-2022	Fixed component pad pitch value on Figure 3, 4, and 5. Added a note about pad pitch value for figure 3, 5.