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## Hardware Design Checklist

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### 1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip USB2412. These checklist items should be followed when utilizing the USB2412 in a new design. A summary of these items is provided in [Section 9.0, "Hardware Checklist Summary," on page 11](#). Detailed information on these subjects can be found in the corresponding sections:

- [Section 2.0, "General Considerations"](#)
- [Section 3.0, "Power"](#)
- [Section 4.0, "USB Signals"](#)
- [Section 5.0, "USB Connectors"](#)
- [Section 6.0, "Clock Circuit"](#)
- [Section 7.0, "Power and Startup"](#)
- [Section 8.0, "Miscellaneous"](#)

### 2.0 GENERAL CONSIDERATIONS

#### 2.1 Required References

The USB2412 implementor should have the following documents on hand:

- *USB2412 Data Sheet*
- AN17.17 – PCB Layout Guide for USB2.0 Hubs
- AN26.21 – USB Device Design Checklist
- EVB-USB2412 Evaluation Board Schematic

#### 2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

#### 2.3 Ground

- The VSS ePAD (pin 29), should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

#### 2.4 USB-IF-Compliant USB Connectors

- The USB2412 upstream facing port is Type-B. The hub downstream facing ports are Type-A. USB-IF-certified USB connectors with a valid Test ID (TID) are required for all USB products to be compliant and pass USB-IF product certification.

# USB2412

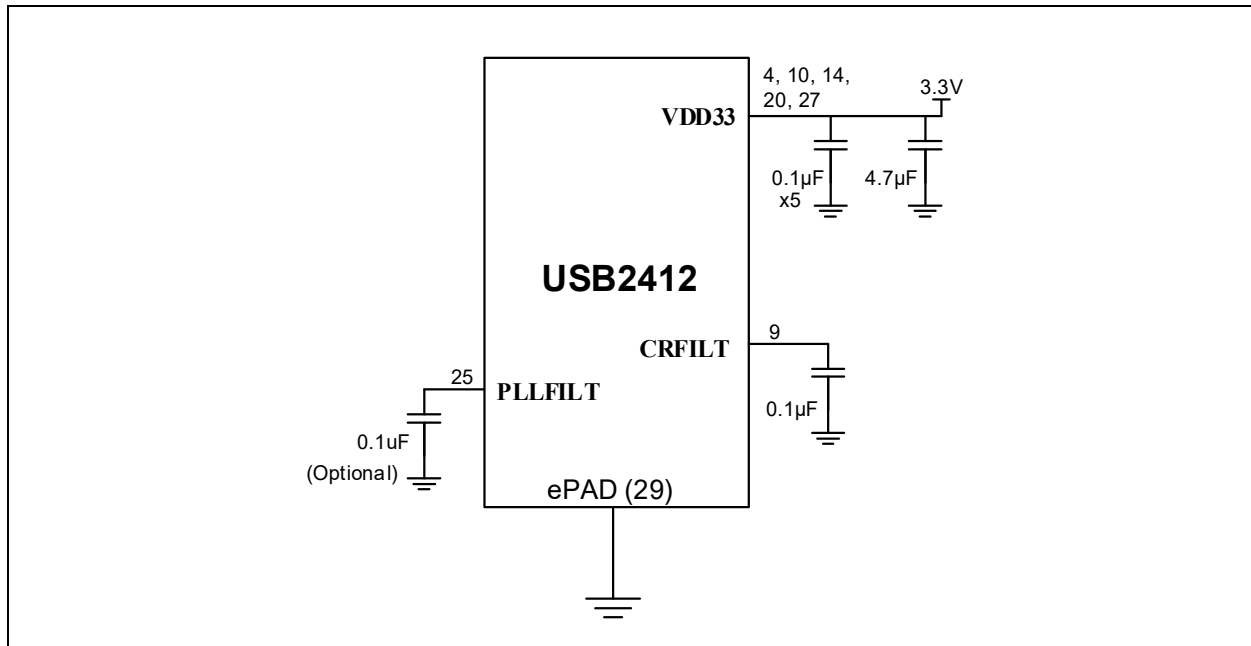
## 3.0 POWER

### 3.1 Power and Bypass Capacitance

- The **VDD33** pins (pins 4, 10, 14, 20, 27) require 0.1  $\mu\text{F}$  bypass capacitors (x5).
- The **PLLFLT** pin (pin 25) shall include a 0.1  $\mu\text{F}$  capacitor to decouple the device. The capacitor size should be SMD\_0603 or smaller.
- The **CRFLT** pin (pin 9) can have a 0.1  $\mu\text{F}$  filter capacitor to VSS or may be left unconnected.

The power and ground connections are shown in [Figure 3-1](#).

**FIGURE 3-1: POWER AND GROUND CONNECTIONS**



## 4.0 USB SIGNALS

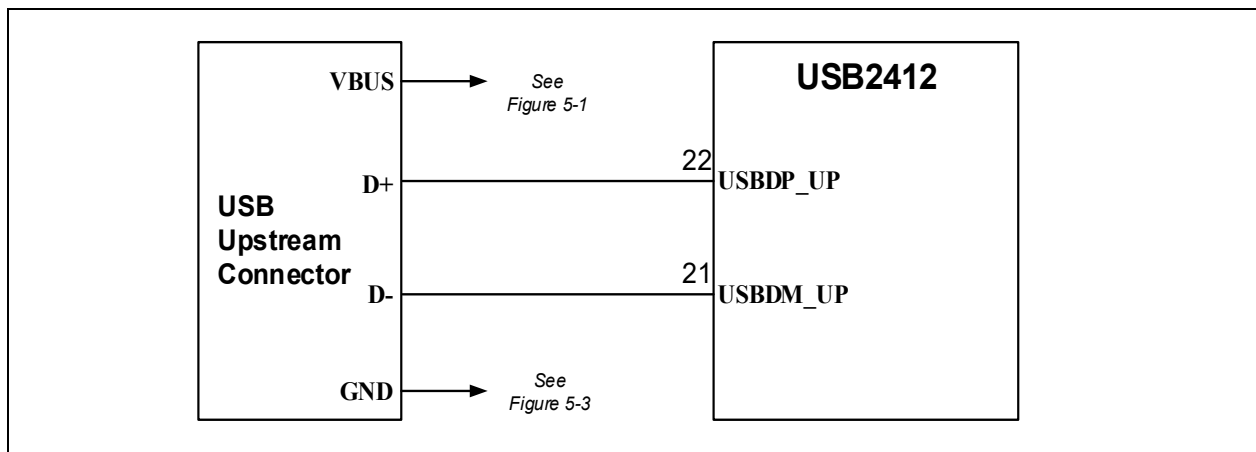
### 4.1 USB PHY Interface

- **USBDP\_UP** (pin 22): This pin is the positive (+) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D+/DP pin of a USB connector.
- **USBDM\_UP** (pin 21): This pin is the negative (-) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D-/DM pin of a USB connector.
- **USBDP\_DNx**: (pins 1 and 3) These pins are the positive (+) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. These pins can connect directly to the D+/DP pin of a USB connector.
- **USBDM\_DNx**: (pins 28 and 2) These pins are the negative (-) signal of the downstream port 1 USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. These pins can connect directly to the D-/DM pin of a USB connector.

**Note:** The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via SMBus/I<sup>2</sup>C configuration registers.

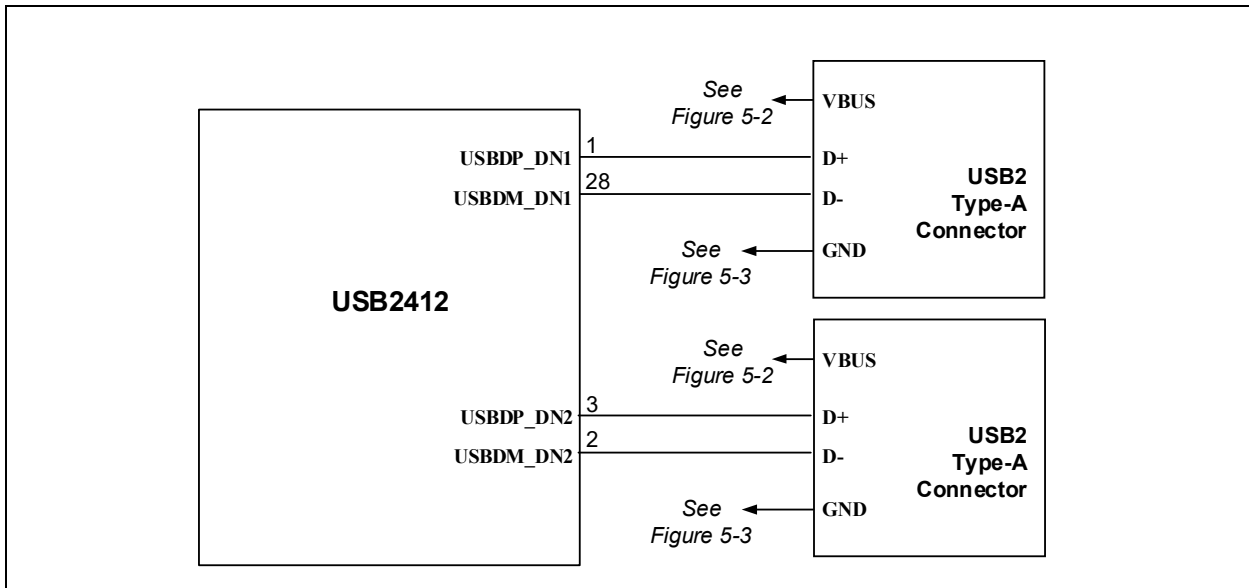
For transmit and receive channel connection details, refer to [Figure 4-1](#) and [Figure 4-2](#).

**FIGURE 4-1: TRANSMIT AND RECEIVE CHANNEL CONNECTIONS UPSTREAM USB PORTS**



# USB2412

FIGURE 4-2: TRANSMIT AND RECEIVE CHANNEL CONNECTIONS DOWNSTREAM PORTS



## 4.1.1 DISABLE DOWNSTREAM PORTS IF UNUSED

If downstream ports are unused, they should be disabled. This can be achieved through a port disable strap option.

If using the port disable strap option, the USBDP\_DNx and USBDM\_DNx signals should be pulled high to 3.3V. This connection can be made directly to the 3.3V power net, or through a pull-up resistor.

## 4.2 USB Protection

The use of external protection circuitry may be required to provide additional ESD protection beyond what is included in the hub IC. These generally are grouped into three categories:

1. TVS protection diodes
  - ESD protection for IEC-61000-4-2 system level tests
2. Application-targeted protection ICs or galvanic isolation devices
  - DC overvoltage protection for short to battery protection
3. Common-mode chokes
  - For EMI reduction

The USB2412 can be used in conjunction with these types of devices, but these devices may have a negative effect on USB signal integrity. Thus, it is important to select components accordingly and follow implementation guidelines from the device manufacturer. The following general guidelines for implementing these devices may also be observed:

- Select only devices that are designed specifically for high-speed applications. Per the USB specification, a total of 5 pF is budgeted for connector, PCB traces, and protection circuitry.
- Place these devices as close as possible to the USB connector.
- Never branch the USB signals to reach protection devices. Always place the protection devices directly on top of the USB differential traces.
- Always ensure a very low impedance path to a large ground plane. The effectiveness of TVS devices depends heavily on effective grounding.
- Place TVS diodes on the same layer as the USB signal trace. Avoid vias or place vias behind the TVS device if possible.

**Note:** Microchip PHYBoost, VariSense™, and High-Speed Disconnect Threshold adjustment configuration options are available for compensating the negative effects of these devices. These features can help to overcome marginal failures. It is simplest to determine the appropriate setting using laboratory experiments, such as USB eye diagram tests, on physical hardware.

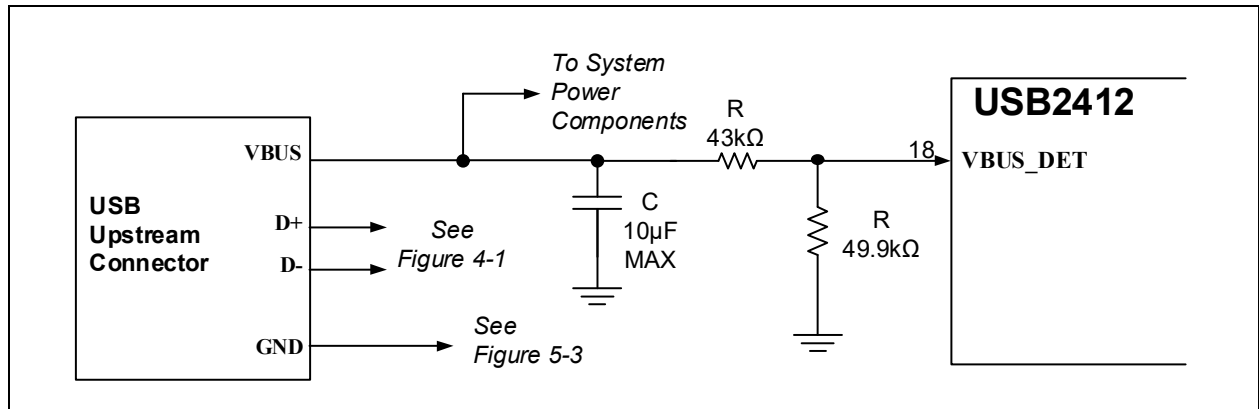
## 5.0 USB CONNECTORS

### 5.1 Upstream Port VBUS and VBUS\_DET

The upstream port VBUS line must have no more than 10  $\mu\text{F}$  in total capacitance connected. The USB2412 uses the VBUS\_DET signal to detect the presence of a USB host.

The recommended implementation is shown in [Figure 5-1](#).

**FIGURE 5-1: RECOMMENDED UPSTREAM PORT VBUS CONNECTIONS**



### 5.2 Downstream Port VBUS and PRTPWR/OCS\_N

The PRTPWR and the OCS\_N pins are hybrid I/O pins that support the following states:

- PORT OFF: PRTPWR is an output and drives low. The PRTPWR pin only transitions to the PORT ON state through a specific command from the USB host.
- PORT ON: There is an input buffer that monitors overcurrent events, which are indicated by the port power controller by pulling the OCS\_N line low. Once an overcurrent event is detected, the PRTPWR automatically moves to the PORT OFF state until the USB host can be notified of the overcurrent event.

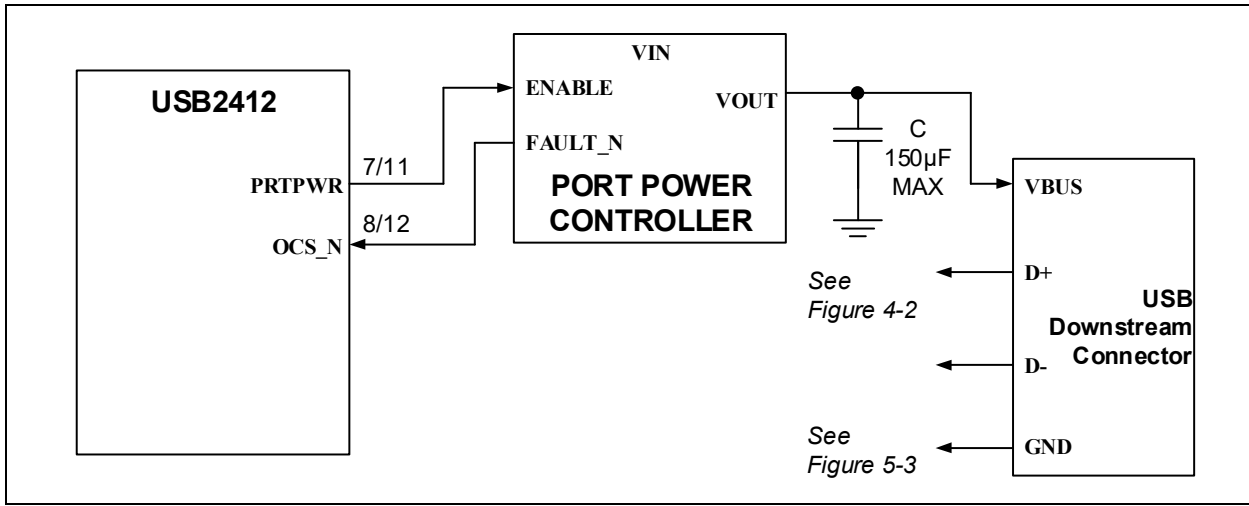
When connecting the PRTPWR/OCS\_N pins to a port power controller, the signals should be connected to both the Enable and the FAULT indicator pins of the port power controller. Do not place an external pull-up resistor on the line.

**Note:** The overcurrent detect debounce parameters are configurable and may be adjusted if required to operate properly with the selected port power controller.

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A typical implementation is shown in [Figure 5-2](#).

**FIGURE 5-2: DOWNSTREAM VBUS AND PRCTL CONNECTIONS**



**Note:** The implementation, as shown in [Figure 5-2](#), assumes that the port power controller has an active-high Enable input, and an active-low, open-drain style FAULT indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

### 5.3 GND and SHIELD Recommendations

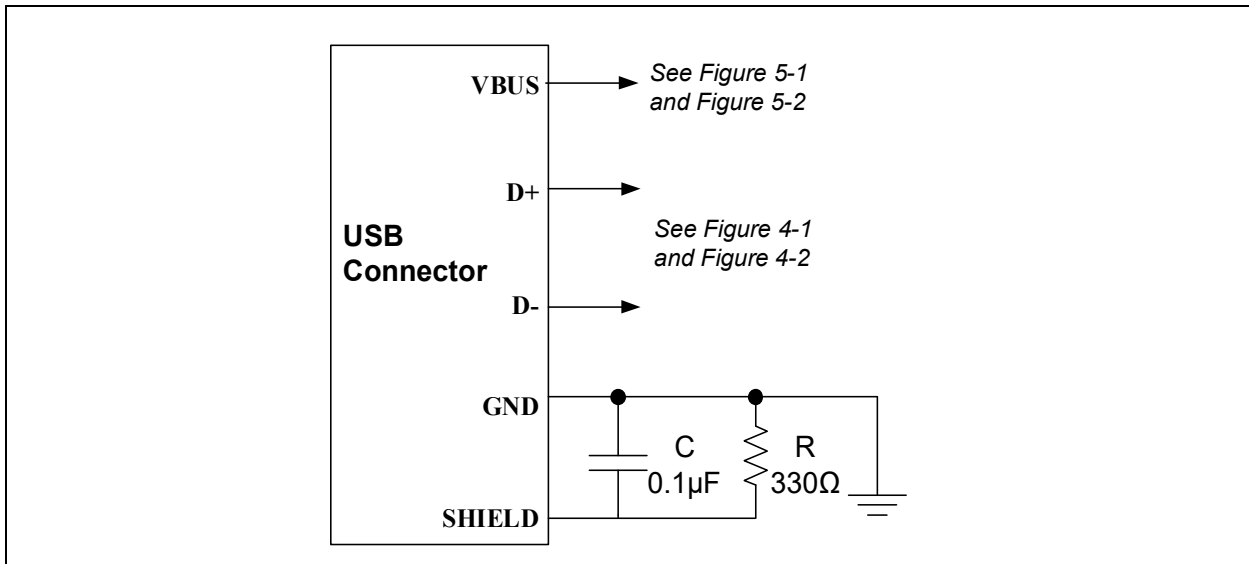
The **GND** pins of the USB connector must be connected to the PCB with a low impedance path directly to a large **GND** plane.

The **SHIELD** pins of the USB connector may be connected in one of two ways:

1. (Recommended) Connect to **GND** through a resistor and capacitor in parallel. A resistor-capacitor (RC) filter can help decouple and minimize EMI between a PCB and a USB cable.
2. Connect directly to the **GND** plane.

The recommended implementation is shown in [Figure 5-3](#).

**FIGURE 5-3: RECOMMENDED USB CONNECTOR GND AND SHIELD CONNECTIONS**



## 6.0 CLOCK CIRCUIT

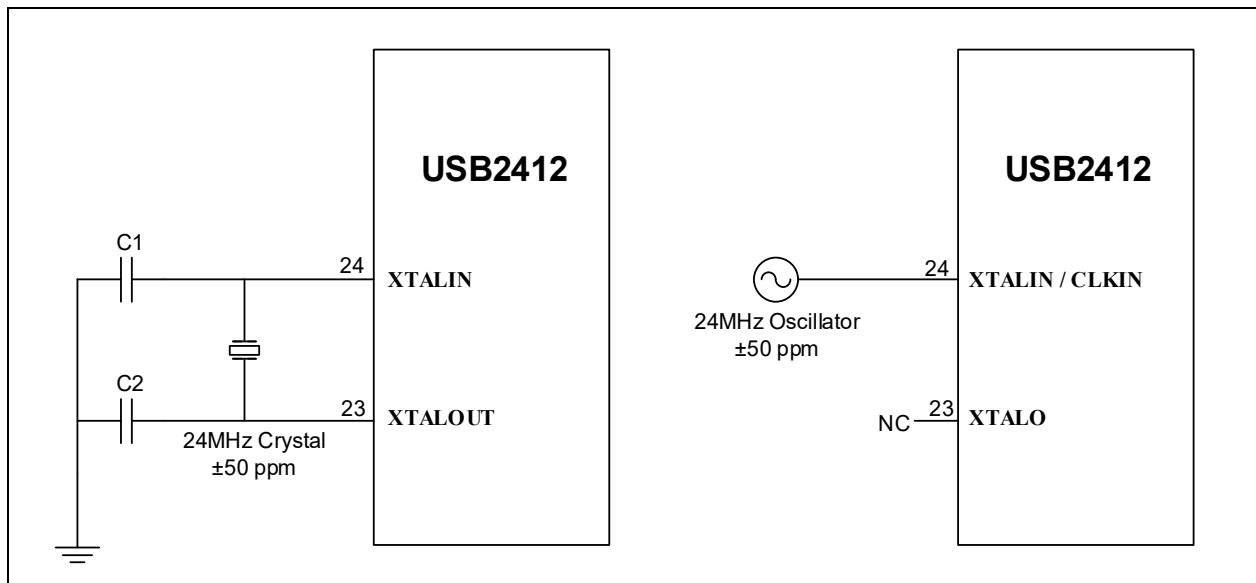
### 6.1 External Clock Connection

The REFCLK reference clock is the source for the USB interface and for all other functions of the device. For exact specifications and tolerances, refer to the latest revision of the *USB2412 Data Sheet*.

- XTALIN/CLKIN (pin 24) is the crystal/external clock circuit input for the USB2412.
- XTALOUT (pin 23) is the clock output for the USB2412. When an external clock source is used to drive XTALIN/CLKIN, leave this pin unconnected.

The crystal and oscillator connections are shown in [Figure 6-1](#).

**FIGURE 6-1: CRYSTAL AND OSCILLATOR CONNECTIONS**



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## 7.0 POWER AND STARTUP

### 7.1 Board Power Supplies

#### 7.1.1 POWER RISE TIME

- The power rail voltage and rise time should adhere to the supply rise time specification as defined in the *USB2412 Data Sheet*.
- If a monotonic or fast power rail rise cannot be assured, then the **RESET\_N** signal should be controlled by a Reset supervisor and only released when the power rail has reached a stable level.

#### 7.1.2 CURRENT CAPABILITY

- It is important to size the 5V and 3.3V power rails appropriately. Please refer to the product data sheet for the power requirements for the specific device. The 5V power supply must be capable of supplying 500 mA (if BC1.2 is not enabled), 1.5A (if BC1.2 is enabled), or up to 2.4A (if certain vendor-specific current negotiation with the USB host is enabled) to the USB downstream port VBUS without dropping below the minimum voltage permissible in the USB specification.
- The 3.3V power supply must be able to supply enough power to the USB hub IC. It is recommend that 3.3V power rail be sized, such that it is able to supply the maximum power consumption specification as displayed in the *USB2412 Data Sheet*.

### 7.2 Reset Circuit

- **RESET\_N** (pin 17) is an active-low Reset input. This signal resets all logic and registers within the USB2412. A hardware reset (**RESET\_N** assertion) is not required following power-up. Refer to the latest copy of the *USB2412 Data Sheet* for Reset timing requirements. [Figure 7-1](#) shows a recommended Reset circuit for powering up the USB2412 when Reset is triggered by the power supply.

**FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY**

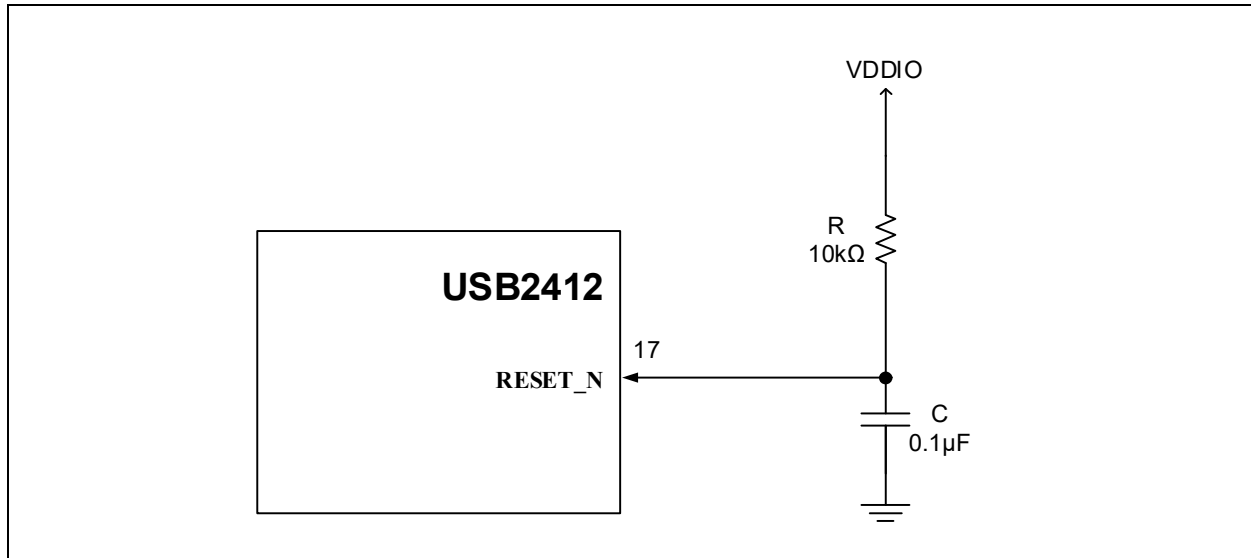
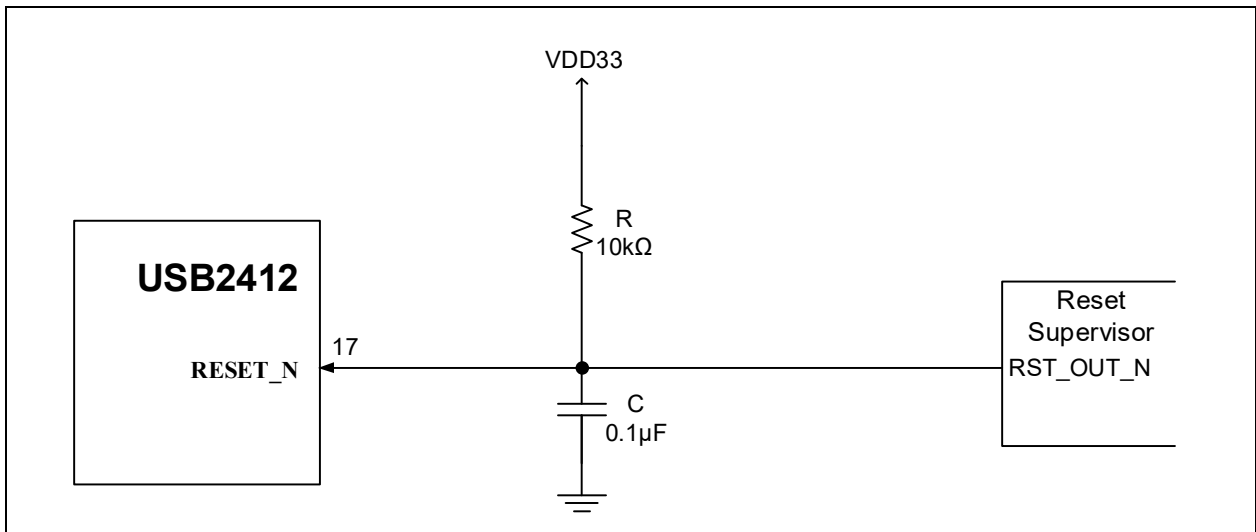




Figure 7-2 details the recommended Reset circuit for applications where Reset is driven by an external CPU/MCU. The Reset out pin (**RST\_OUT\_N**) from the CPU/MCU provides the warm Reset after power-up.

**FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/MCU RESET OUTPUT**



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## 8.0 MISCELLANEOUS

### 8.1 Self-Powered/Bus-Powered Settings

In a typical USB2412 application, the hub should be configured as self-powered, which is the default configuration setting.

The following guidelines can be used to determine which setting to use:

- If the entire system (hub included) is powered completely from the upstream USB connector's **VBUS** pin and the system is designed to operate using standard USB cabling and any standard USB host, then the hub system is **bus-powered**.
- If the entire system (hub included) is always powered by a separate power connector, then the hub system is **self-powered**.
- If the hub included is part of a larger embedded system with fixed cabling and a fixed USB host, then the hub system is most likely **self-powered** (even if all of the power is derived from the upstream USB connector's **VBUS** pin).

**Note:** The self-powered/bus-powered device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors, which the USB host uses to budget power accordingly. Since a standard USB2.0 port is required to supply 500 mA to the downstream port, a self-powered hub and all of its downstream ports must continue to operate within that 500 mA budget. A USB host typically limits the downstream ports of a bus-powered hub to 100 mA. Any device that connects to a bus-powered hub, which declares it needs more than 100 mA, will be prevented from operating by the USB host.

## 9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All the required references are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	The grounds are tied together.		
	Section 2.4, "USB-IF-Compliant USB Connectors"	USB-IF-compliant USB connectors with an assigned TID are used in the design (if USB compliance is required for the design).		
Section 3.0, "Power"	Section 3.0, "Power"	The VDD33 is within the range of 3.0V to 3.6V and a 0.1 $\mu$ F capacitor is on the pin.		
		PLLFLT has a 1.0 $\mu$ F capacitor to GND.		
		CRFLT has a 0.1 $\mu$ F capacitor to GND or unconnected.		
Section 4.0, "USB Signals"	Section 4.1, "USB PHY Interface"	The USB data pins are correctly routed to the USB connectors. (Pay special attention to the polarity of the USB2.0 D+ and D- data lines.)		
	Section 4.2, "USB Protection"	The ESD/EMI protection devices are designed specifically for high-speed data applications. In addition, the combined parasitic capacitance of the protection devices, USB traces, and USB connector do not exceed 5 pF on each USB trace.		
Section 5.0, "USB Connectors"	Section 5.1, "Upstream Port VBUS and VBUS_DET"	The upstream port VBUS has no more than 10 $\mu$ F capacitance, and the VBUS signal is properly divided down to a 3.3V signal and connected to the VBUS_DET pin of the hub.		
	Section 5.2, "Downstream Port VBUS and PRT_PWR/OCS_N"	The PRT_CTL is properly connected to both the Enable pin of the downstream port power controller and the FAULT indicator output of the port power controller.		
	Section 5.3, "GND and SHIELD Recommendations"	The USB connector is properly connected to PCB ground on both the GND pins and the SHIELD pins. It is recommended that an RC filter be placed between the SHIELD pins and PCB ground.		
Section 6.0, "Clock Circuit"	Section 6.1, "External Clock Connection"	The REFCLK input is connected to a positive square wave clock source from 0V to 3.6V.		

**TABLE 9-1: HARDWARE DESIGN CHECKLIST (CONTINUED)**

Section	Check	Explanation	√	Notes
Section 7.0, "Power and Startup"	Section 7.1, "Board Power Supplies"	<p>The board power supplies deliver 3.0V to 3.6V to the hub power rails, and the power-on rise time meets the requirement of the hub as defined in the data sheet.</p> <p>If the rise time requirement cannot be met, the <b>RESET_N</b> line is held low until the power regulators reach a steady state.</p>		
	Section 7.2, "Reset Circuit"	The <b>RESET_N</b> signal has an external pull-up resistor, or is otherwise properly controlled by an external SoC, MCU, or Reset supervisor device.		
Section 8.0, "Miscellaneous"	Section 8.1, "Self-Powered/Bus-Powered Settings"	<p>Verify the application requirements for Self-Powered or Bus-Powered operation.</p> <p>If self-powered operation is required, then no additional configuration or circuitry is required. If bus-powered operation is required, then the hub must be configured via OTP or I<sup>2</sup>C/SMBus.</p>		

## APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004537A (05-26-22)	Initial release	

# USB2412

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