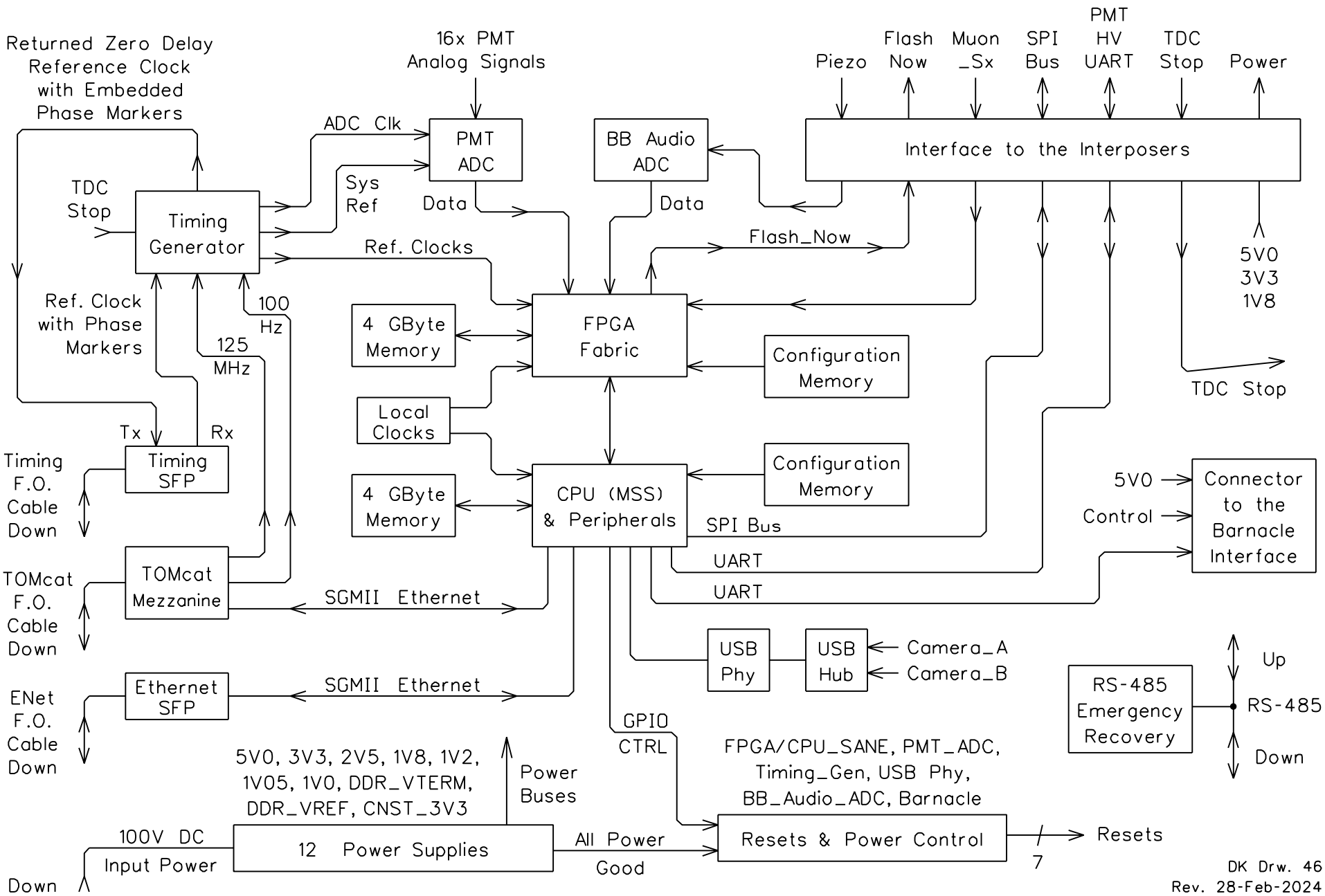
Disco-Kraken Circuit Diagram Index - Current Design

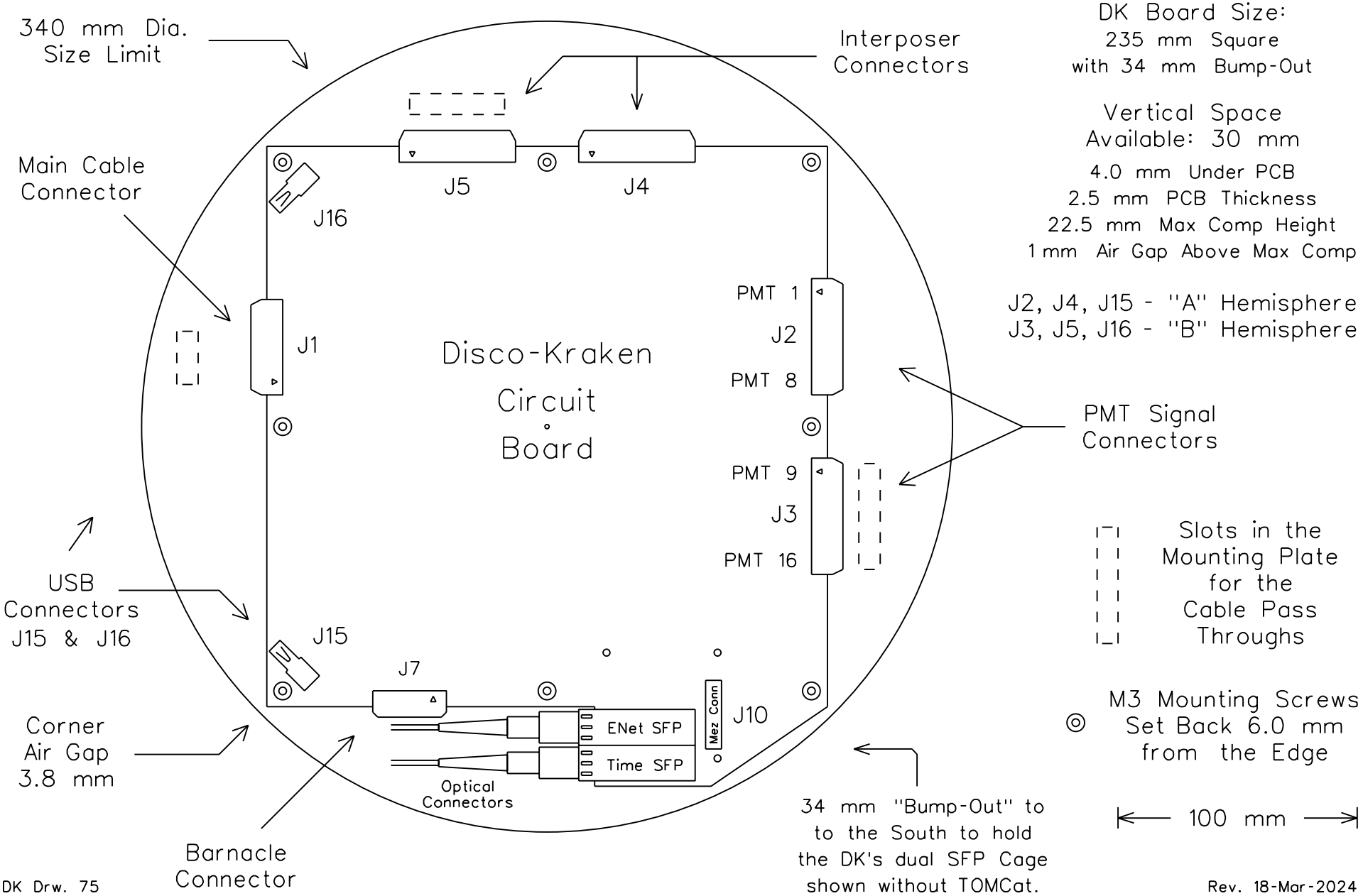
Rev. 26-July-2024

All files on web: https://web.pa.msu.edu/people/edmunds/Disco_Kraken/

DK Board - Simplified Block Diagram



DK with a Bump-Out for its SFPs



DK Board Size:
235 mm Square
with 34 mm Bump-Out

Vertical Space
Available: 30 mm

4.0 mm Under PCB
2.5 mm PCB Thickness
22.5 mm Max Comp Height
1 mm Air Gap Above Max Comp

J2, J4, J15 - "A" Hemisphere
J3, J5, J16 - "B" Hemisphere

PMT Signal
Connectors

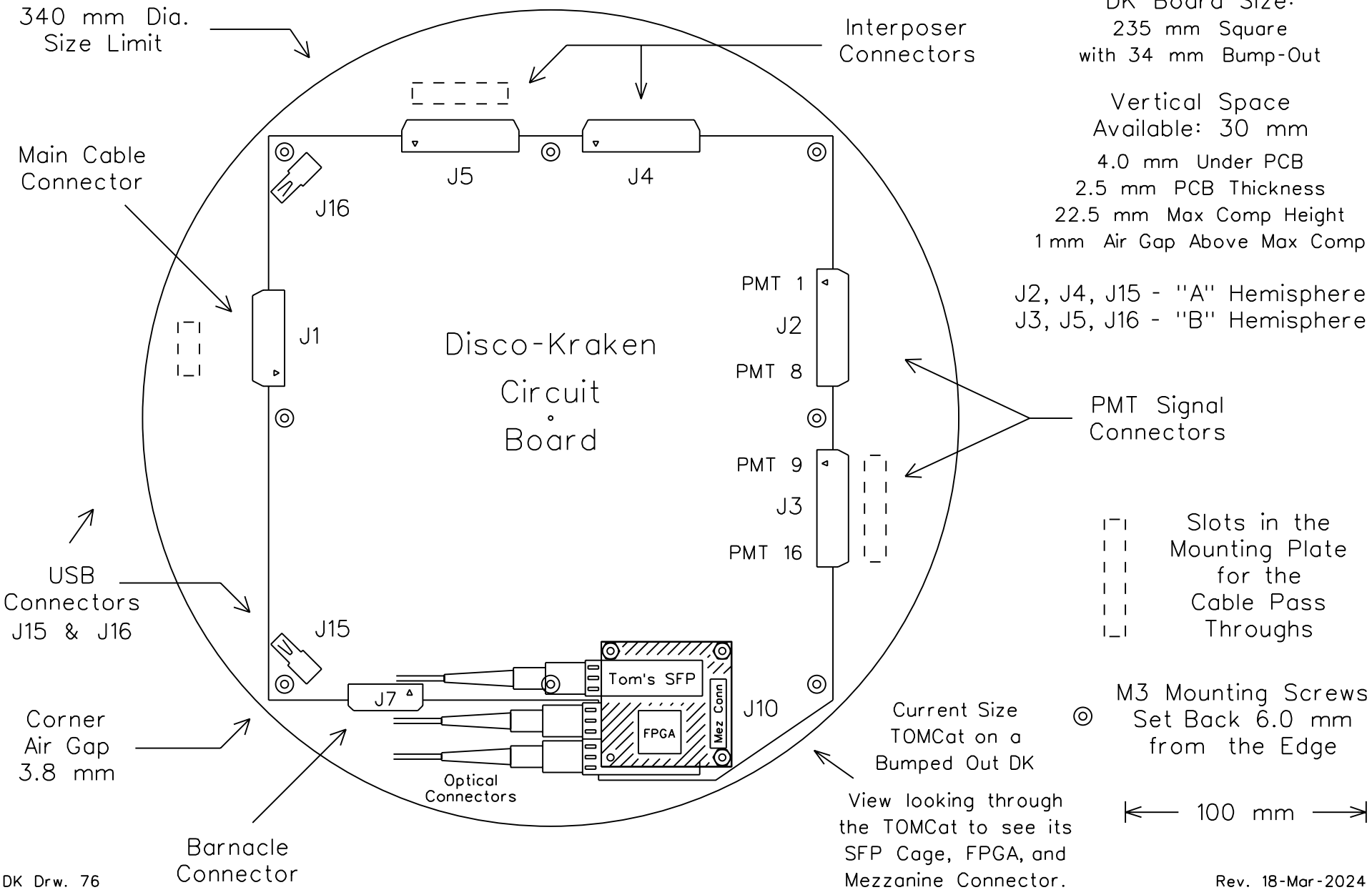
Slots in the
Mounting Plate
for the
Cable Pass
Throughs

M3 Mounting Screws
Set Back 6.0 mm
from the Edge

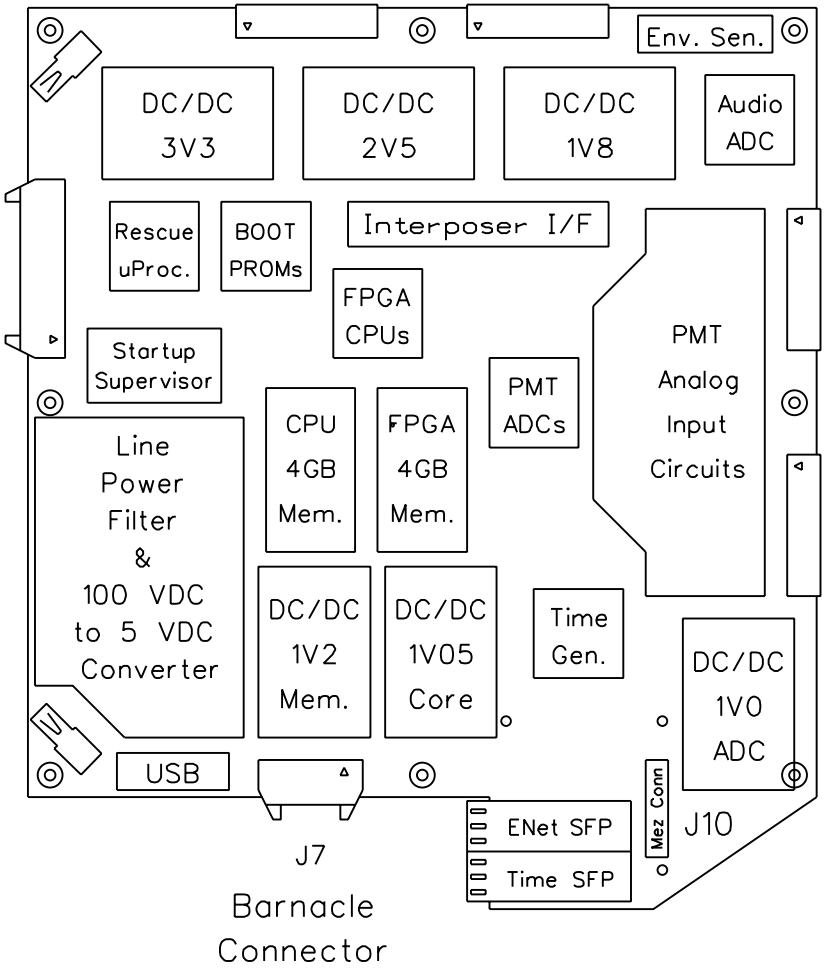
DK Drw. 75

Rev. 18-Mar-2024

Bumped Out DK with a TOMCat Installed



Disco-Kraken - PCB Floor Plan



DK Board Size:
235 mm Square
plus 34 mm Bump-Out
on the South Edge

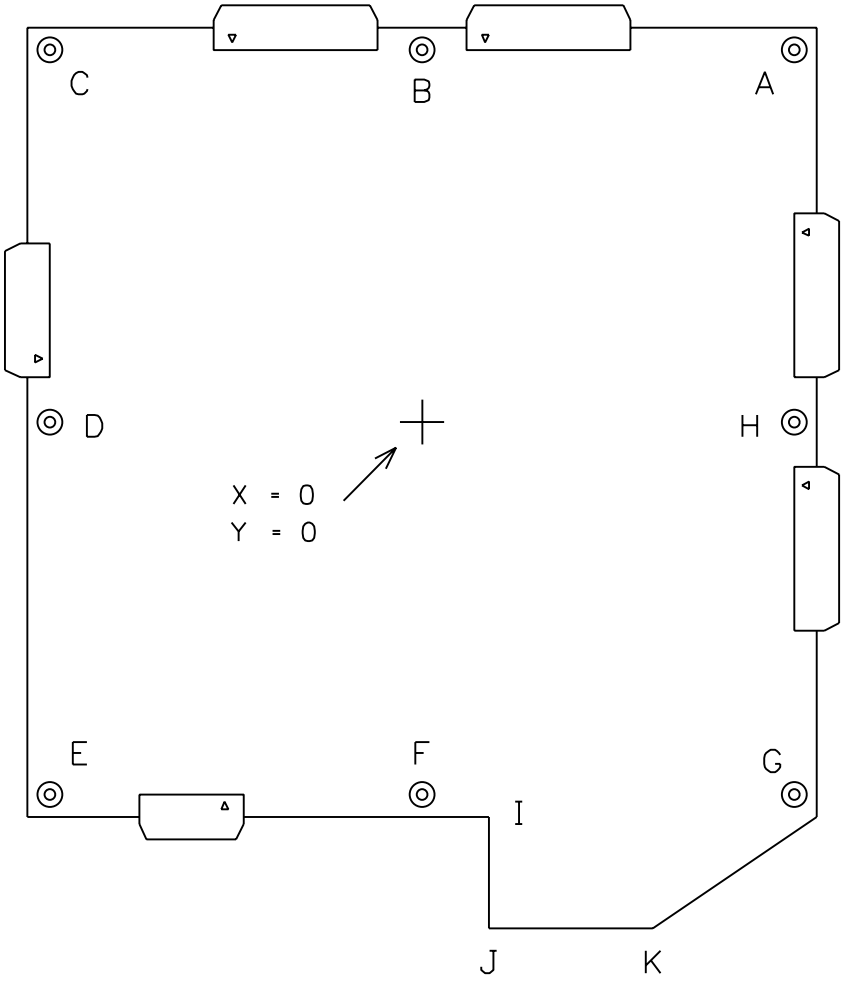
Vertical Space
Available: 30 mm
4.0 mm Under PCB
2.5 mm PCB Thickness max
22.5 mm Max Comp Height
1 mm Air Gap Above Max Comp

The shown locations and areas are only the current estimates.

Many functions and connectors are not shown.

◎ Mounting Screws

Disco-Kraken - Mounting Hole & Corner Locations



Board Corner Locations
Relative to the Center

Corner	X	Y
A	117,5	117,5
C	-117,5	117,5
E	-117,5	-117,5
I	20,5	-117,5
J	20,5	-151,5
K	68,5	-151,5
G	117,5	-117,5

Mounting Hole Locations
Relative to the Center

Hole	X	Y
A	111,5	111,5
B	0,0	111,5
C	-111,5	111,5
D	-111,5	0,0
E	-111,5	-111,5
F	0,0	-111,5
G	111,5	-111,5
H	111,5	0,0

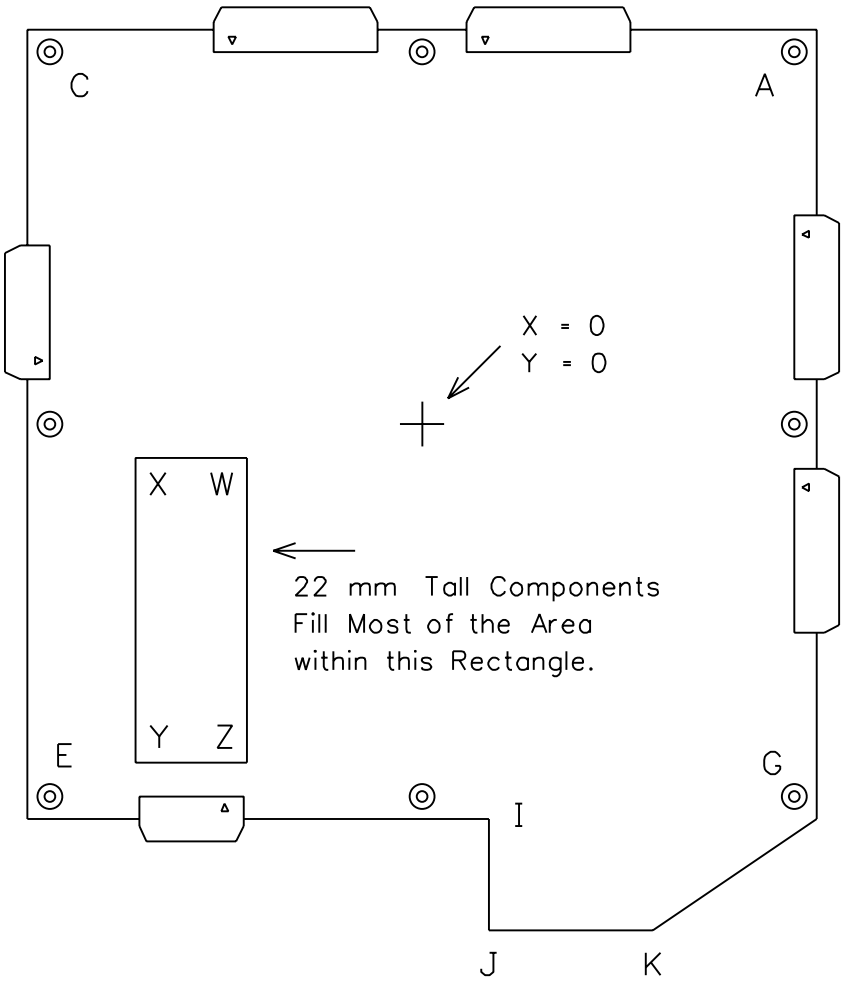
DK Board Size:

235 mm Square plus a
34 mm Bump-Out on the South Edge

◎ M3 Mounting Screws
Set Back 6.0 mm
from the Edge

DK Drw. 65
Rev. 18-Mar-2024

Disco-Kraken - Tallest Component Location



Board Corner Locations
Relative to the Center

Corner	X	Y
A	117,5	117,5
C	-117,5	117,5
E	-117,5	-117,5
I	20,5	-117,5
J	20,5	-151,5
K	68,5	-151,5
G	117,5	-117,5

22 mm Tall Component Location
Relative to the Board's Center

Location Corner	X	Y
W	-52,2	-10,5
X	-85,8	-10,5
Y	-85,8	-101.0
Z	-52,2	-101,0

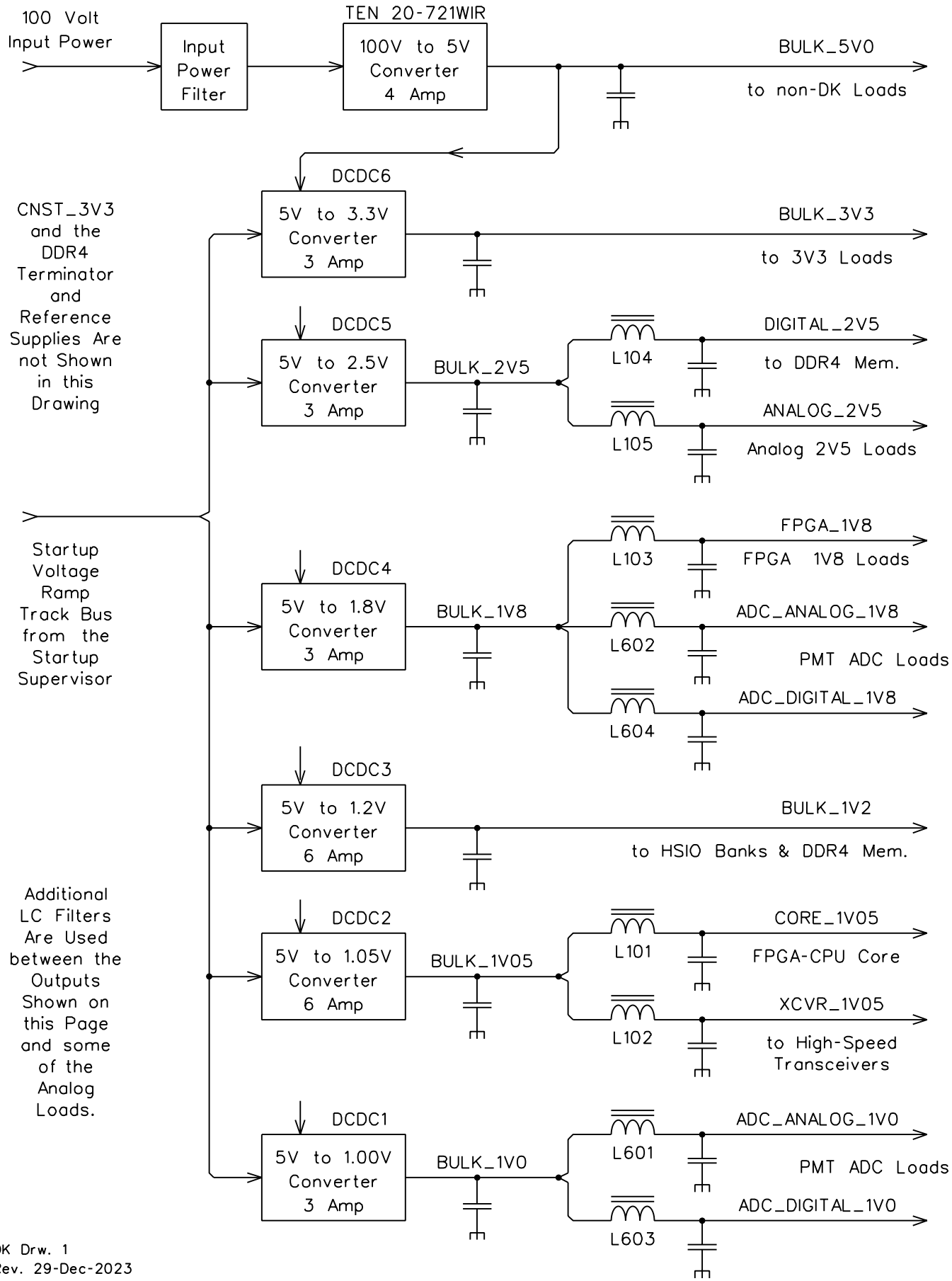
DK Board Size:

235 mm Square plus a
34 mm Bump-Out on the South Edge

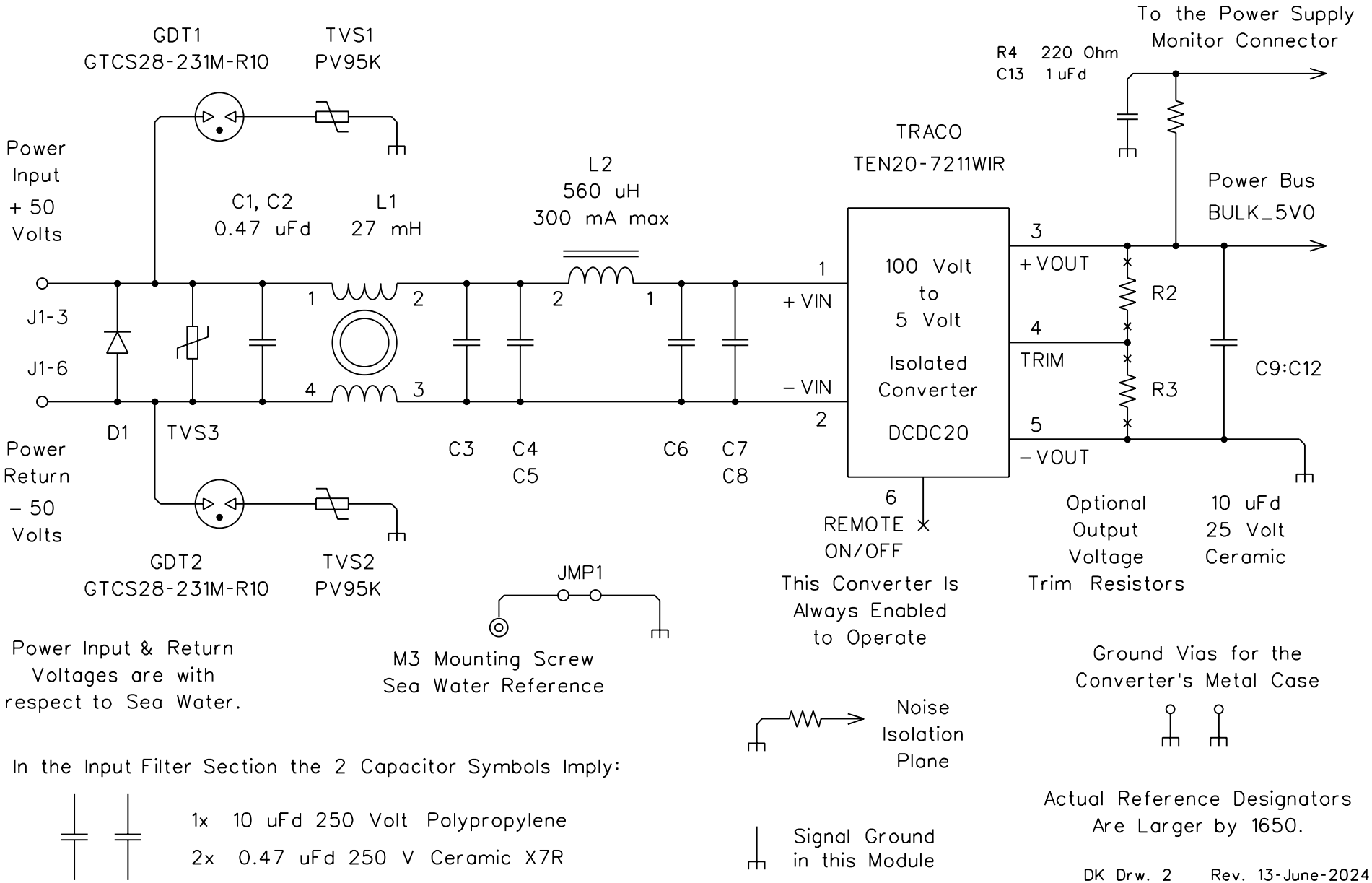
◎ M3 Mounting Screws
Set Back 6.0 mm
from the Edge

DK Drw. 91
Rev. 17-July-2024

DK Board Power Supplies

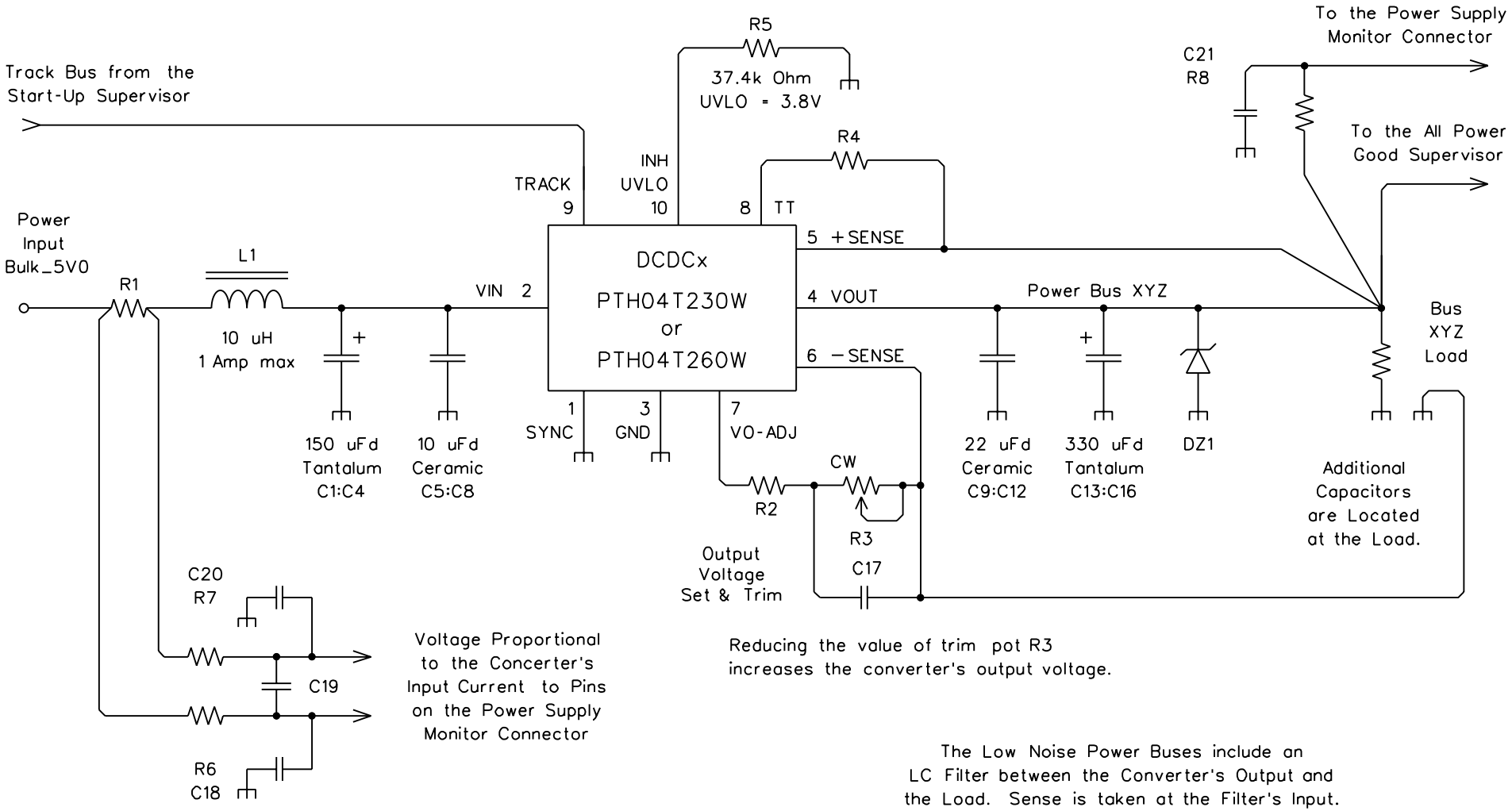


DK Board Input Power to 5 Volt Converter



DK Drw. 2 Rev. 13-June-2024

DK Board DC-DC Converter Design



The Low Noise Power Buses include an LC Filter between the Converter's Output and the Load. Sense is taken at the Filter's Input.

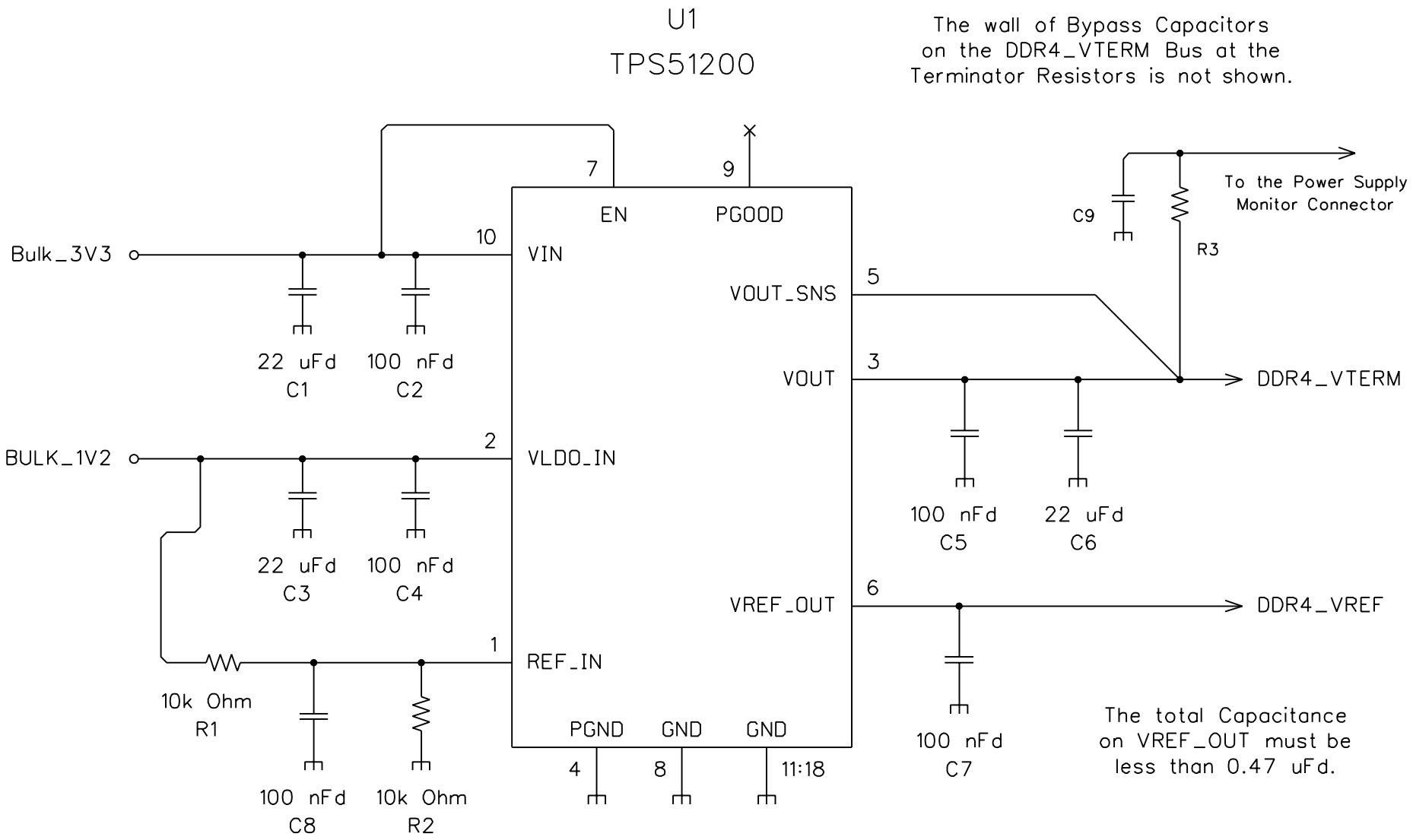
R1 is 5 to 30 mOhm depending on the DCDC Converter.

All 6 DCDC Converters are similar in design. Actual reference designators are larger by 1700. Reference designators increment by 30 from one converter to the next.

The RC Filters for the Power Supply Monitors:
220 Ohm Resistors
1 uFd Capacitors
220 usec 723 Hz

DK Drw. 3
Rev. 2-Jan-2024

DDR4 Reference and Terminator Supplies

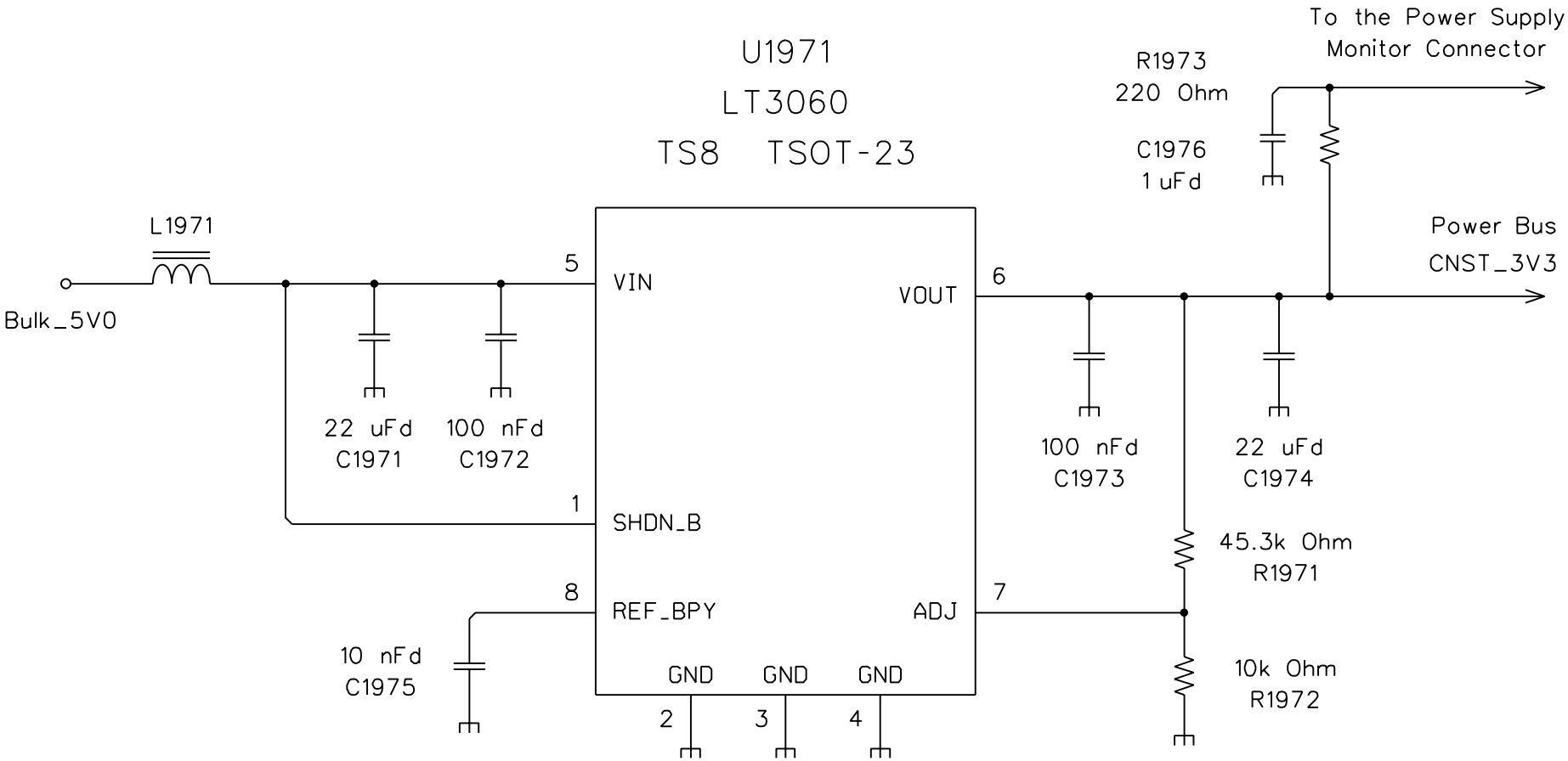


There are separate
TPS51200 DDR4 Terminator & Reference
Supplies for the Fabric and CPU memory arrays.

The Reference Designators Start at:
1921 for the FPGA DDR4 Term Ref. Supply
1941 for the CPU DDR4 Term Ref. Supply

DK Drw. 6
Rev. 20-June-2024

DK Board CNST_3V3 Supply



The 10 nFd REF-BPY capacitor gives a startup time of about 10 msec.

The CNST_3V3 bus provides power whenever the BULK_5V0 bus is above about 3.6 Volts.

The LT3060's Internal Reference is 600 mV. Maximum output current is 100 mA with a typical drop of 300 mV.

Rev. 3-Jan-2024

FPGA/CPU - Power Bus Connections

DK SUPPLY	Microchip NAME	FUNCTION
CORE_1V05	VDD	Core Supply
FPGA_1V8	VDD18	Prgm & HSIO Aux
Analog_2V5	VDD25	PLLs and PNVM
XCVR_1V05	VDDA	XCVR Power
Analog_2V5	VDDA25	XCVR PLLs
Analog_2V5	XCVR_CLK	XCVR Clk Buffers
10k Ohm to Gnd	XCVR_REF	XCVR Clk Ref.

DK SUPPLY		Microchip NAME	FUNCTION
BULK_1V2		VDDI0	I/O Bank 0 FPGA HSIO FPGA DDR4 Memory
BULK_3V3 BULK_3V3	*	VDDI1 VDDAUX1	I/O Bank 1 FPGA GPIO DK's 3V3 I/O
BULK_3V3 BULK_3V3	*	VDDI2 VDDAUX2	I/O Bank 2 CPU I/O USB UPLI & QSPI
BULK_3V3		VDDI3	I/O Bank 3 Controller JTAG & Controller SPI
10k Ohm Gnd 10k Ohm Gnd	*	VDDI4 VDDAUX4	I/O Bank 4 CPU I/O Not Used No Power
BULK_3V3		VDDI5	I/O Bank 5 CPU SGMII Used only for CPU Clk
BULK_1V2		VDDI6	I/O Bank 6 CPU DDR CPU DDR4 Memory
BULK_3V3 BULK_3V3	*	VDDI7 VDDAUX7	I/O Bank 7 FPGA GPIO If Used It's 3V3
10k Ohm Gnd		VDDI8	I/O Bank 8 FPGA HSIO Not Used No Power
FPGA_1V8 DIGITAL_2V5	*	VDDI9 VDDAUX9	I/O Bank 9 FPGA GPIO DK's 1V8 I/O

* When an FPGA GPIO Bank or a CPU IO Bank operates from 2V5 or 3V3 power then that Bank's Auxiliary supply must come from the same 2V5 or 3V3 bus.

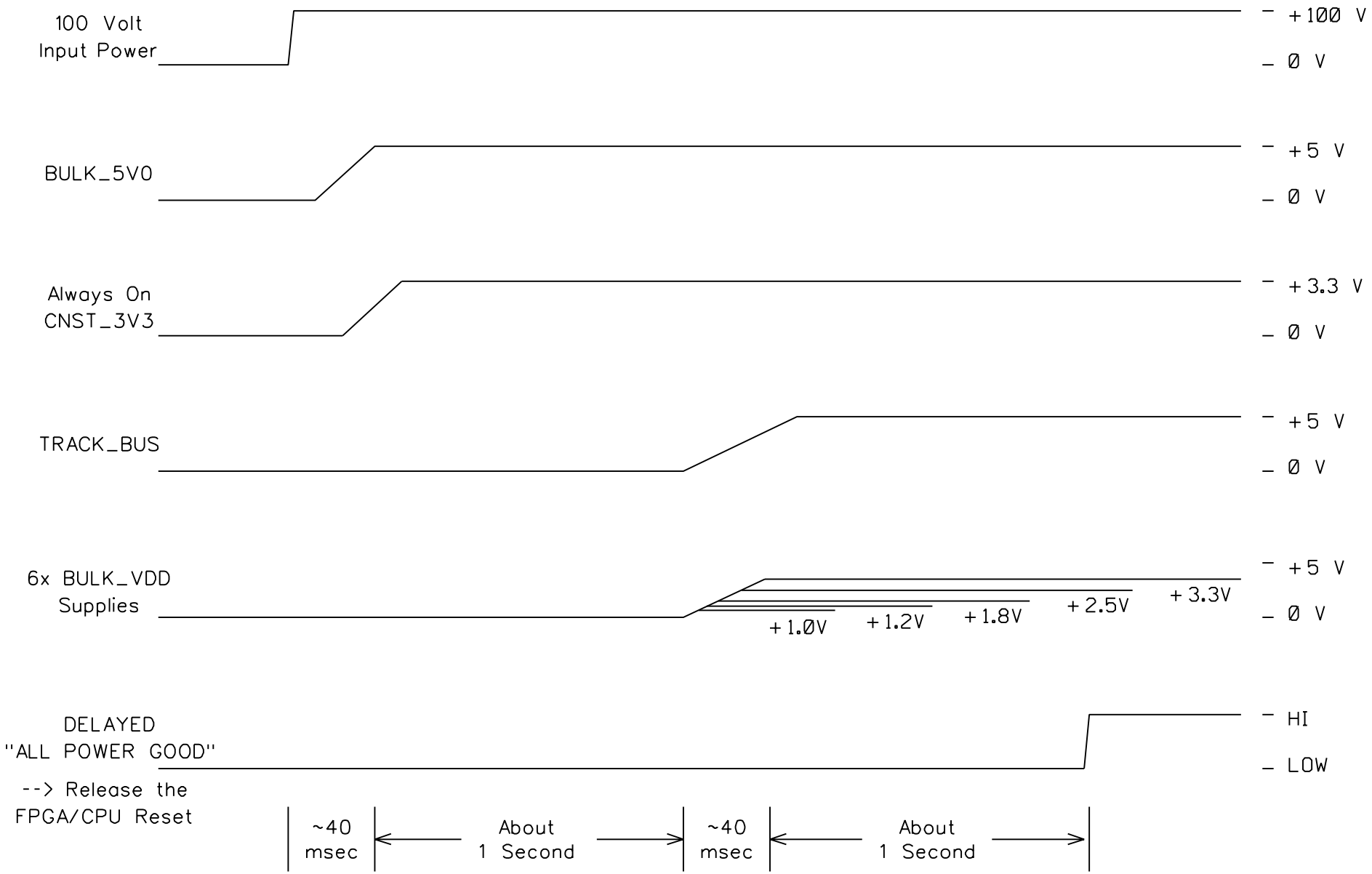
* When an FPGA GPIO Bank or a CPU IO Bank operates from 1V8 or lower voltage power then that Bank's Auxiliary supply must come from the 2V5 bus.

DK Drw. 45

Do not confuse VDD18 and VDDI8.

Rev. 15-Jan-2024

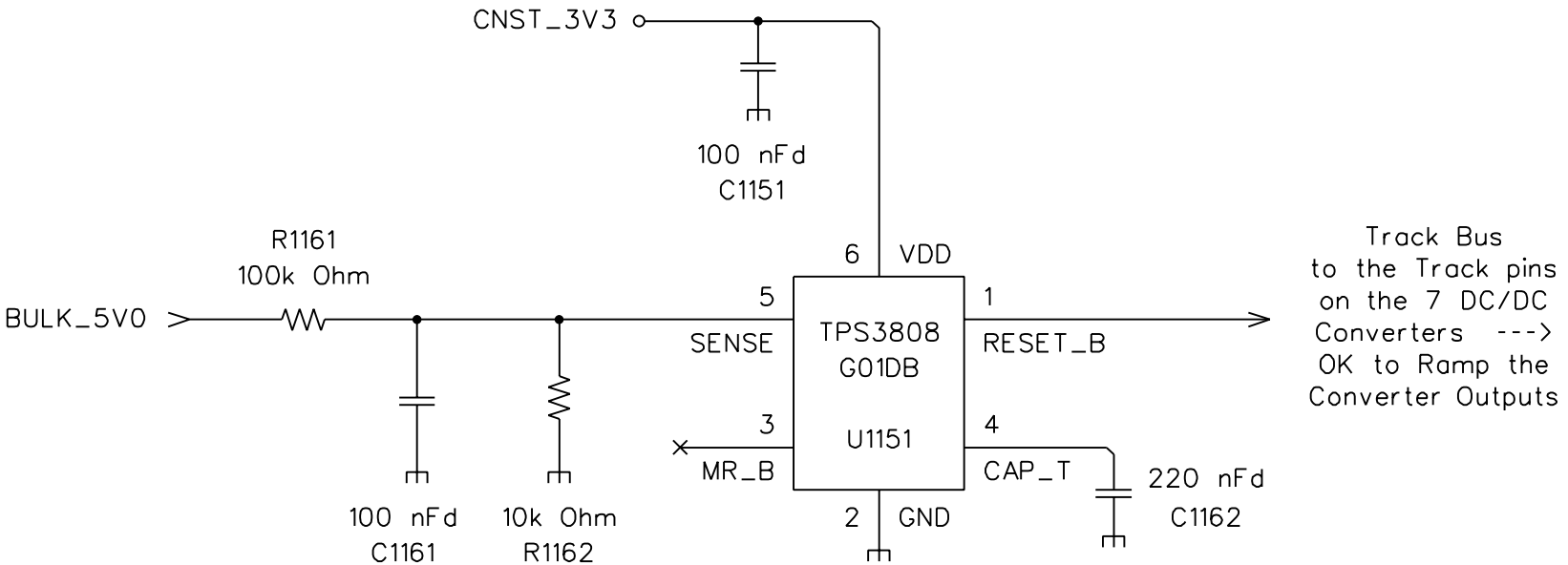
DK Board Power Supply Startup



Rev. 5-Jan-2024

DK Drw. 9

DK Board Power Supply Startup Supervisor



The 10k Ohm and 100 nFd provide about 1 msec of filtering.

The Internal Reference of the TPS3808 is 0.405 Volts.

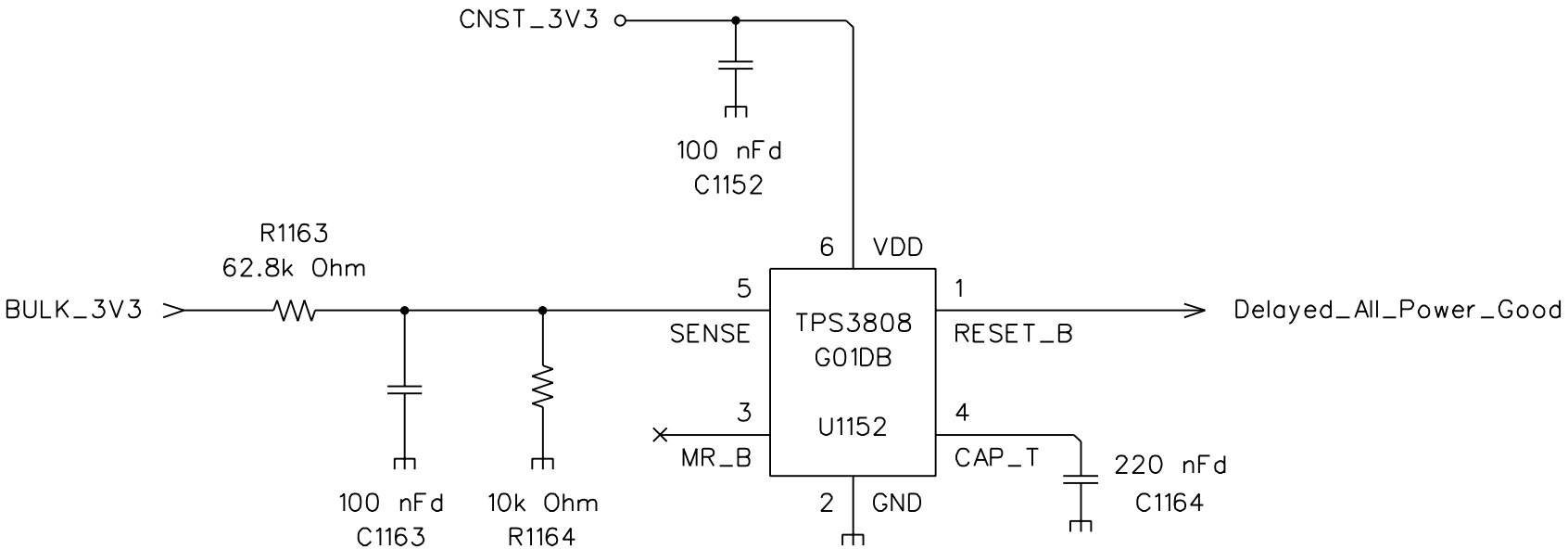
R1161 and R1162 imply a threshold of about 4.455 Volts on BULK_5V0.

The 220 nFd timing Capacitor implies about 1.2 seconds of delay between BULK_5V0 reaching its threshold and the Track Bus starting to ramp up.

The RESET_B pin is an Open Drain output.

The RESET_B pin is Low until the Sense pin is Above Threshold AND the Delay Period has has elapsed.

All Power Good Supervisor



The 10k Ohm and 100 nFd provide about 1 msec of filtering.

The Internal Reference of the TPS3808 is 0.405 Volts.

R1163 and R1164 imply a threshold of about 2.950 Volts on BULK_3V3.

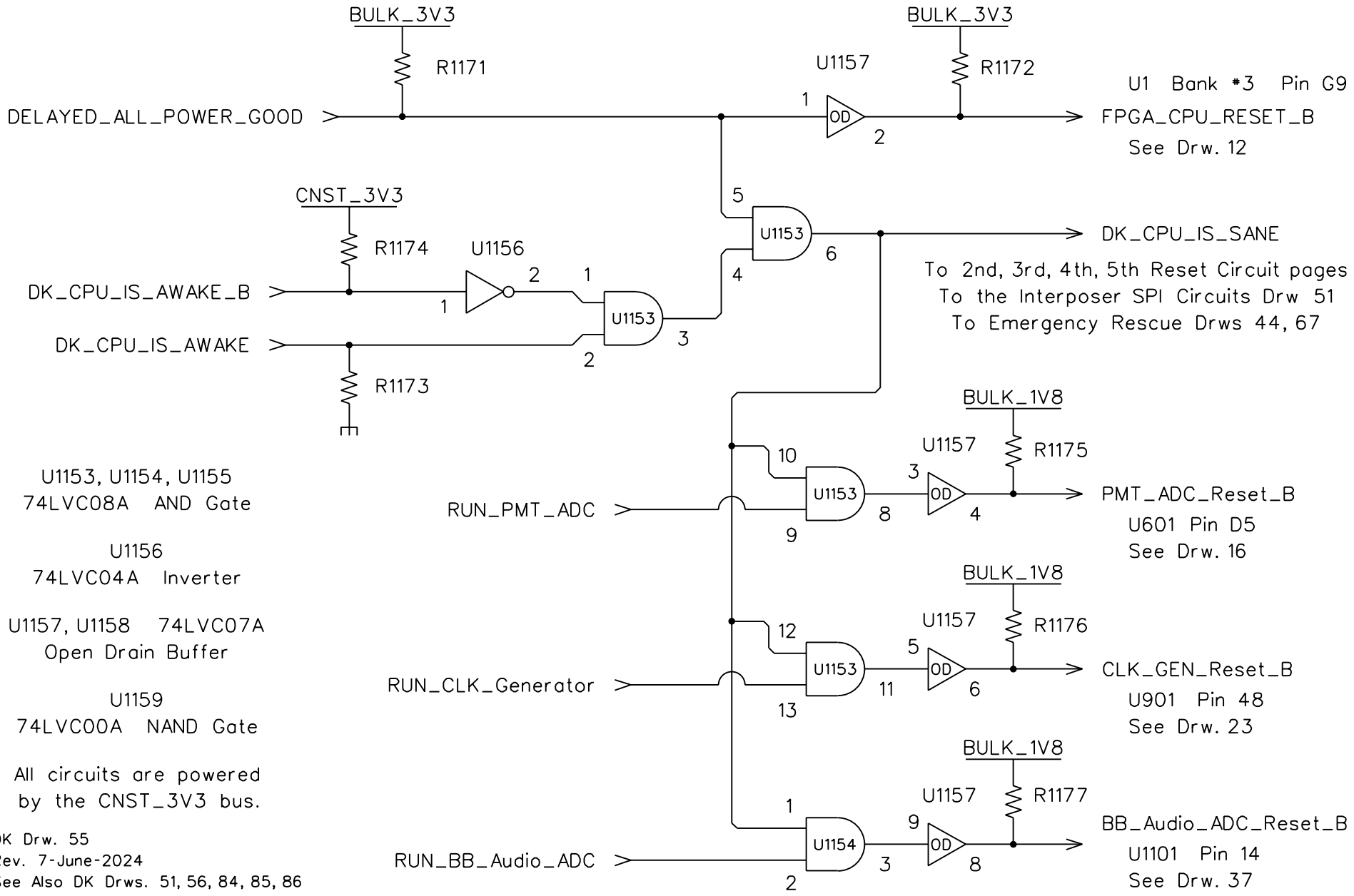
The 220 nFd timing Capacitor implies about 1.2 seconds of delay between BULK_3V3 reaching its threshold and the Assertion of Delayed_All_Power_Good.

The RESET_B pin is an Open Drain output.

The RESET_B pin is Low until the Sense pin is Above Threshold AND the Delay Period has has elapsed.

DK Drw. 5
Rev. 23-Apr-2024

DK Board Reset Circuits Page 1



U1153, U1154, U1155
74LVC08A AND Gate

U1156
74LVC04A Inverter

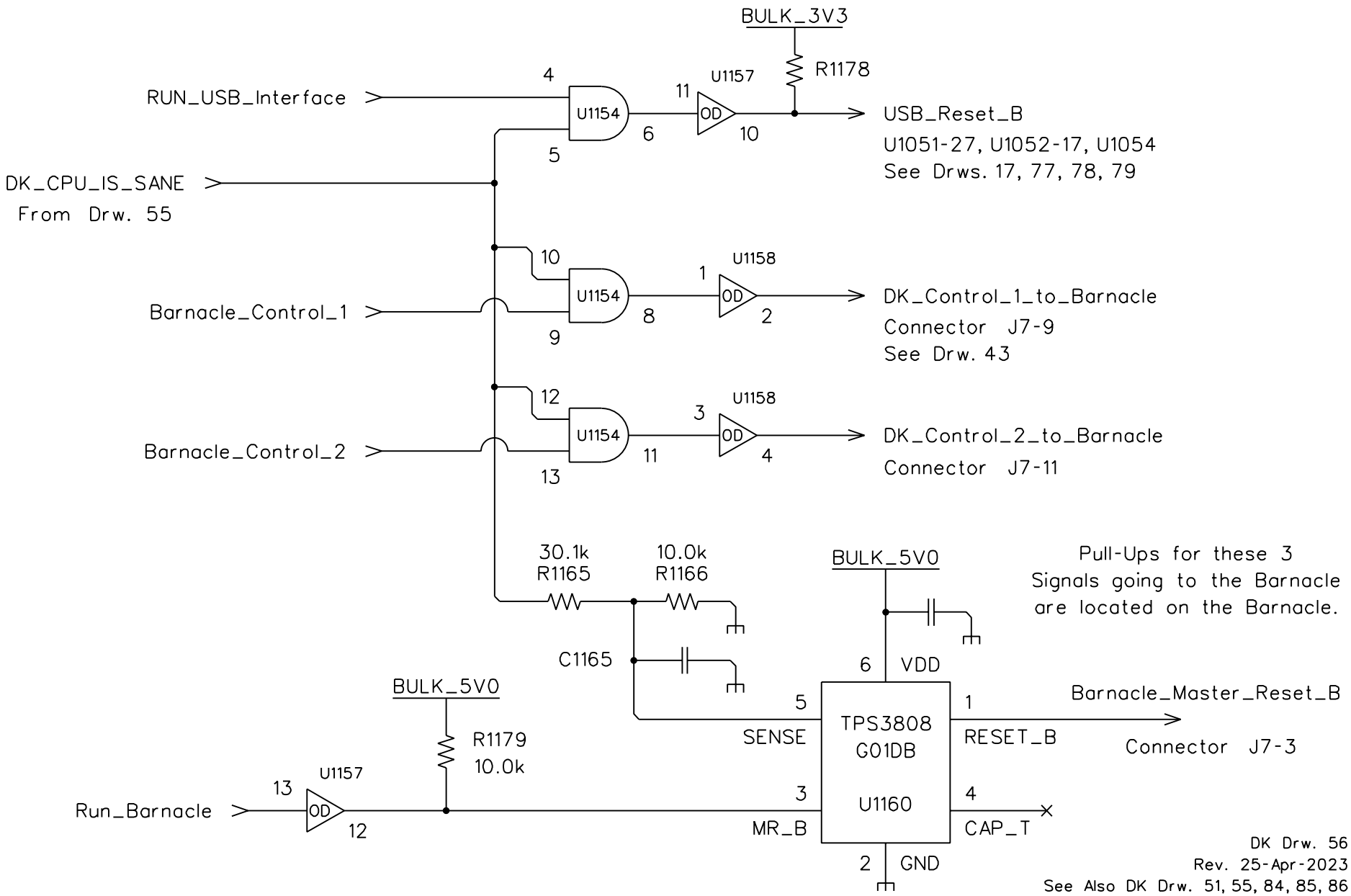
U1157, U1158 74LVC07A
Open Drain Buffer

U1159
74LVC00A NAND Gate

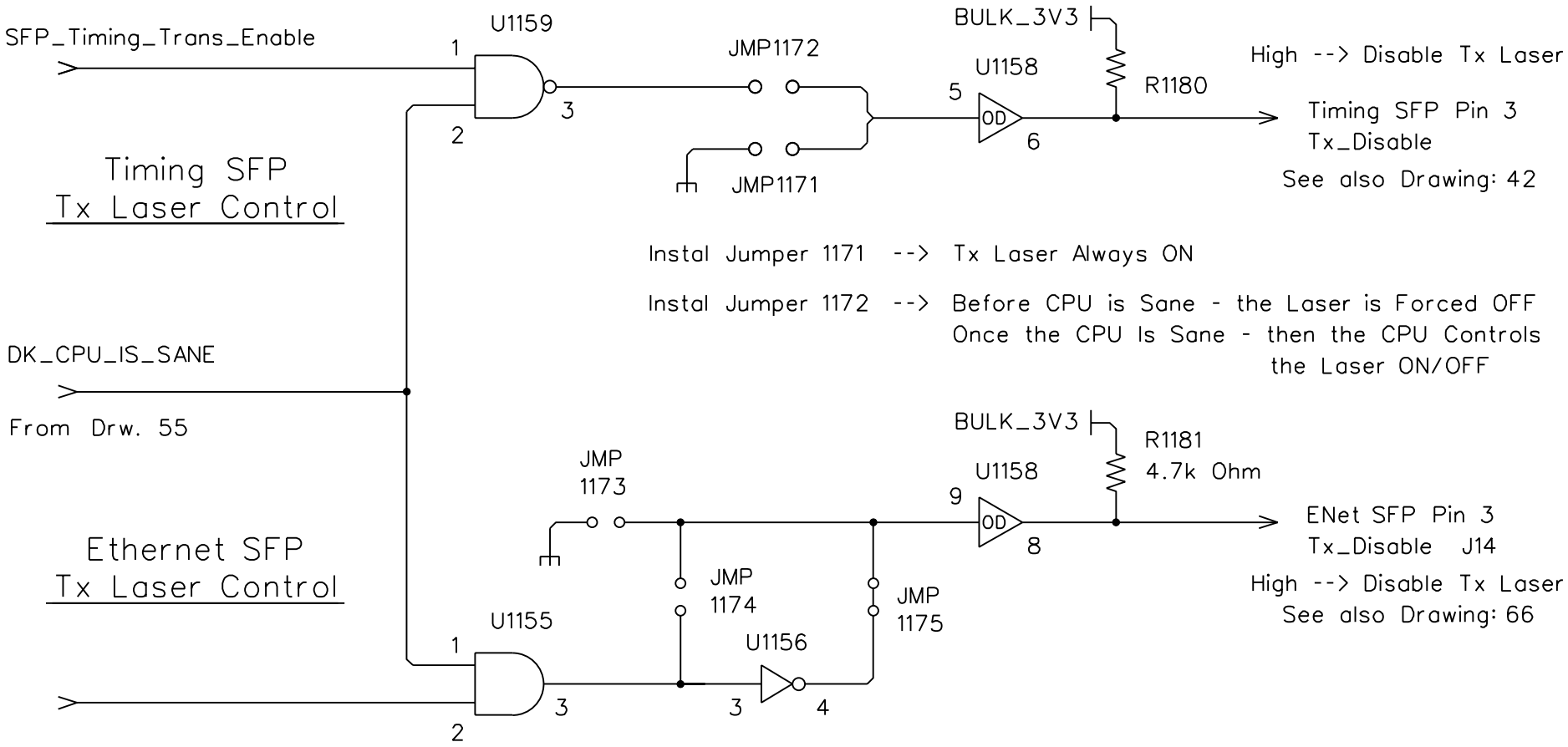
All circuits are powered
by the CNST_3V3 bus.

DK Drw. 55
Rev. 7-June-2024
See Also DK Drws. 51, 56, 84, 85, 86

Reset Circuits Page 2 & Barnacle Control



Timing & ENet SFP Tx Laser Control Page 3

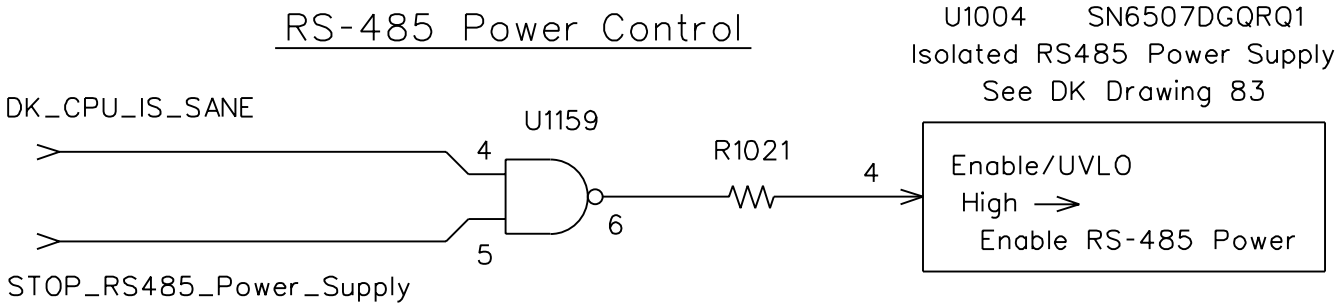


DK Drw. 84
Rev. 25-Apr-2024
See Also DK Drw. 51, 55, 56, 85, 86

These discrete logic circuits are powered by the CNST_3V3 bus.

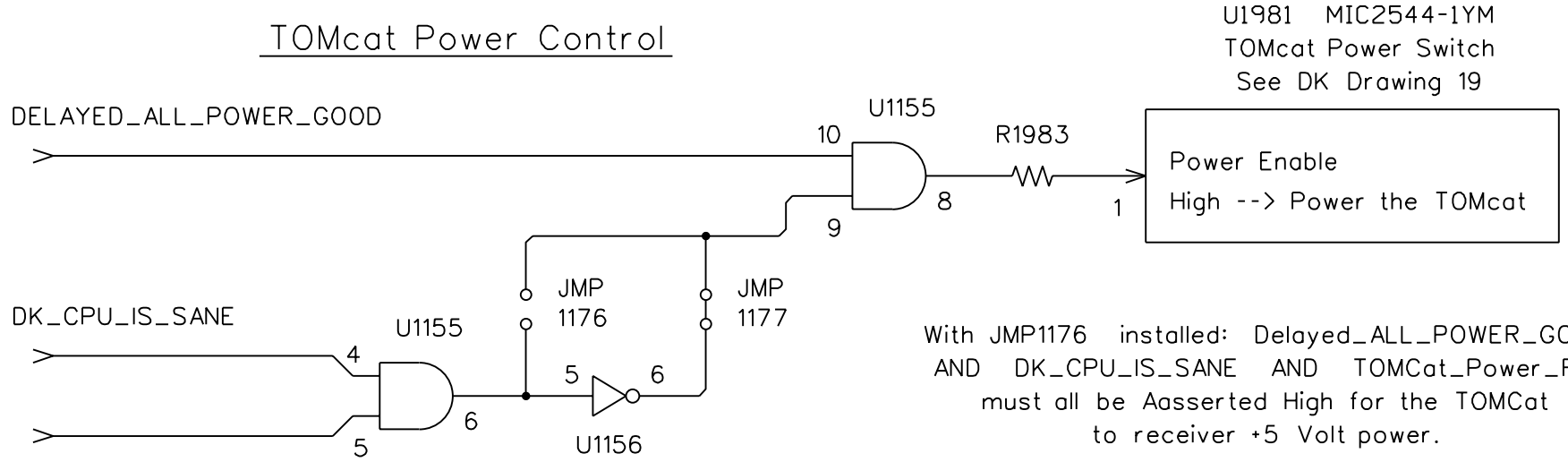
RS-485 & TOMcat Power Control Page 4

RS-485 Power Control



To Turn OFF the Isolated RS-485 Power: DK_CPU_Is_Sane AND Stop_RS485_Power_Supply must both be asserted High.

TOMcat Power Control



JMP1176 --> TOMCat_Power_Run

JMP1177 --> TOMCat_Power_Stop

With JMP1176 installed: Delayed_ALL_POWER_GOOD AND DK_CPU_IS_SANE AND TOMCat_Power_Run must all be Aasserted High for the TOMCat to receiver +5 Volt power.

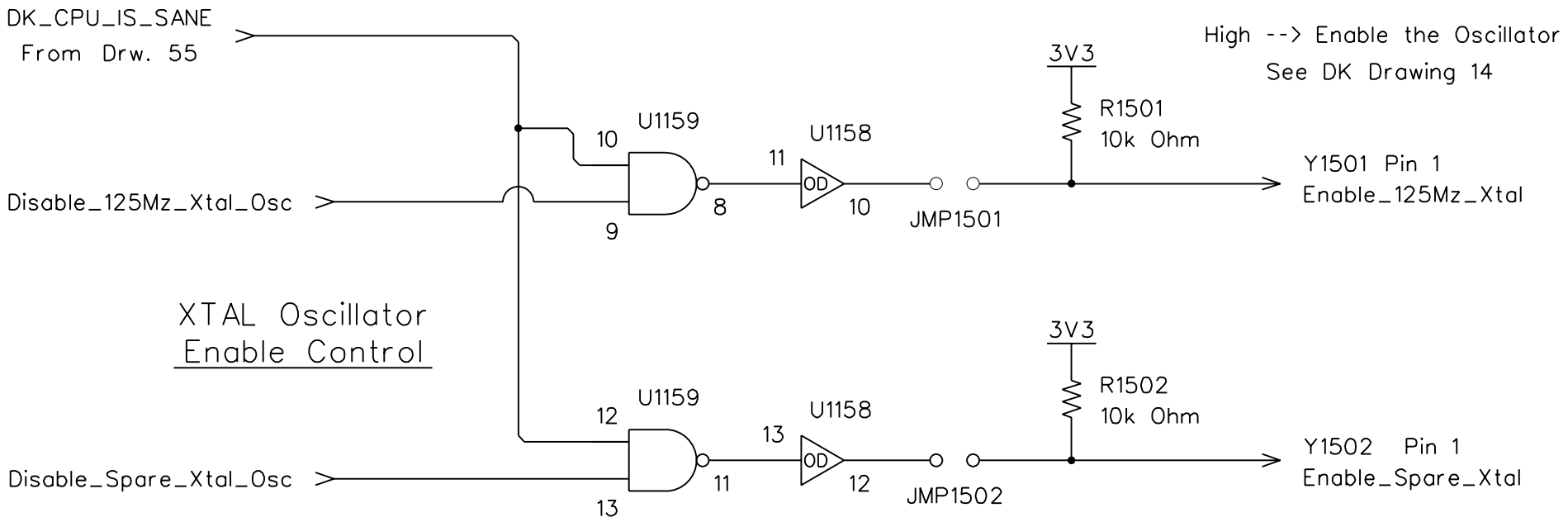
With JMP1177 installed, TOMCat receives +5 Volt power as soon as DELAYED_ALL_POWER_GOOD is asserted. Assertion High of CPU_IS_SANE AND TOMCat_Power_Stop is required to Turn Off the TOMCat power.

DK Drw. 85
See Also DK Drw. 51, 55, 56, 84, 86

These discrete logic circuits are powered by the CNST_3V3 bus.

Rev. 25-Apr-2024

Crystal Oscillator Enable Control Page 5



HI Active Disable signals
from the DK's CPU GPIO

Instal the Jumper to Allow
Disabling of the Oscillator.

Jumper Not Installed -->
Oscillator Always Runs.

Spare Gates in the Startup Supervisor and Reset/Enable Section

1 Spare AND in U1155

Notes: 2 Inverters in U1156 are used by the ER circuits in Drw. 44

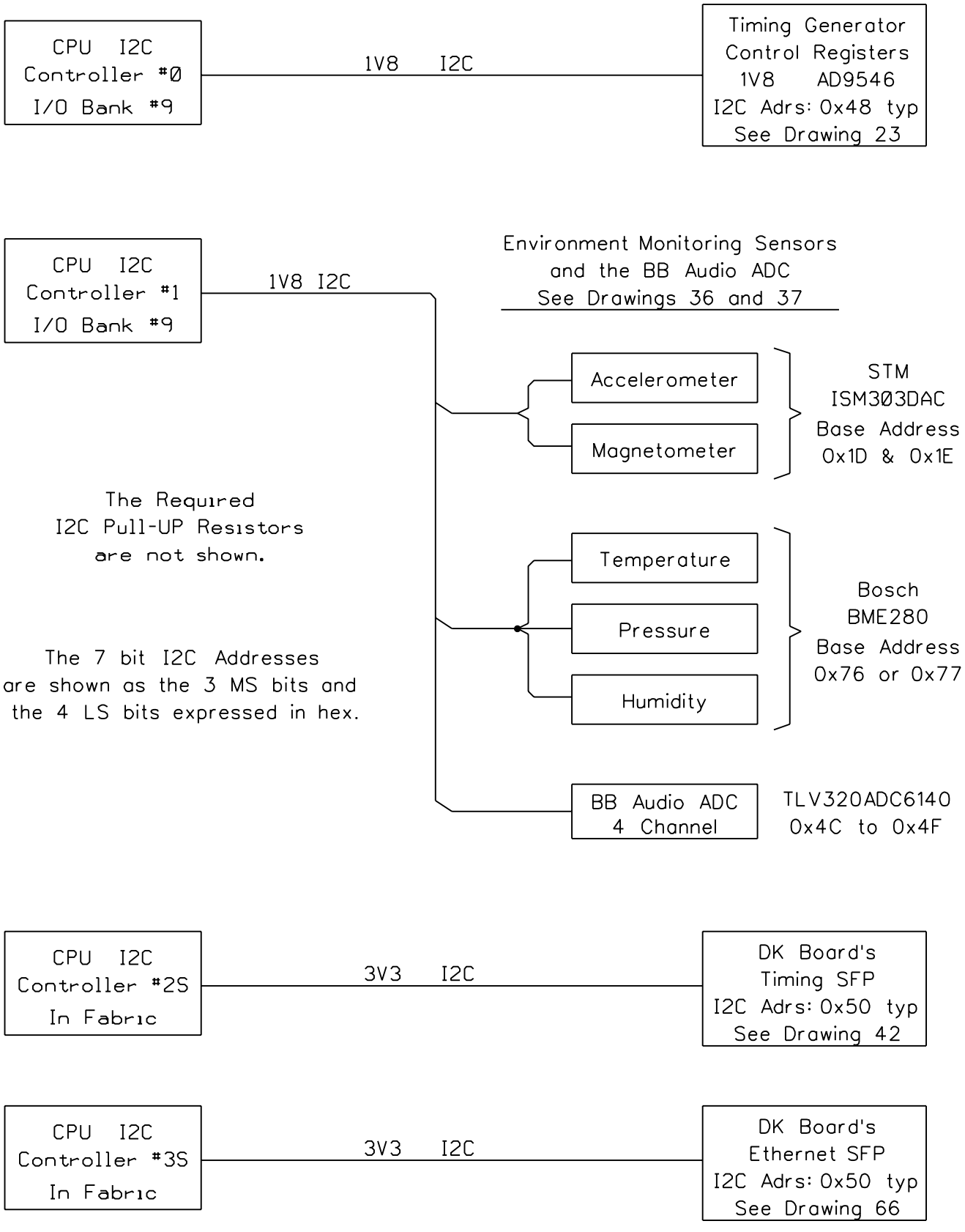
1 Inverter in U1156 is used by Interposer SPI circuits in Drw. 51

This discrete logic is powered by CNST_3V3.

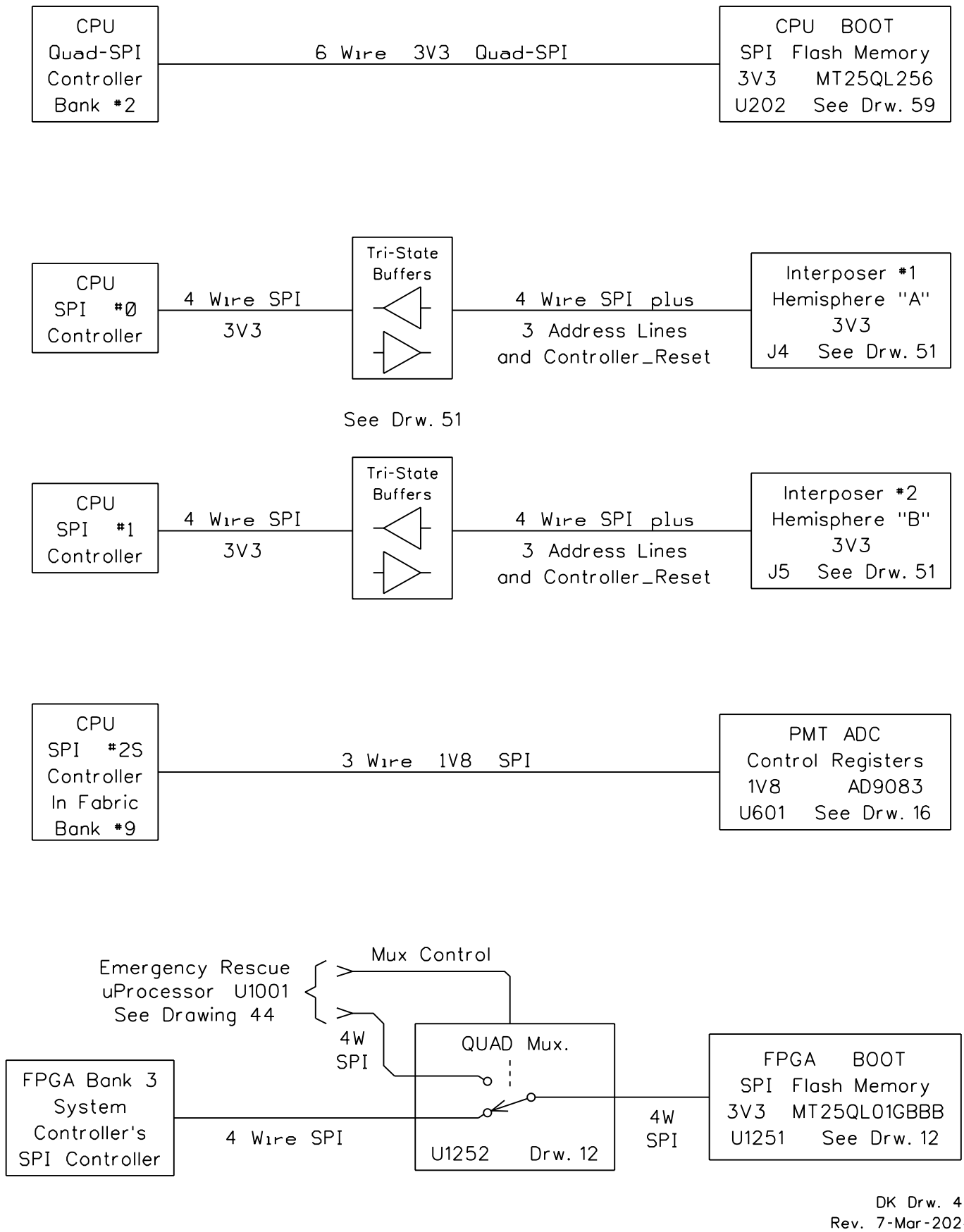
Rev. 14-May-2024

See Also DK Drw. 51, 55, 56, 84, 85

DK Board's I2C Buses

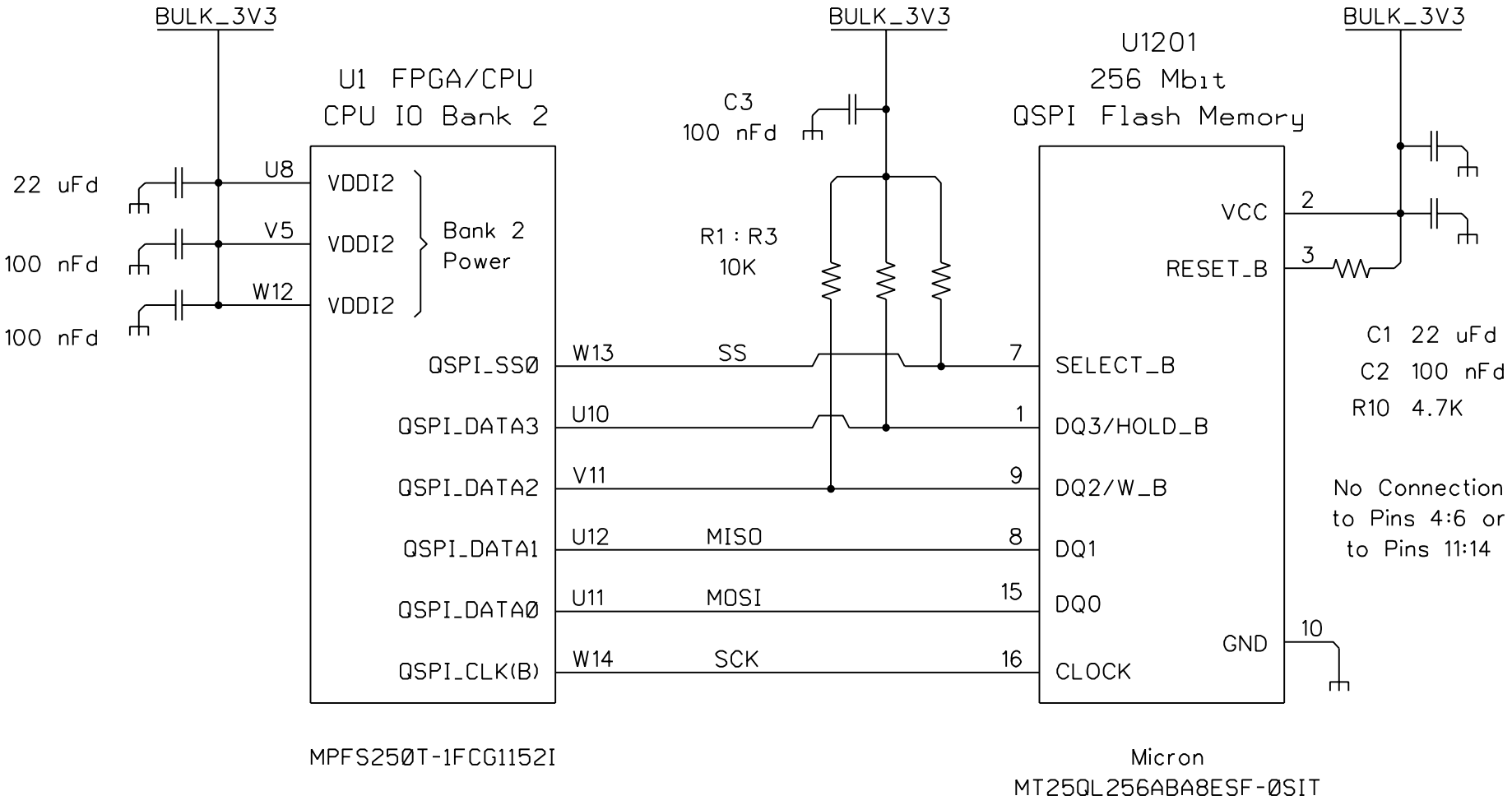


DK Board's SPI Buses



DK Drw. 48
Rev. 7-Mar-2024

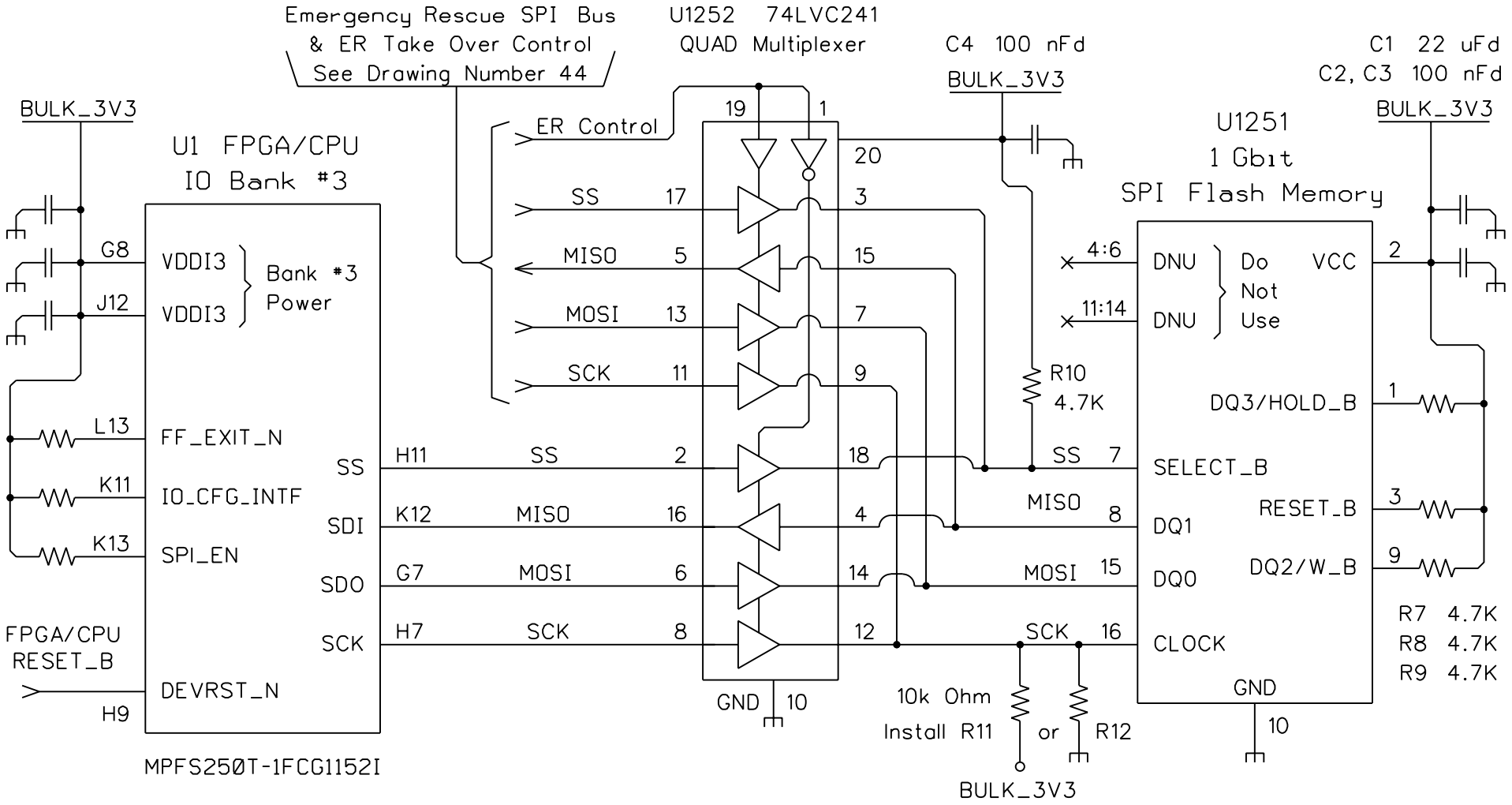
CPU QSPI Port & CPU Boot Memory



The U1 pin numbers for the QSPI Controller represent routing it out via Bank #2.

This section's actual reference designators start at 1201.

IO Bank #3 FPGA Boot Memory & Multiplexer



Bank #3 Pull-Ups

R1351 4.7K
R1352 4.7K
R1353 4.7K

ER Control: LOW --> Normal Boot, HI --> Emergency Rescue

Normally the FPGA/CPU System Controller is the SPI Master.

FF_EXIT_N is a Reserved Input to the System Controller.

IO_CFG_INTF set to 0 for SPI Slave, 1 for SPI Master.

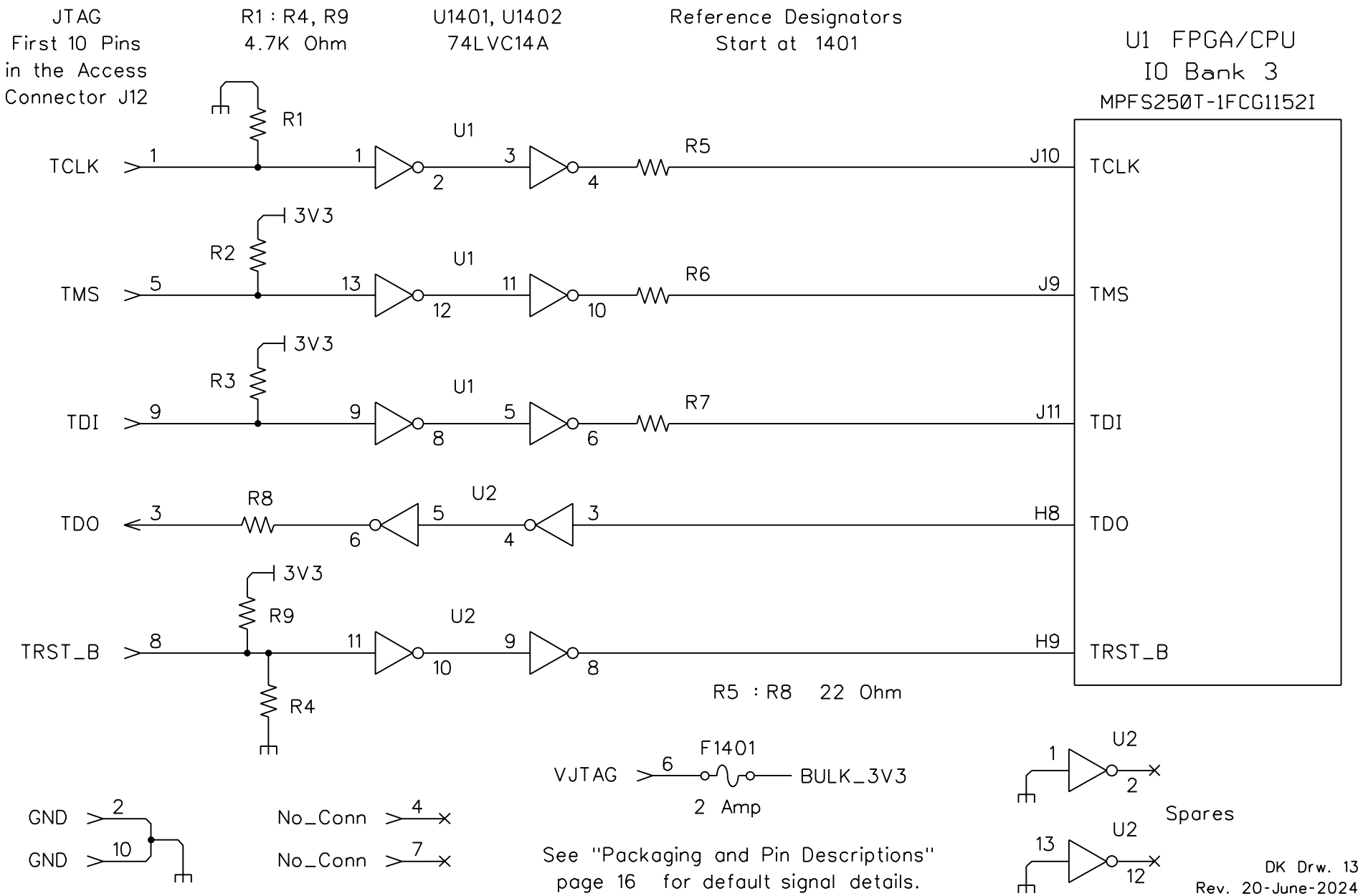
SPI_EN set to 0 for SPI tri-stated, 1 for SPI Enabled.

Reference Designators
Start at 1251

DK Drw. 12

Rev. 19-June-2024

FPGA Bank 3 JTAG Connection & Buffers



UARTs - DK's FPGA/CPU and ER's LPC845

DK's FPGA/CPU UARTs

MMUART_0 <--> Header 3V3

MMUART_1 <--> Emergency Rescue 3V3

MMUART_2 <--> Barnacle Connector 3V3

MMUART_3 <--> Interposer #1 1V8

MMUART_4 <--> Interposer #2 1V8

ER's LPC845 UARTs

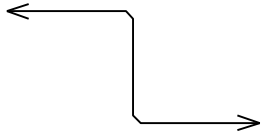
UART_0 <--> RS-485 Transceiver 3V3

UART_1 <--> Header 3V3

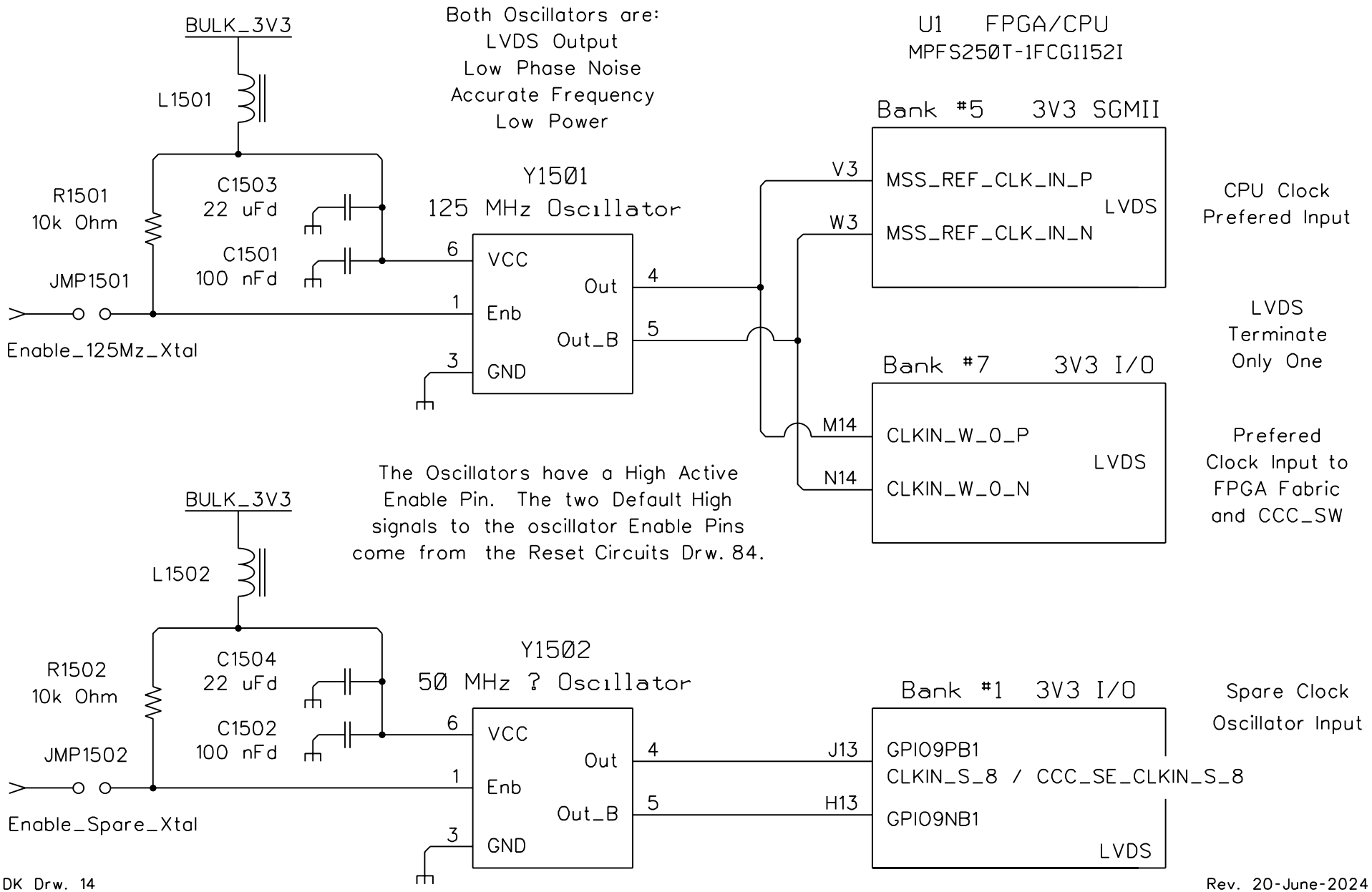
UART_2 <--> DK's FPGA/CPU 3V3

UART_3 <--> TOMcat via 3V3 <-> LVDS

UART_4 <--> Not Used 3V3



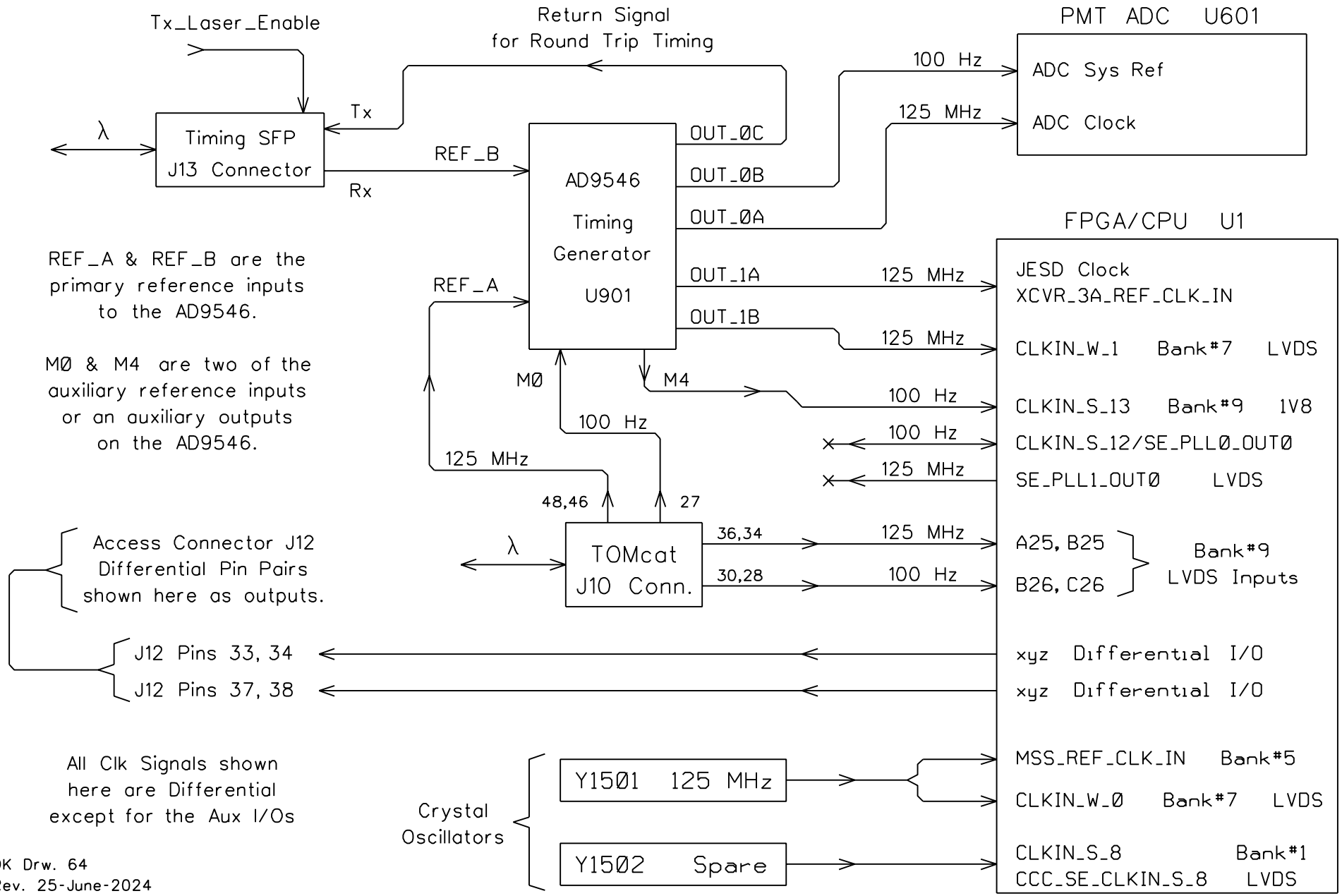
Quartz Oscillator Clocks on the DK Board



DK Drw. 14

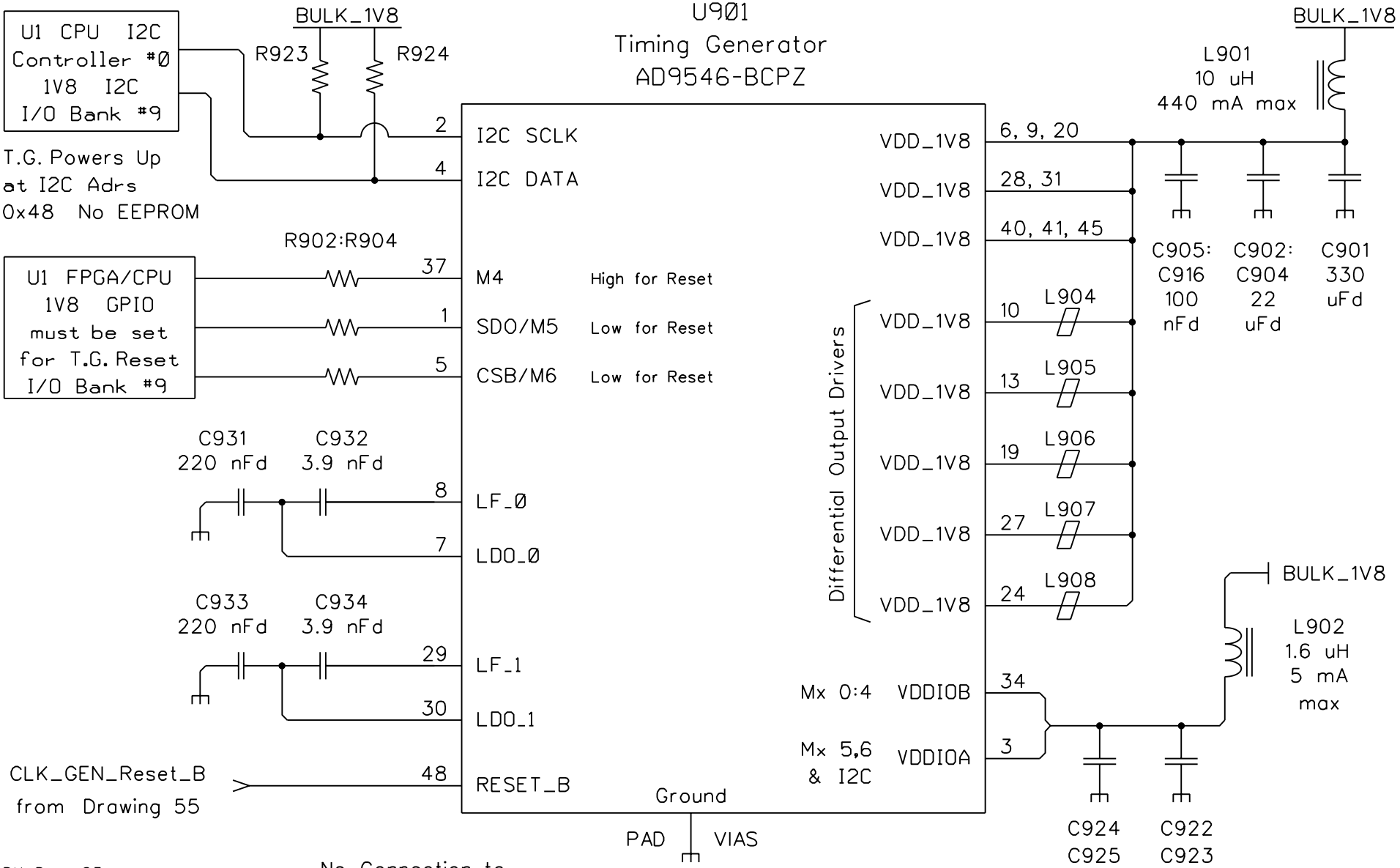
Rev. 20-June-2024

Clocks Type Signals on the DK Board

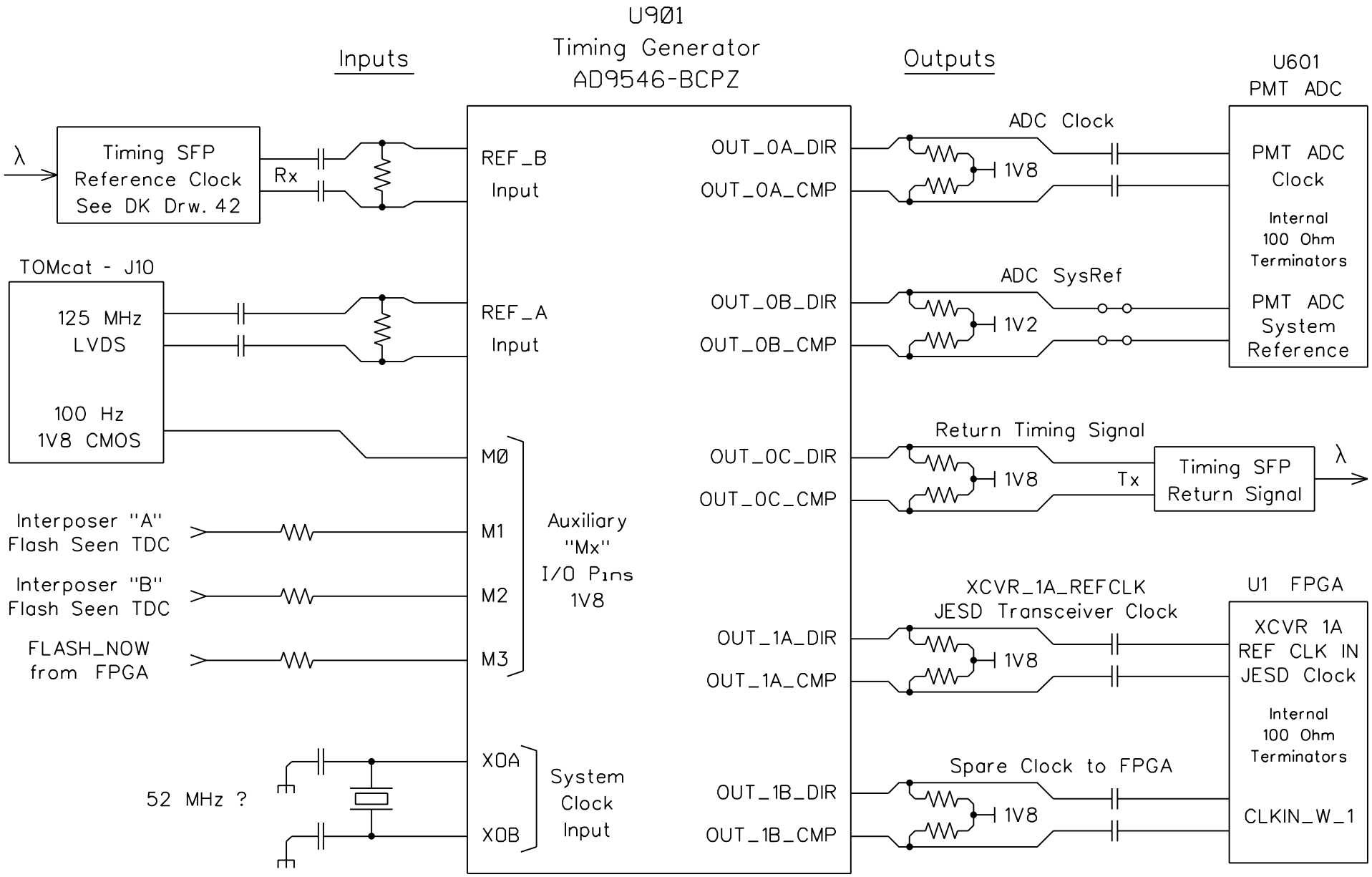


DK Drw. 64
Rev. 25-June-2024

Timing Generator - Control, Power, & Gnd



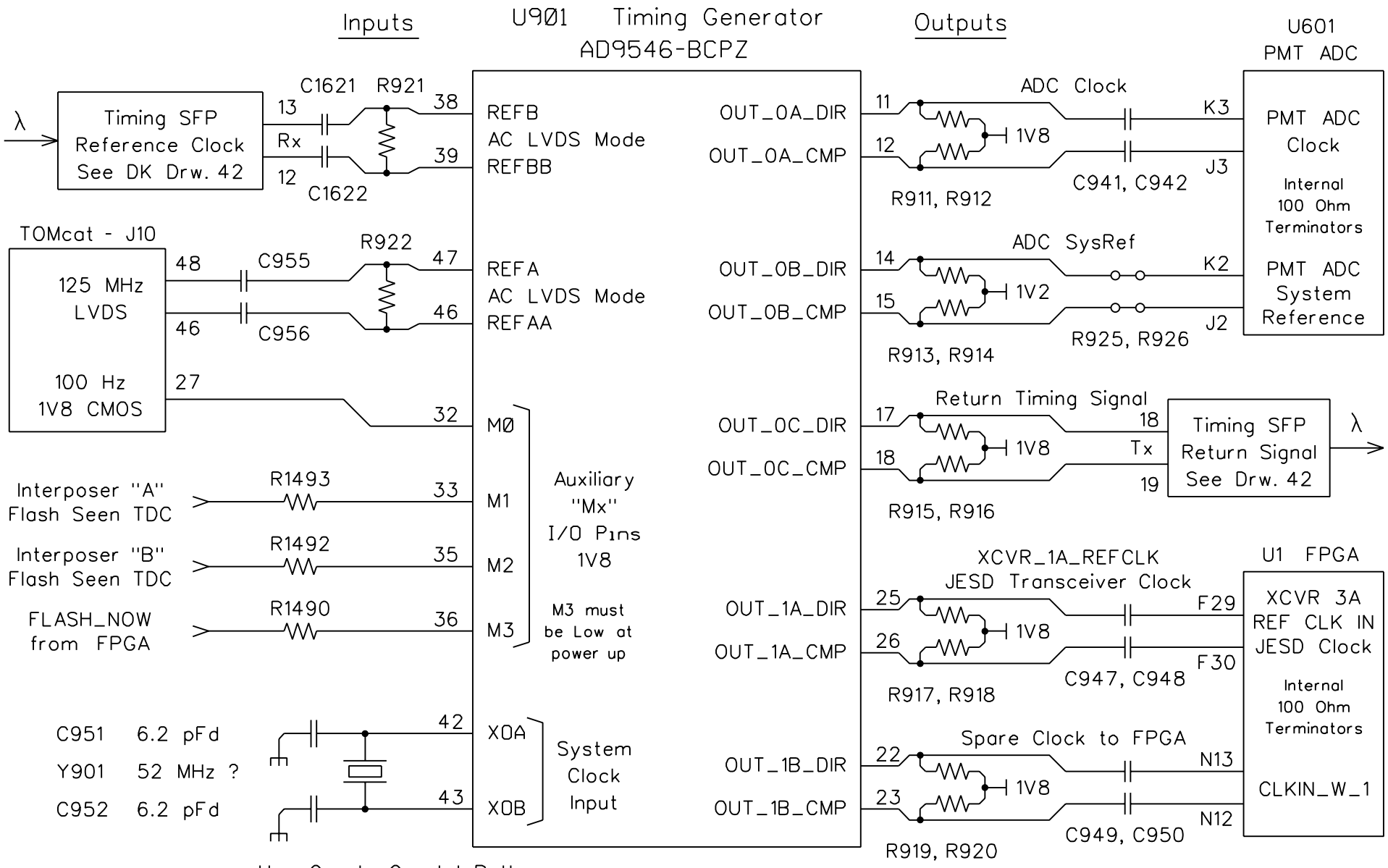
Timing Generator - Input/Output Signals - Simplified



DK Drw. 70
aka Drw. 50 Simplified

Rev. 17-June-2024

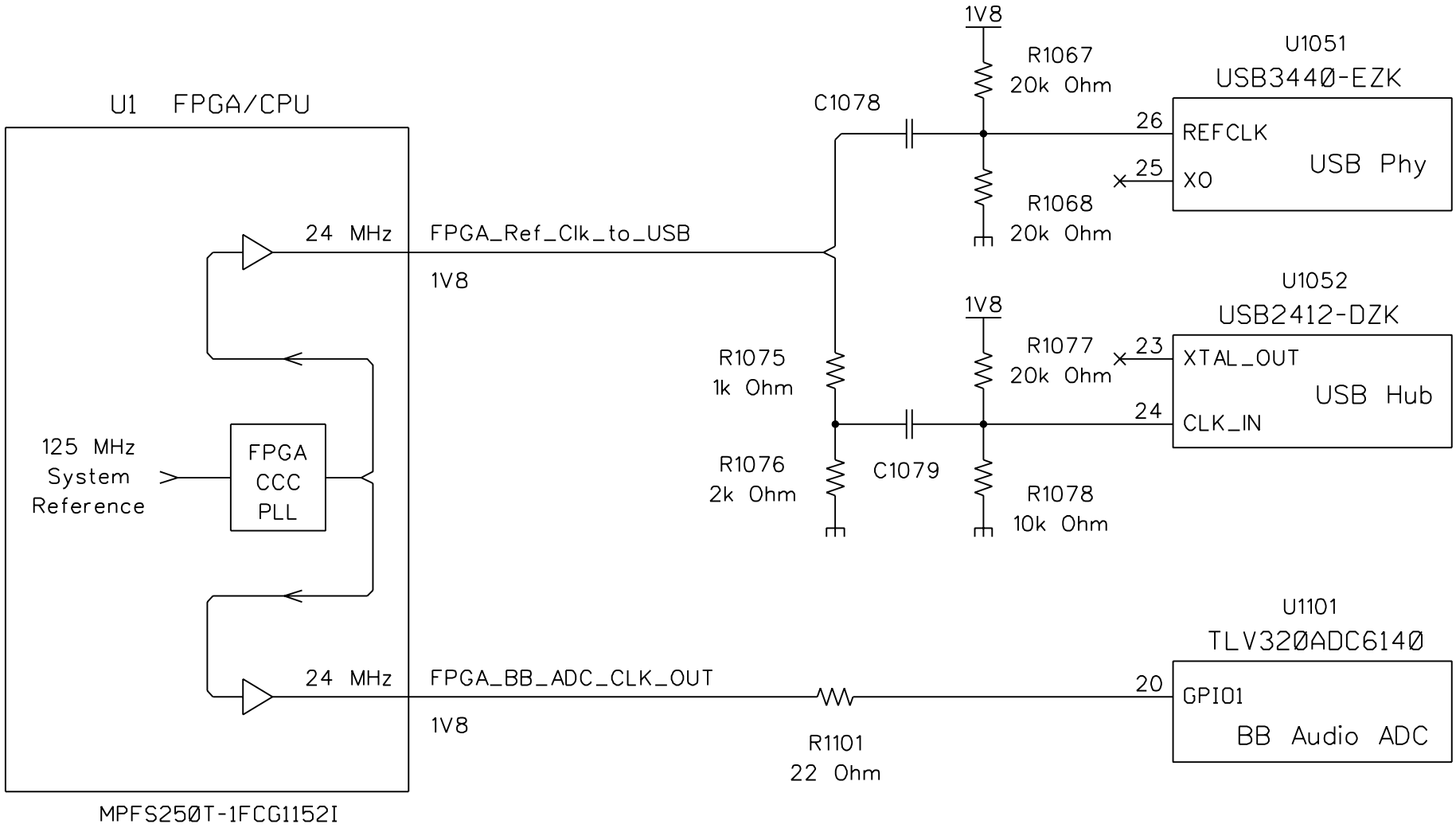
Timing Generator - Timing Signals Input/Output



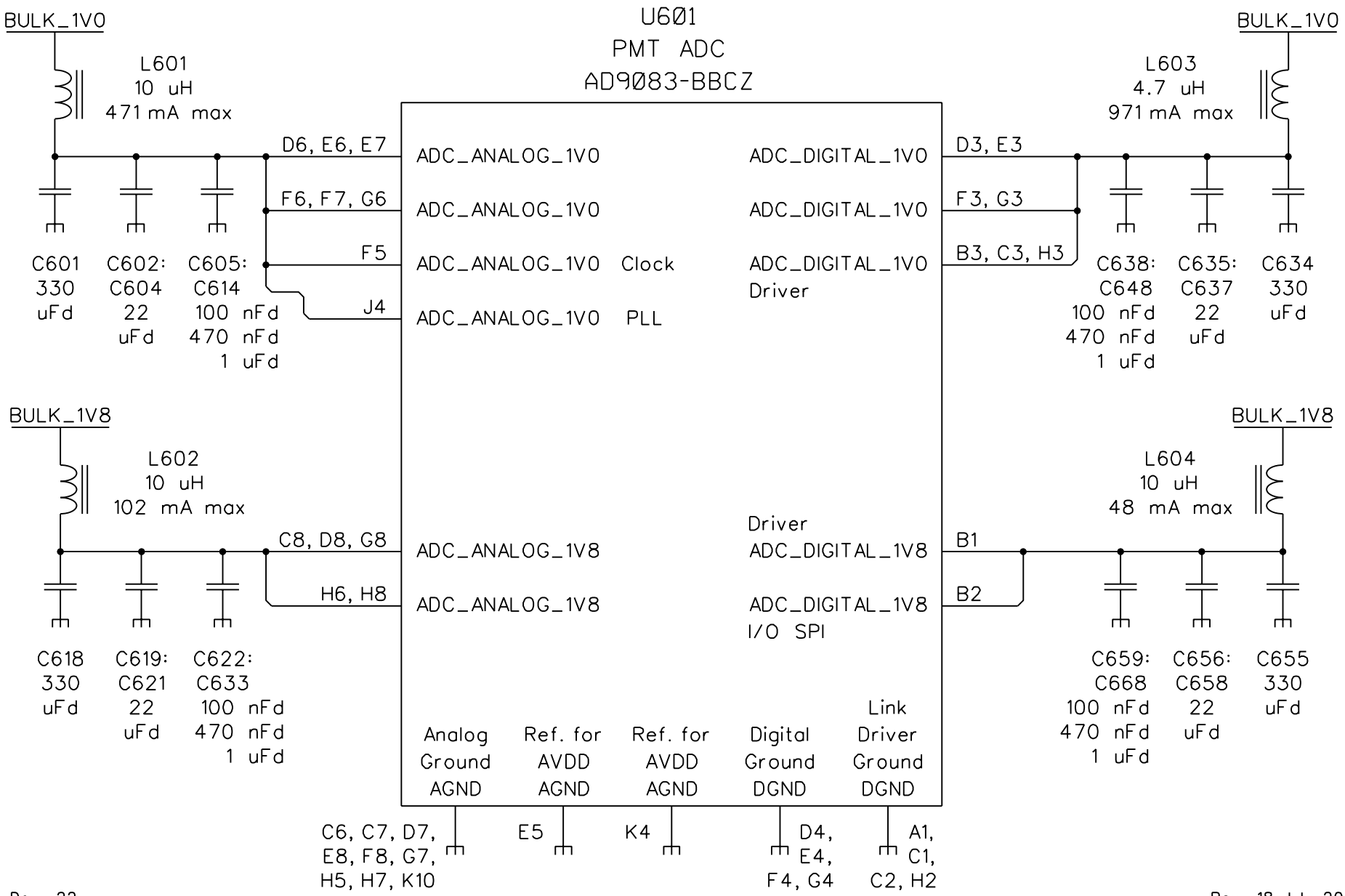
Rev. 17-June-2024

DK Drw. 50

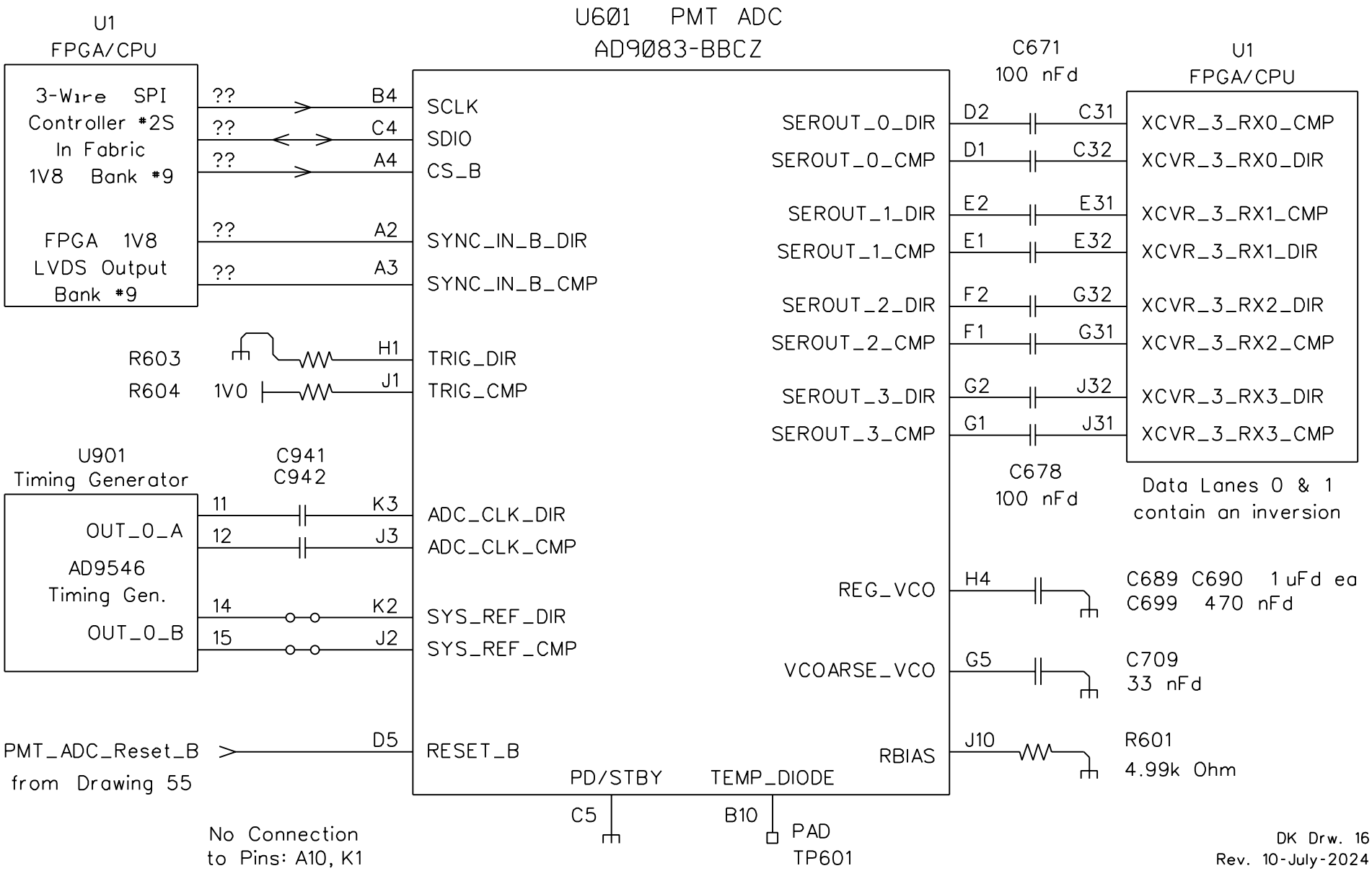
FPGA/CPU Clocks to External Consumers



PMT ADC - Power and Ground

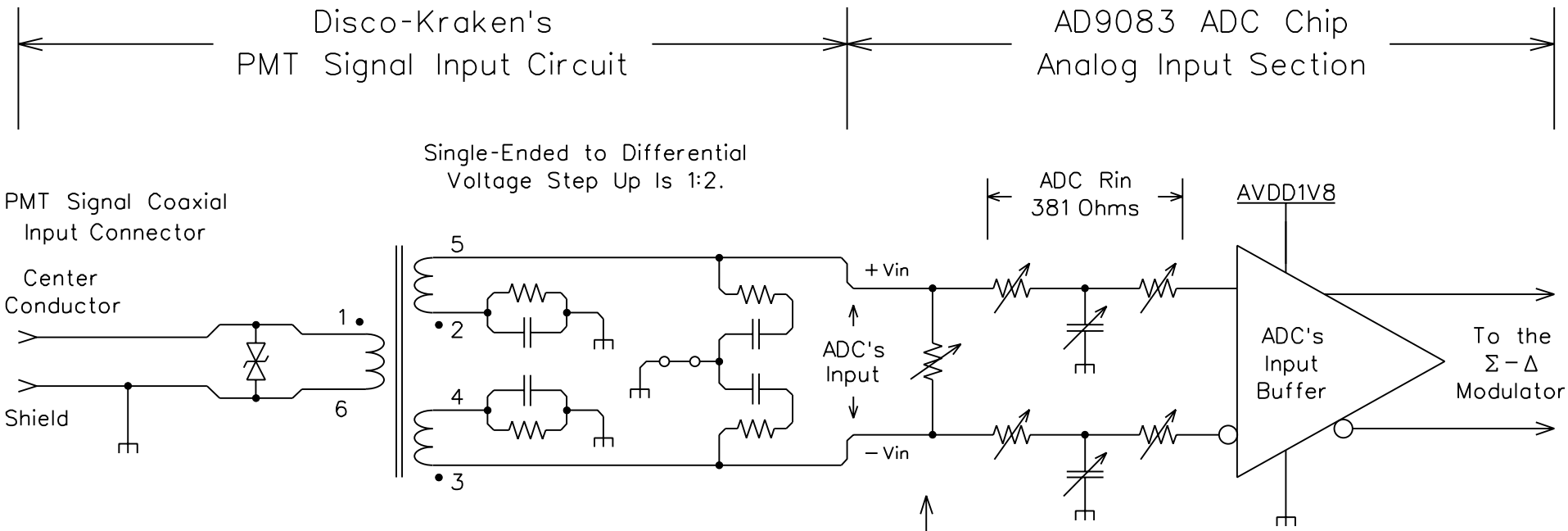


PMT ADC - Clocks, Control, & Output Links



DK Drw. 16
Rev. 10-July-2024

PMT to ADC Analog Input Circuit



DC Bias Set to 80% of Negative Full Scale.

Overall Parallel AC Termination Is 200 Ohms.

See the
AD9083 Datasheet
Page 5 note 6
Pages: 30 and 31

For the ADC's Input to Swing from Its Static 80% of Neg. FS to 100% of Pos. FS Requires a 0.81 V Pulse Across the Primary of the Input Transformer aka 16.2 mA through 50 Ohms.

The Capacitor Symbol Represents Parallel 1 uFd and 47 nFd Ceramic Capacitors

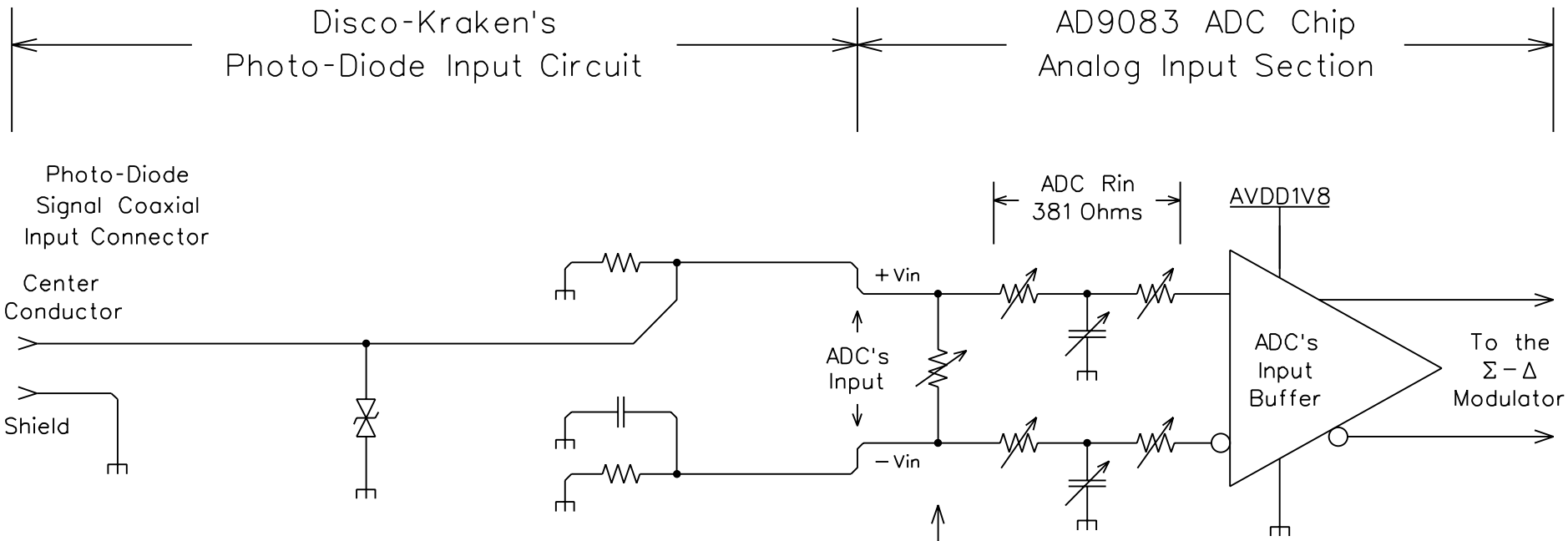
The Recommended Common Mode at the ADC's Input is 0.7 Volts

The ADC's Nominal Vmax is 1.8 Vpp
---> Pos. Full Scale Is:
+Vin 1.15V −Vin 0.25V
---> Neg. Full Scale Is:
+Vin 0.25V −Vin 1.15V

The ADC Actively Holds the Inputs of Its Input Buffer at a Common Mode of 1.1 Volts

DK Drw. 10
Rev. 7-Mar-2024

Photo-Diode to ADC Analog Input Circuit



DC Bias Set to 80% of Negative Full Scale.

Overall Parallel AC Termination Is 200 Ohms.

See the AD9083 Datasheet Pages: 5 note 6, 30, and 31.

For the ADC's Input to Swing from Its Static 80% of Neg. FS to 100% of Pos. FS Requires a 1.62 V Positive Input Pulse. A 1.62 V Pulse across the 200 Ohm load requires 8.1 mA.

The Capacitor Symbol Represents Parallel 10 uFd and 47 nFd Ceramic Capacitors

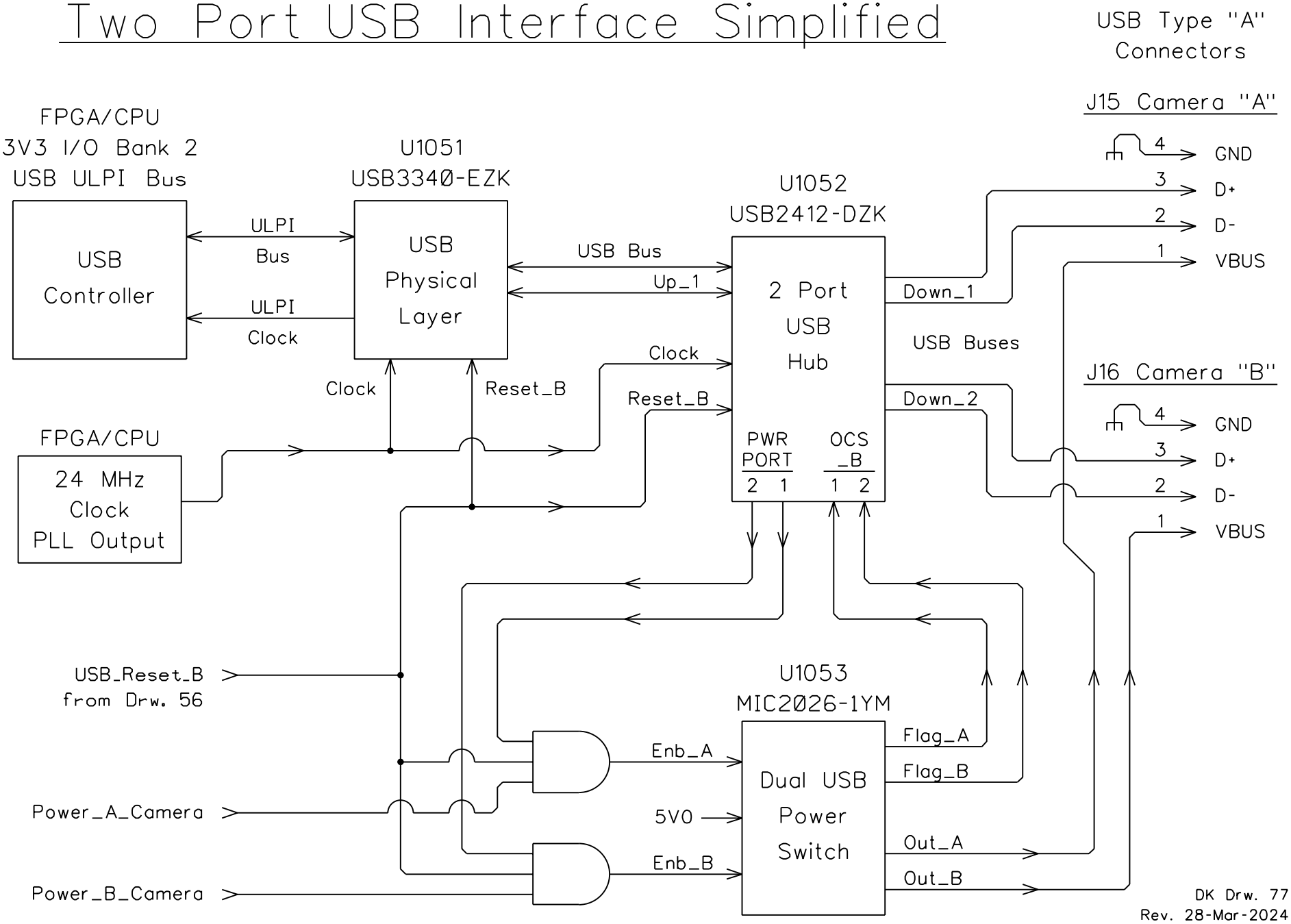
The Recommended Common Mode at the ADC's Input is 0.7 Volts

The ADC's Nominal Vmax is 1.8 Vpp
---> Pos. Full Scale Is:
+Vin 1.15V −Vin 0.25V
---> Neg. Full Scale Is:
+Vin 0.25V −Vin 1.15V

The ADC Actively Holds the Inputs of Its Input Buffer at a Common Mode of 1.1 Volts

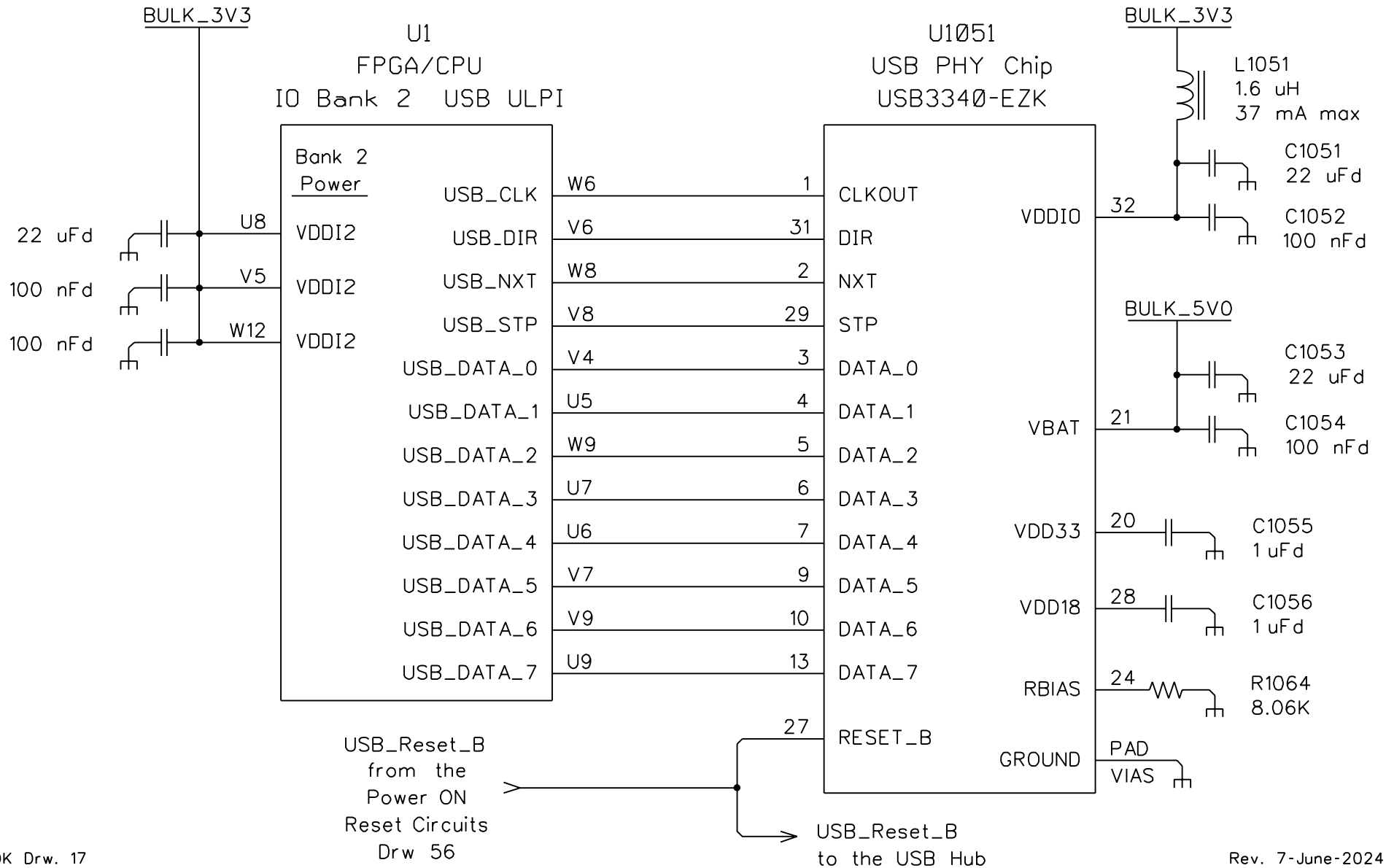
DK Drw. 62
Rev. 7-Mar-2023

Two Port USB Interface Simplified

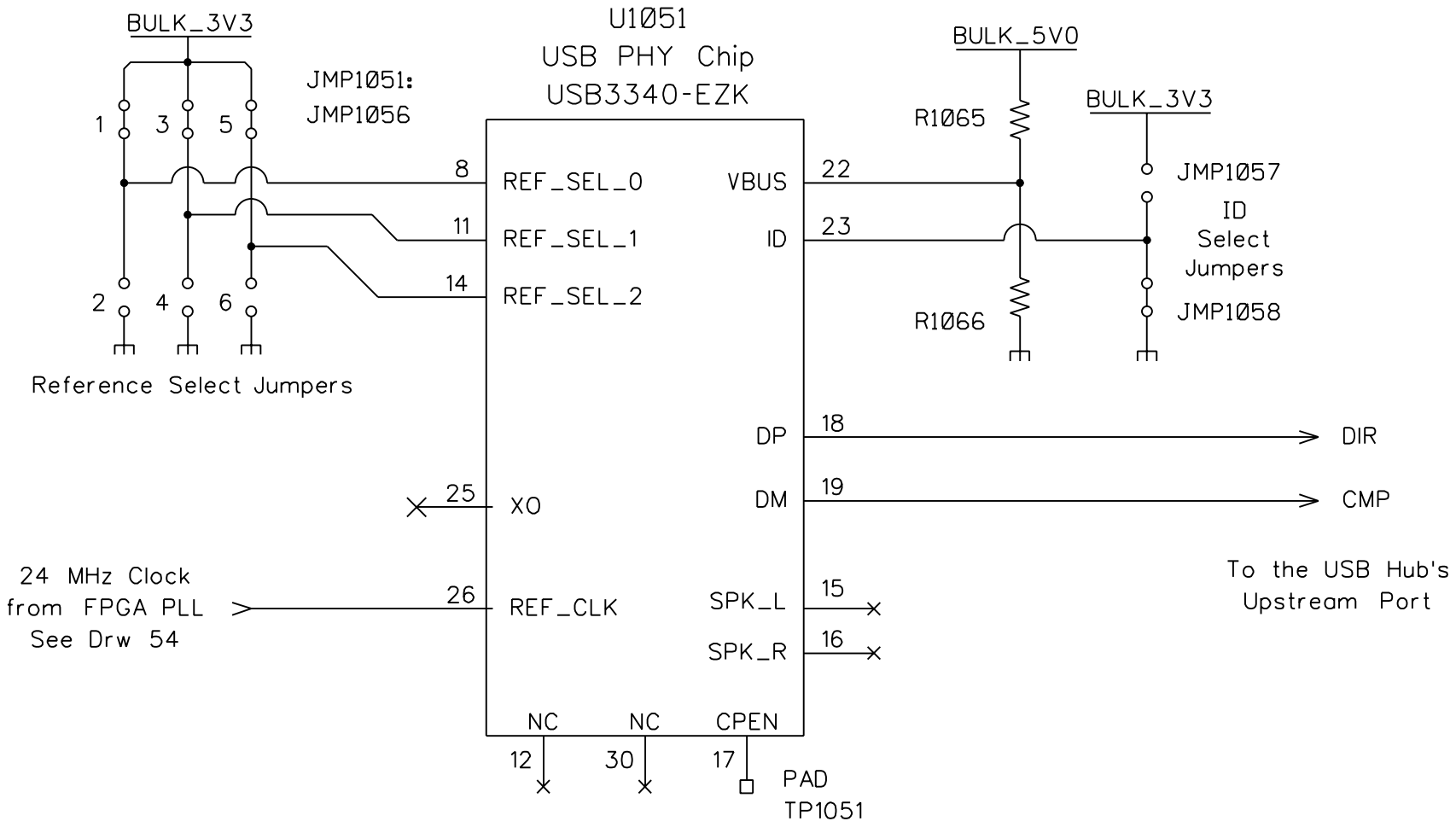


DK Drw. 77
Rev. 28-Mar-2024

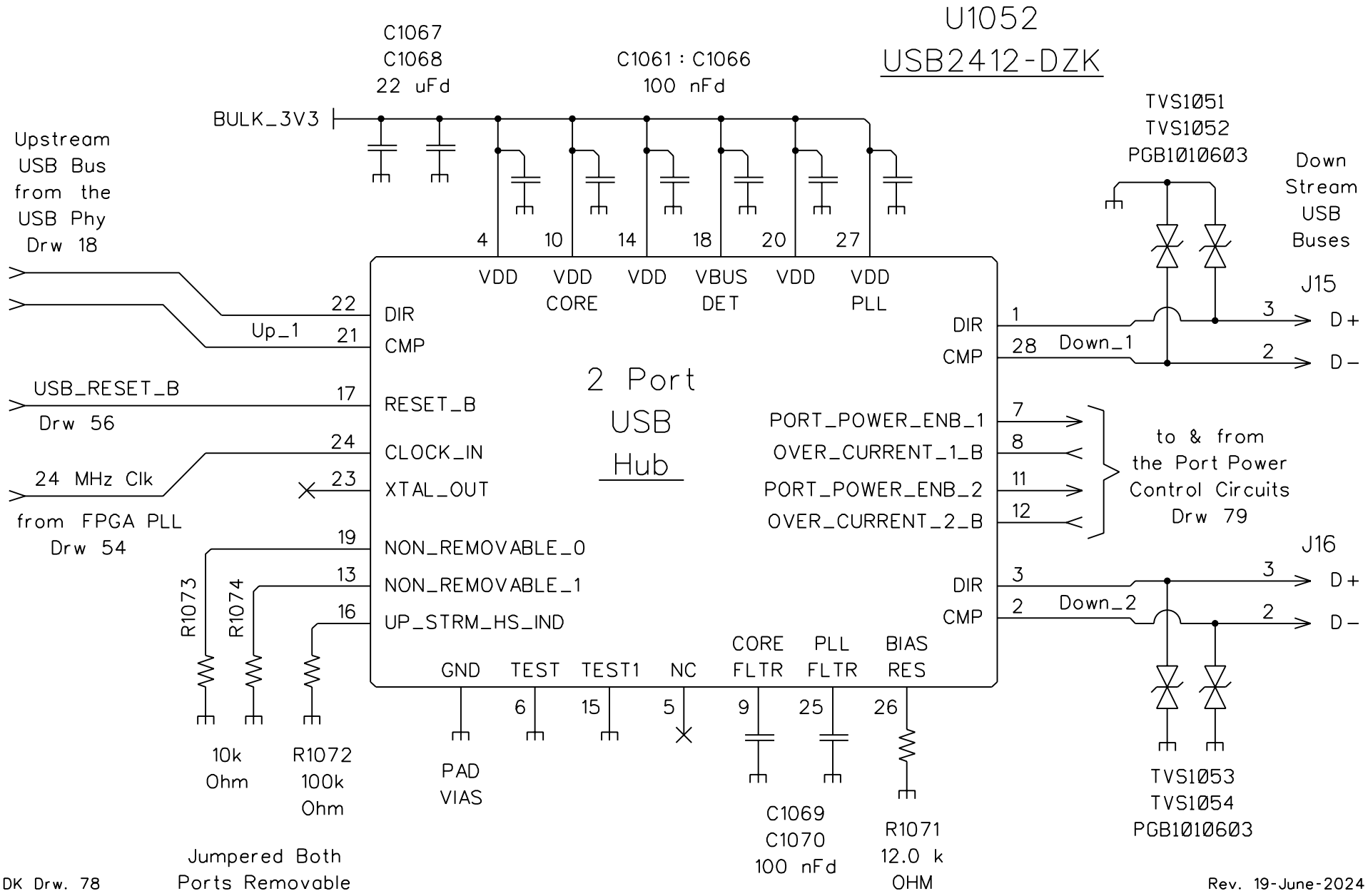
IO Bank 2 USB ULPI Bus to USB PHY



USB PHY to USB Hub



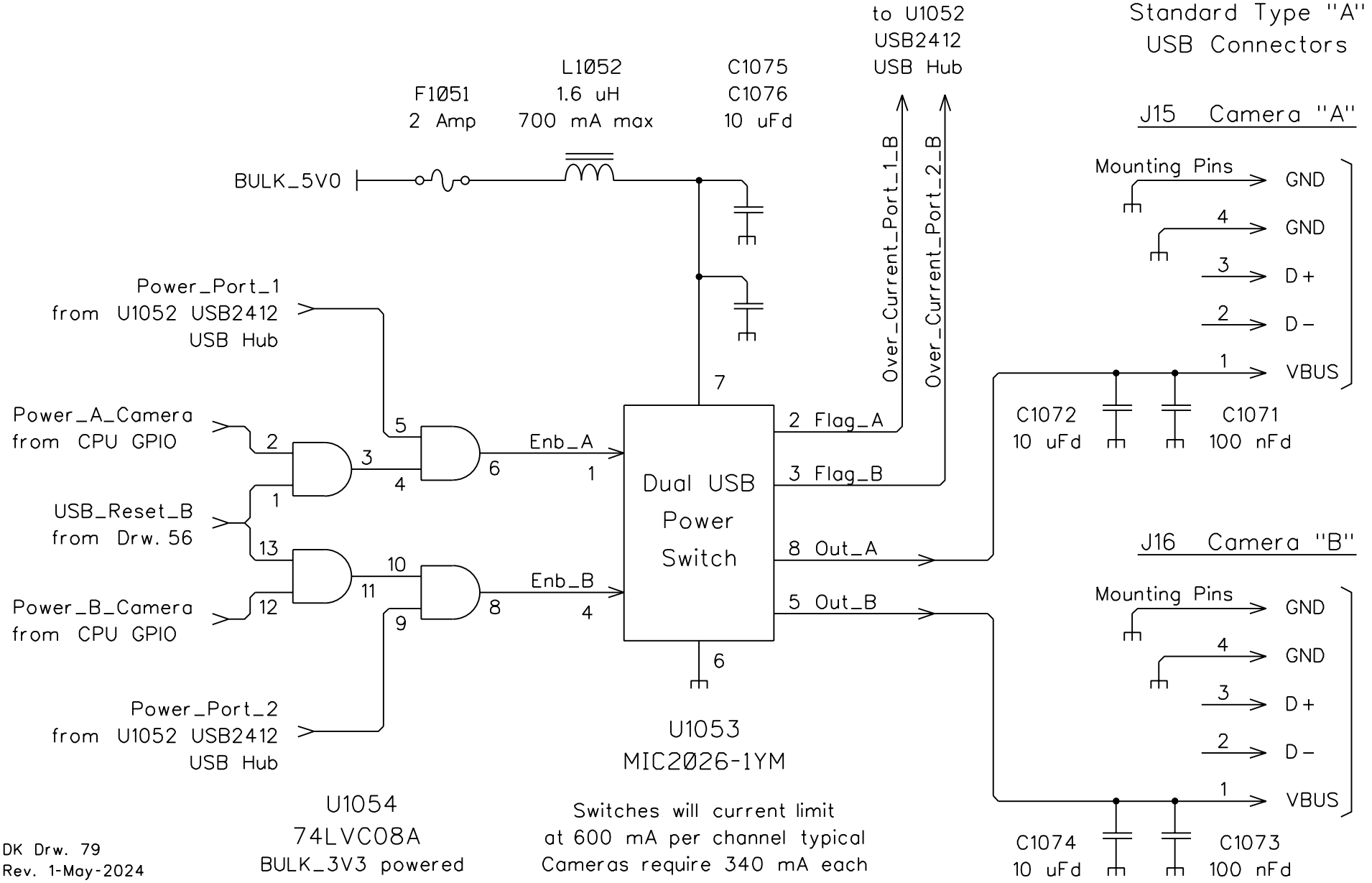
USB Hub 2 Port Controller



DK Drw. 78

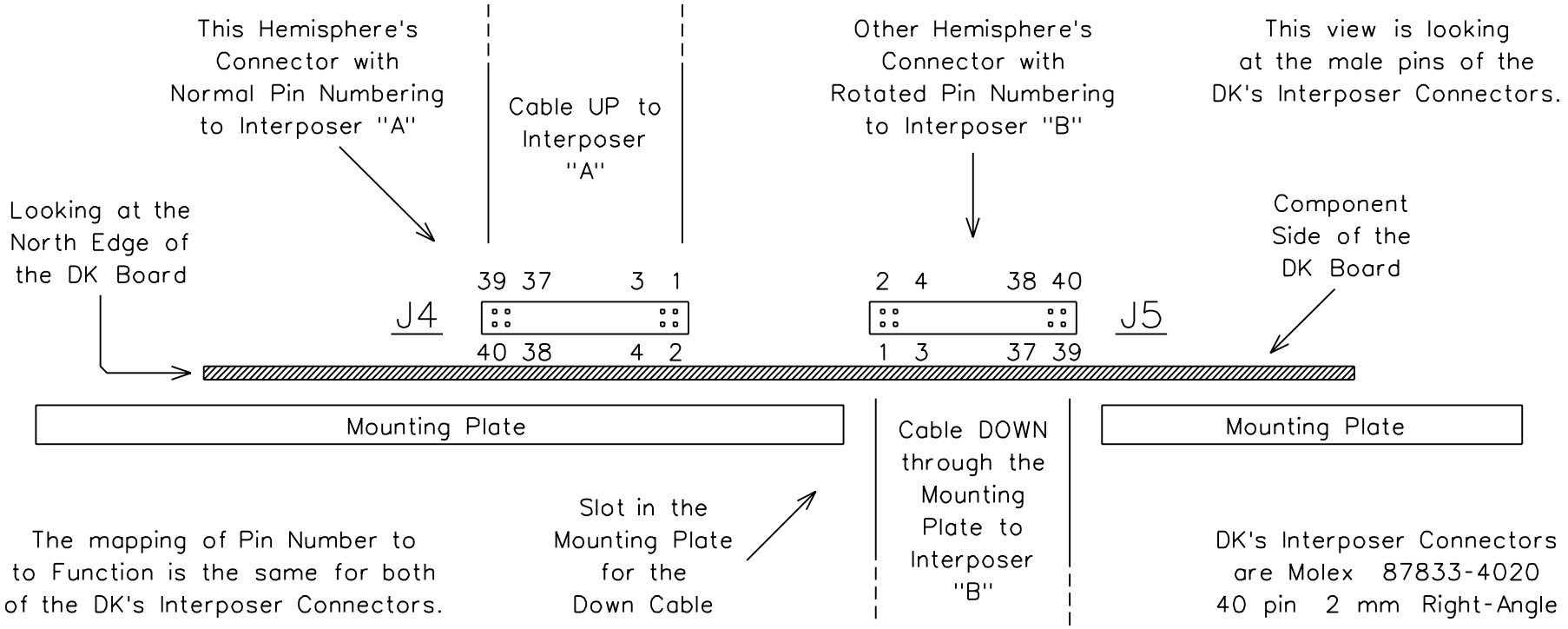
Rev. 19-June-2024

USB Hub 2 Port Power Control



DK Drw. 79
Rev. 1-May-2024

DK's Interposer Connectors & Pin Layout



Pin Num	Function	Pin Num	Function
1	1V8	2	1V8
3	3V3	4	3V3
5	Gnd	6	Gnd
7	Flash_Pulse_P	8	Flash_Pulse_N
9	Gnd	10	Gnd
11	Piezo_P	12	Piezo_N
13	Gnd	14	Gnd
15	FLASH_TDC	16	Gnd
17	Gnd	18	SPI_CLK
19	Ctrl_Reset	20	SPI_MISO

DK Drw. 69
Rev. 26-July-2024

Pin Num	Function	Pin Num	Function
21	Gnd	22	SPI_MOSI
23	A0	24	SPI_CS
25	Gnd	26	Gnd
27	A2	28	A1
29	Gnd	30	Gnd
31	uBase_UART_Tx	32	uBase_UART_Rx
33	Muon_S1	34	Gnd
35	Muon_S2	36	Muon_S3
37	Muon_S4	38	Gnd
39	5V0	40	5V0

Interposer Connector Locks

The connector is a
Molex: 87833-4020

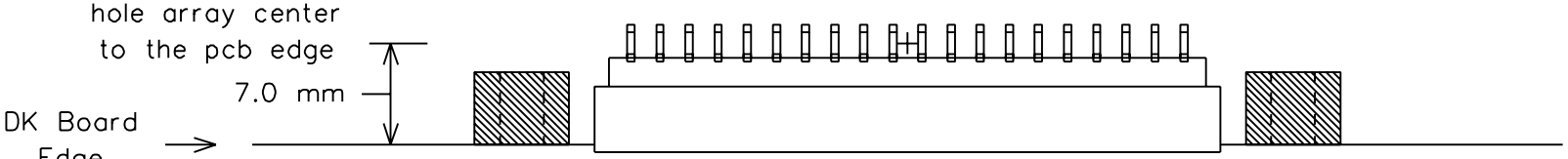
View looking down onto the
top surface of the DK board

Screw Blocks:
6.35 mm wide
5.00 mm deep
9.75 mm tall
with a M3
threaded hole
SMTRAM3-7-5ET
dimensions

Connector's through
hole array center
to the pcb edge

7.0 mm

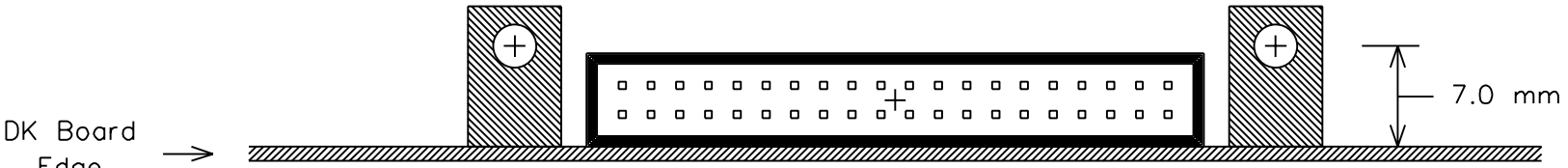
DK Board
Edge



The connector
overhangs the
the pcb edge
by 0.40 mm

The Screw block
is flush with
the pcb edge

51.4 mm
Hole Center to Hole Center



Screw hole
center above
the DK board's
top surface

7.0 mm

DK Board
Edge

7.0 mm - 3.15 mm = 3.85 mm

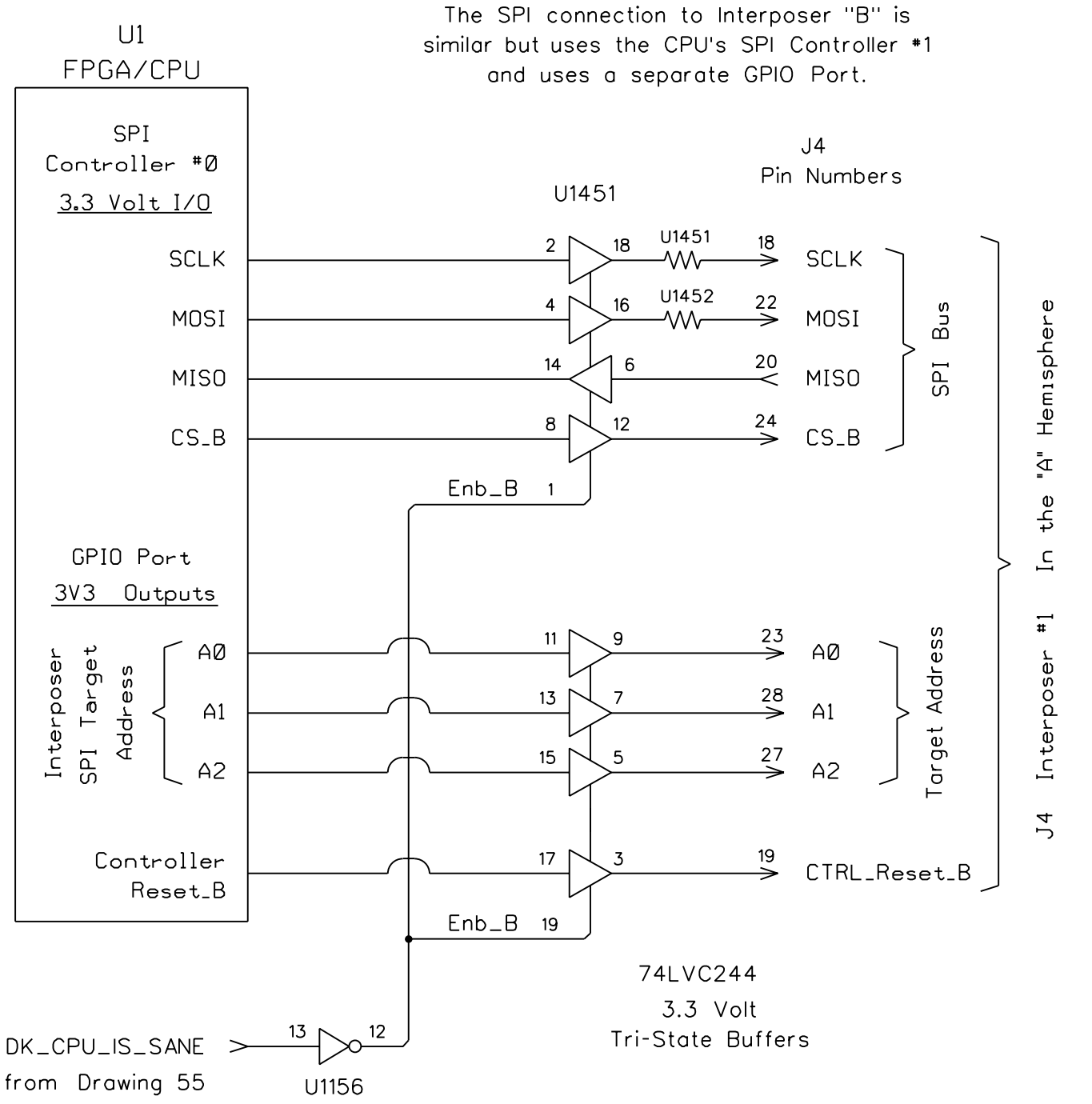
The center of the
connector's 40 pin array
is 3.15 mm above the
DK board's top surface.

View looking into the
Interposer Connector on the DK board

The screw blocks are electrically connected
to the DK board's ground planes.

DK Drw. 87
Rev. 16-Apr-2023

SPI Connection to Interposer "A"



All signals to the Interposer are held in a quiescent state until the DK's CPU is awake and sane.

Not Shown Are the Pull-Up & Pull-Down Resistors:

SCLK & MOSI to the Interposer are Pulled Down: R1461, R1462

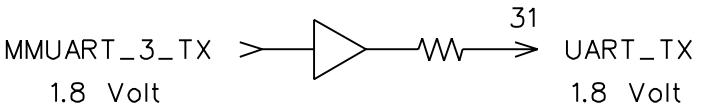
MISO to the SPI Controller is Pulled Down: R1463

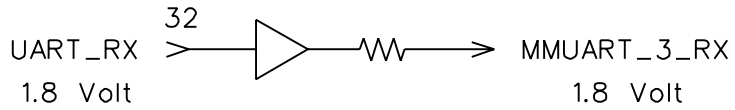
CS_B to the Interposer is Pulled Up: R1464

Ax & CNTL_Reset_B to the Interposer are Pulled Down: R1465...R1468

All Other Connections with the Interposers

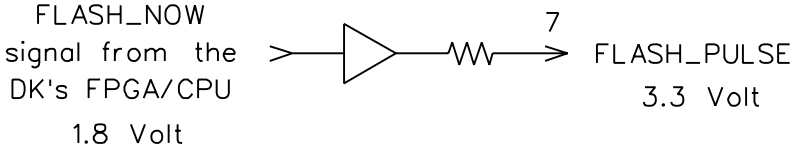
Connections From the DK Board	Connections To an Interposer	Connections From an Interposer	Connections To the DK Board

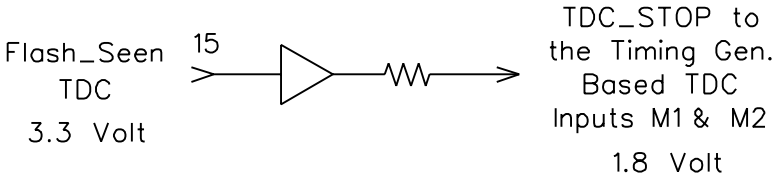




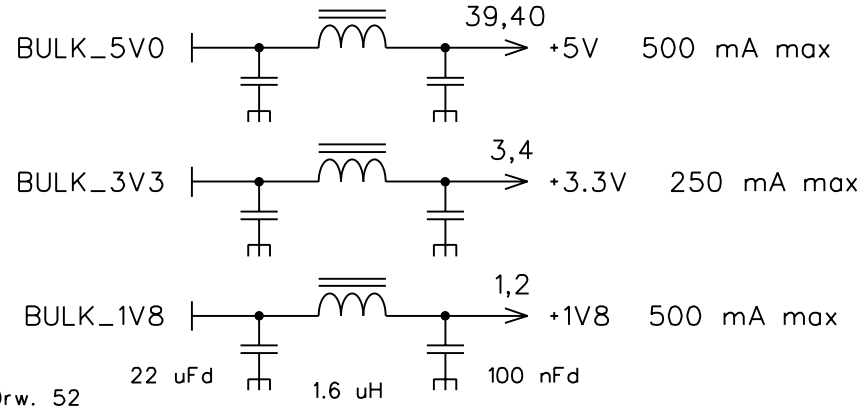
CPU MMUART_3 Services Interposer "A"
CPU MMUART_4 Services Interposer "B"

J4, J5
Pin Numbers

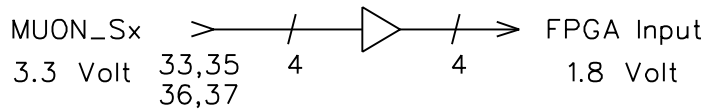


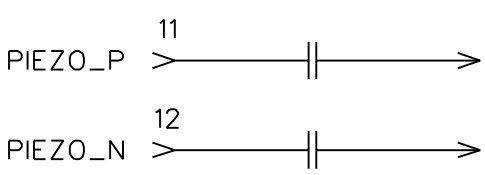


Separate Power Filters for Interposers "A" & "B"



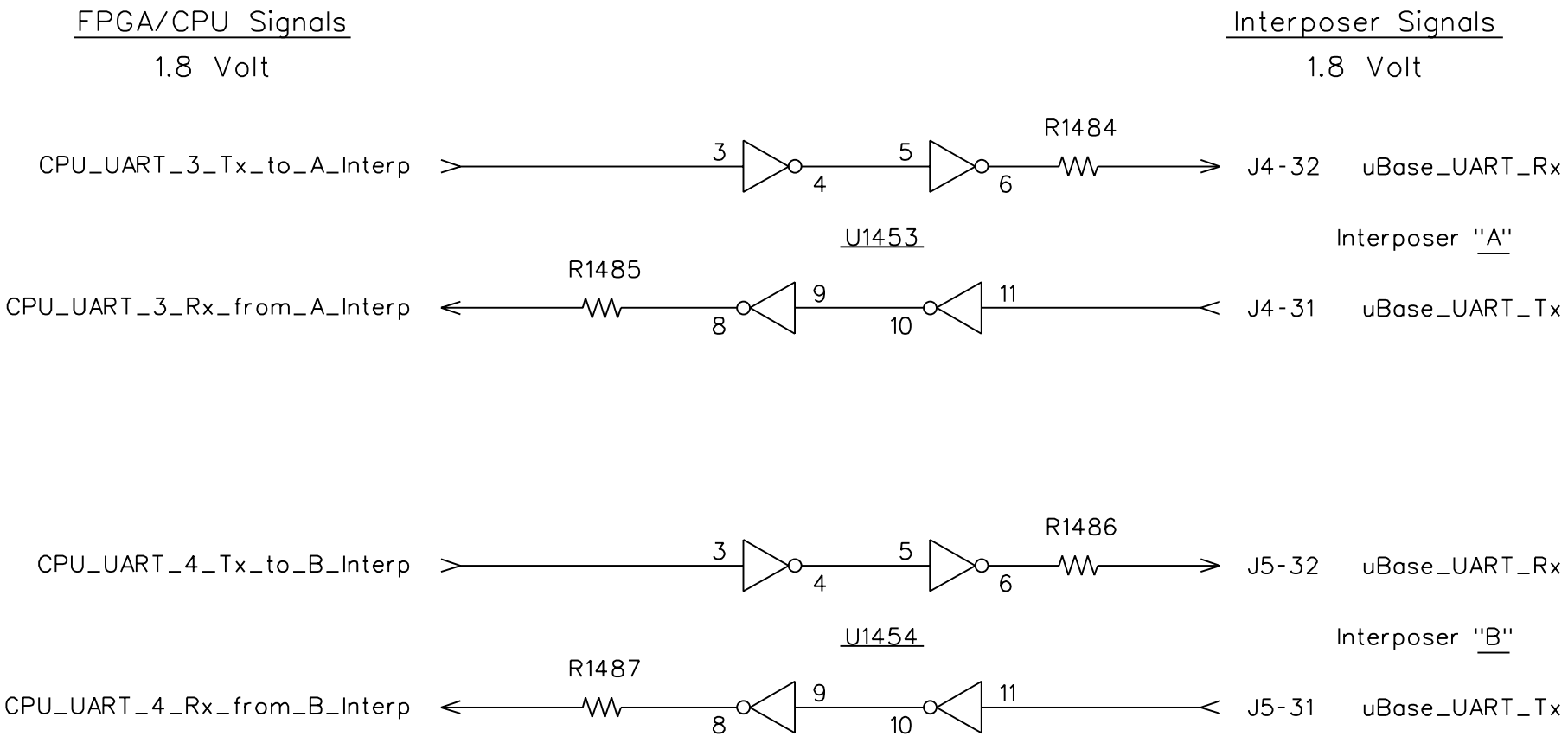
Muon Scintillator Signals from Interposer "B" Only





Interposer Connection Details Page 1

PMT microBase - UART Signals

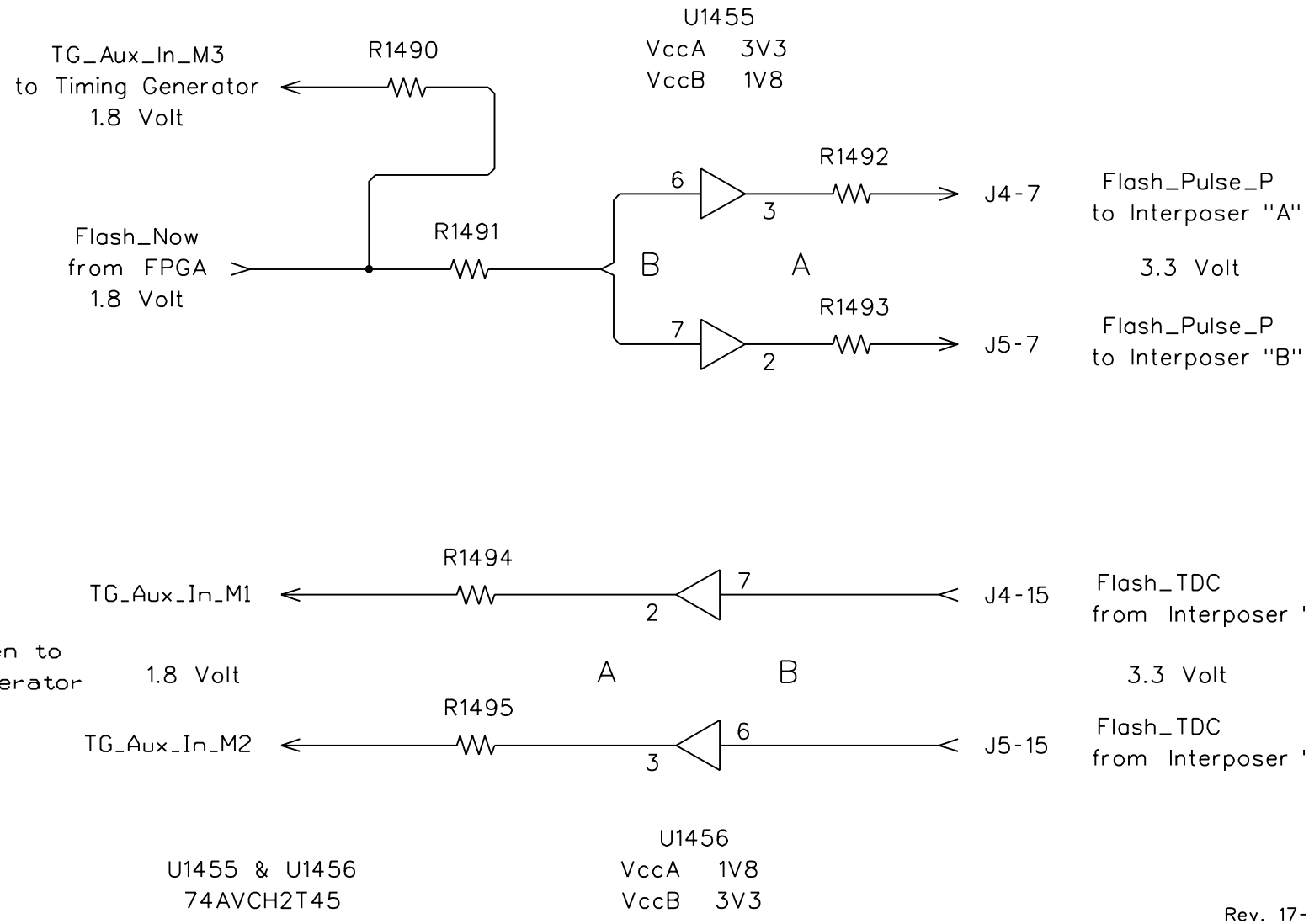


U1454 and U1455 are 1.8 Volt and have 2 unused sections each.

Interposer Connection Details Page 2

DK FPGA/CPU and Timing Generator Signals

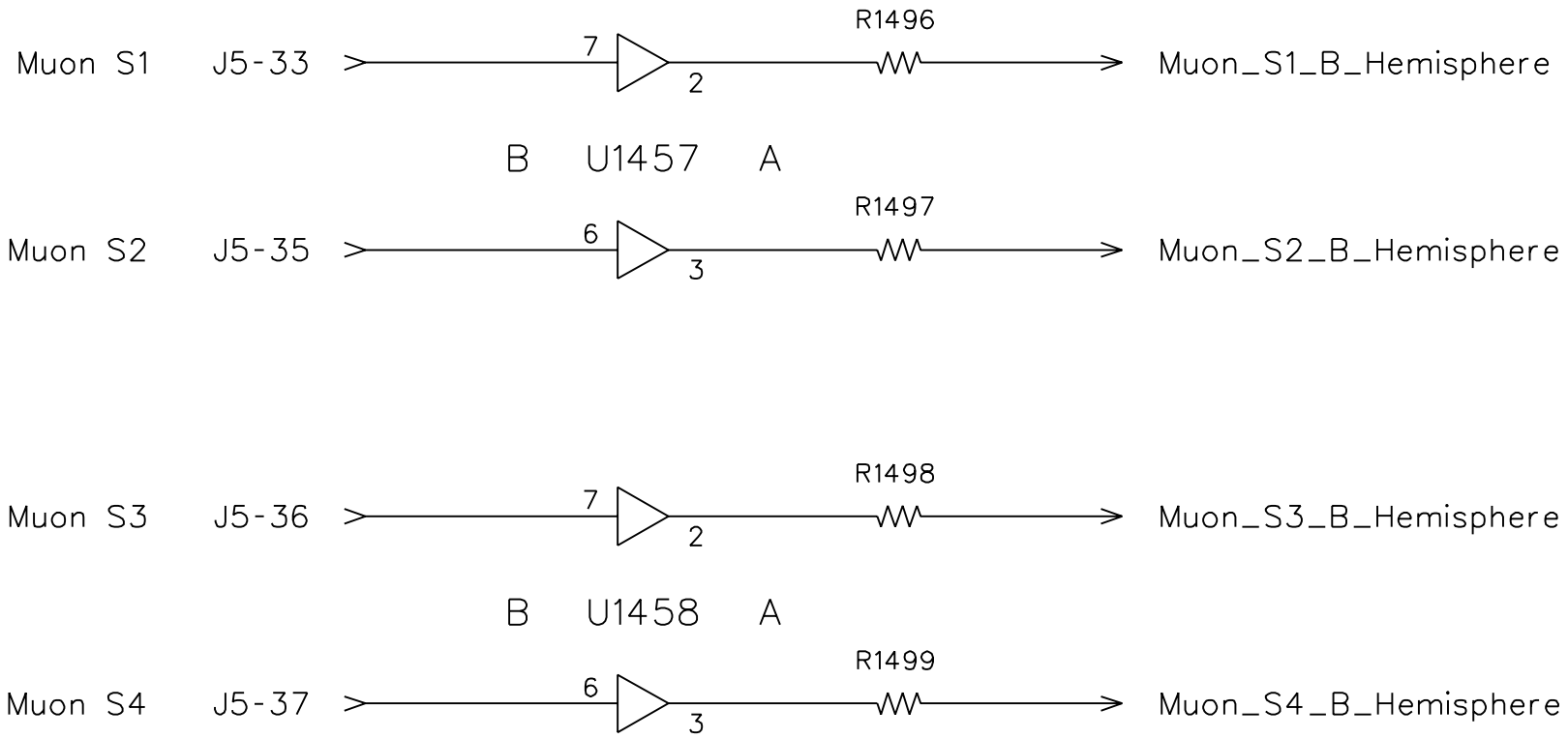
Interposer Signals



Interposer Connection Details Page 3

Interposer "B"
Muon Scintillator
Signals 3.3 Volt

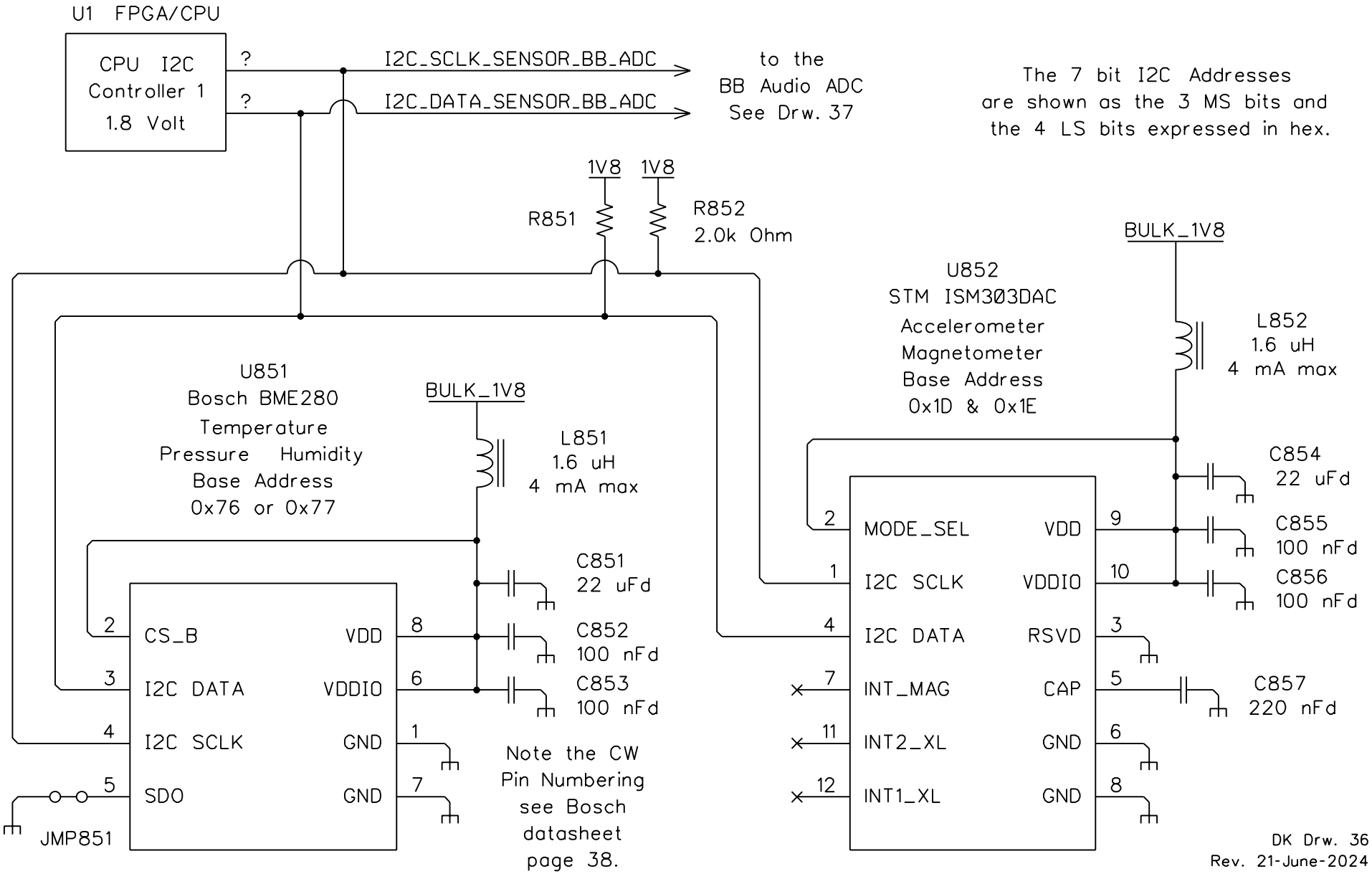
DK FPGA/CPU
Signals 1.8 Volt



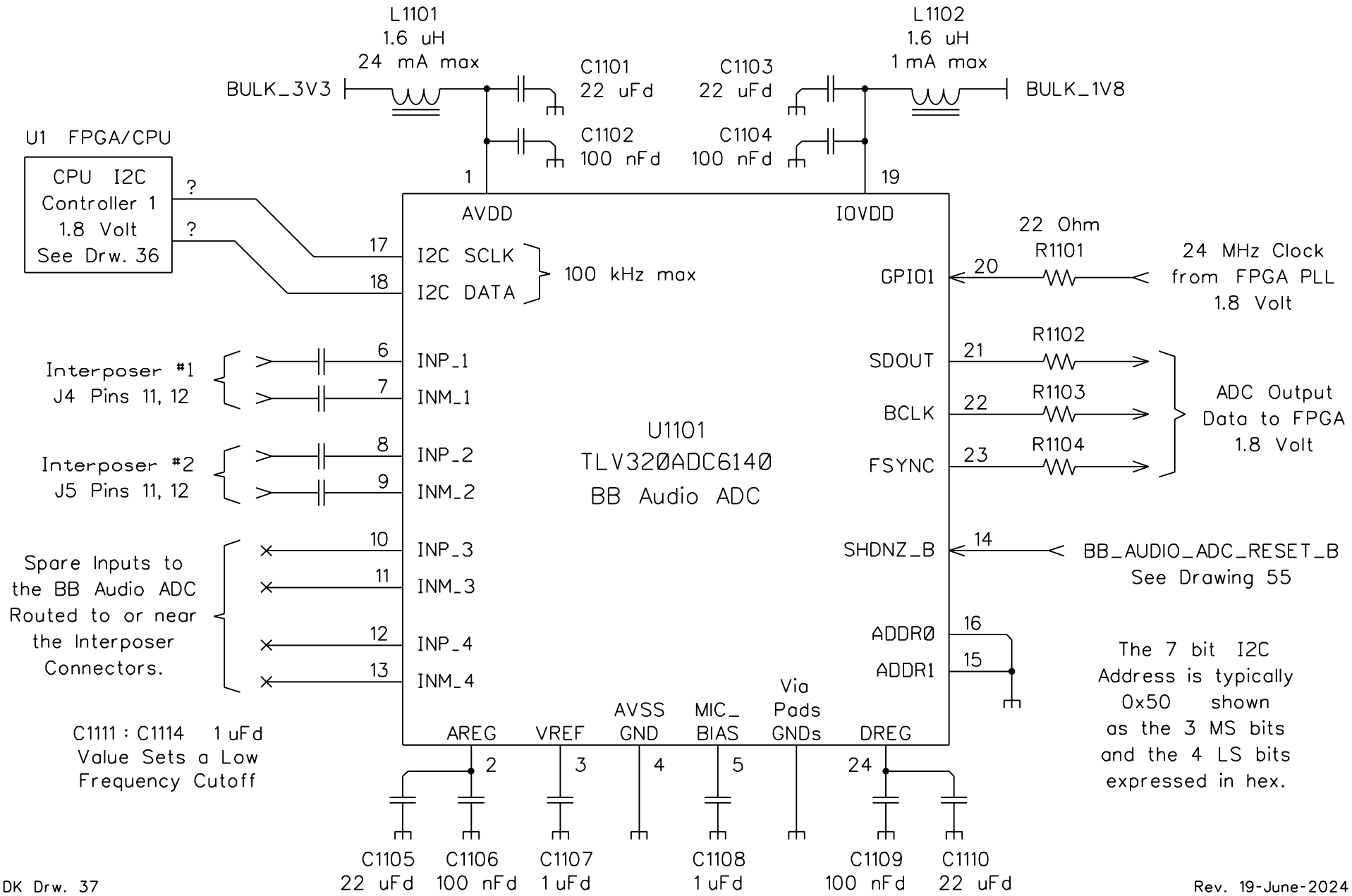
U1457 & U1458
VccA 1V8
VccB 3V3

U1457 & U1458
74AVCH2T45

Environmental Sensors



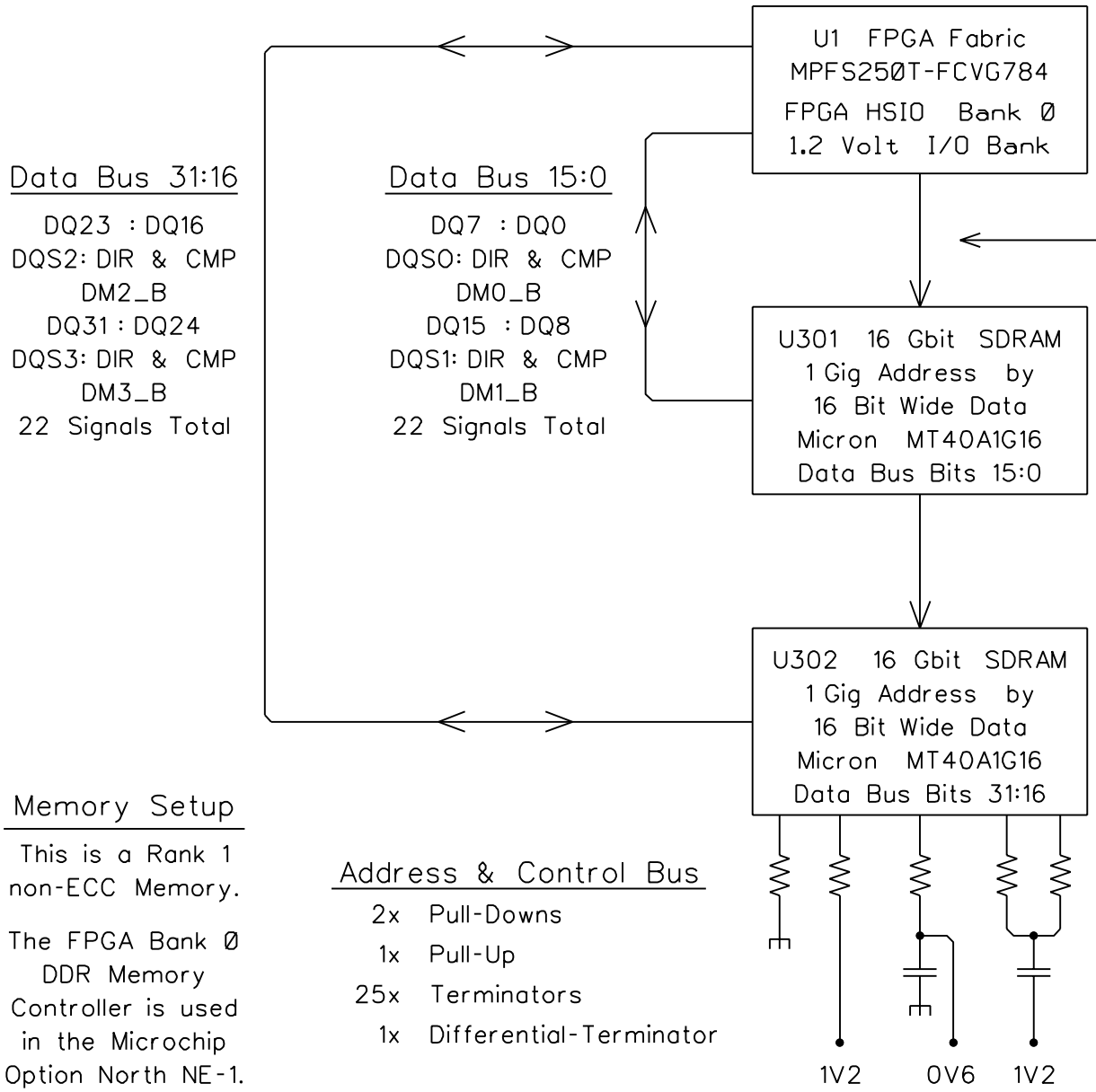
BB Audio ADC



DK Drw. 37

Rev. 19-June-2024

FPGA DDR4 Memory - 4 GBytes - 32 Bit Wide Data



Data Bus 31:16

DQ23 : DQ16
DQS2: DIR & CMP
DM2_B
DQ31 : DQ24
DQS3: DIR & CMP
DM3_B
22 Signals Total

Data Bus 15:0

DQ7 : DQ0
DQS0: DIR & CMP
DM0_B
DQ15 : DQ8
DQS1: DIR & CMP
DM1_B
22 Signals Total

Address & Control Bus

ADRS13 : ADRS0	Term
ADRS14_WE_B	Term
ADRS15_CAS_B	Term
ADRS16_RAS_B	Term
BA1, BA0	Term
BG0	Term
ODT	Term
CLK: DIR & CMP	Diff-Term
CLK_ENB	Term
CS_B	Term
ALERT_B	Pull-Up
PARITY	Term
ACT_B	Term
RESET_B	Pull-Down
TEN	Pull-Down

30 Signals Total

Memory Setup

This is a Rank 1 non-ECC Memory.

The FPGA Bank 0 DDR Memory Controller is used in the Microchip Option North NE-1.

Address & Control Bus

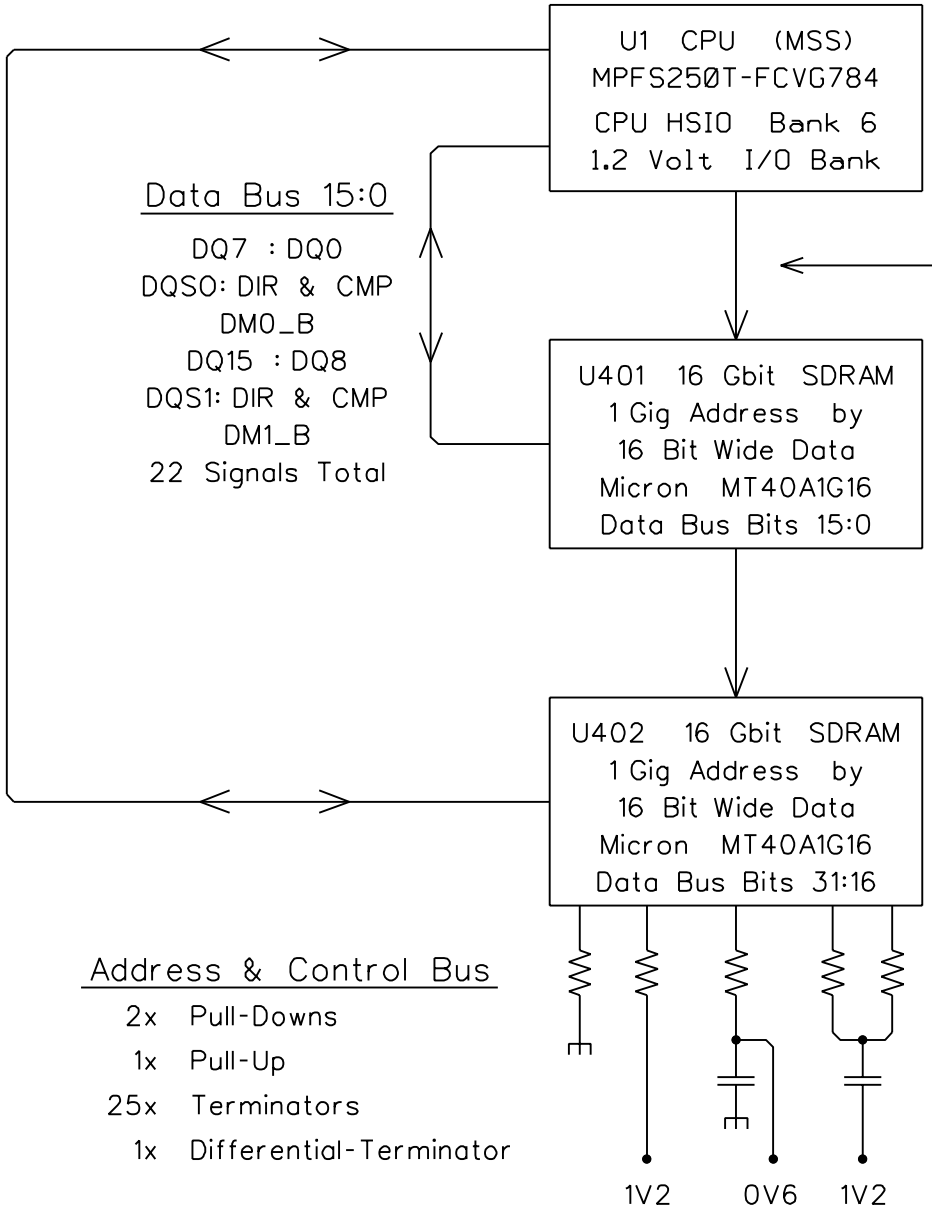
2x	Pull-Downs
1x	Pull-Up
25x	Terminators
1x	Differential-Terminator

Memory Chip Power Supplies

Core Power	1V2
I/O Power	1V2
Word-Line Power	2V5
Reference Supply	0V6
ZQ Calibration	240 Ohm to GND.

DK Drw. 38
Rev. 8-June-2023

CPU DDR4 Memory - 4 GBytes - 32 Bit Wide Data



Data Bus 31:16

DQ23 : DQ16
DQS2: DIR & CMP
DM2_B
DQ31 : DQ24
DQS3: DIR & CMP
DM3_B
22 Signals Total

Data Bus 15:0

DQ7 : DQ0
DQS0: DIR & CMP
DM0_B
DQ15 : DQ8
DQS1: DIR & CMP
DM1_B
22 Signals Total

Address & Control Bus

ADRS13 : ADRS0	Term
ADRS14_WE_B	Term
ADRS15_CAS_B	Term
ADRS16_RAS_B	Term
BA1, BA0	Term
BG0	Term
ODT	Term
CLK: DIR & CMP	Diff-Term
CLK_ENB	Term
CS_B	Term
ALERT_B	Pull-Up
PARITY	Term
ACT_B	Term
RESET_B	Pull-Down
TEN	Pull-Down

30 Signals Total

Memory Chip Power Supplies

Core Power	1V2
I/O Power	1V2
Word-Line Power	2V5
Reference Supply	0V6
ZQ Calibration	240 Ohm to GND.

Memory Setup

This is a Rank 1 non-ECC Memory.

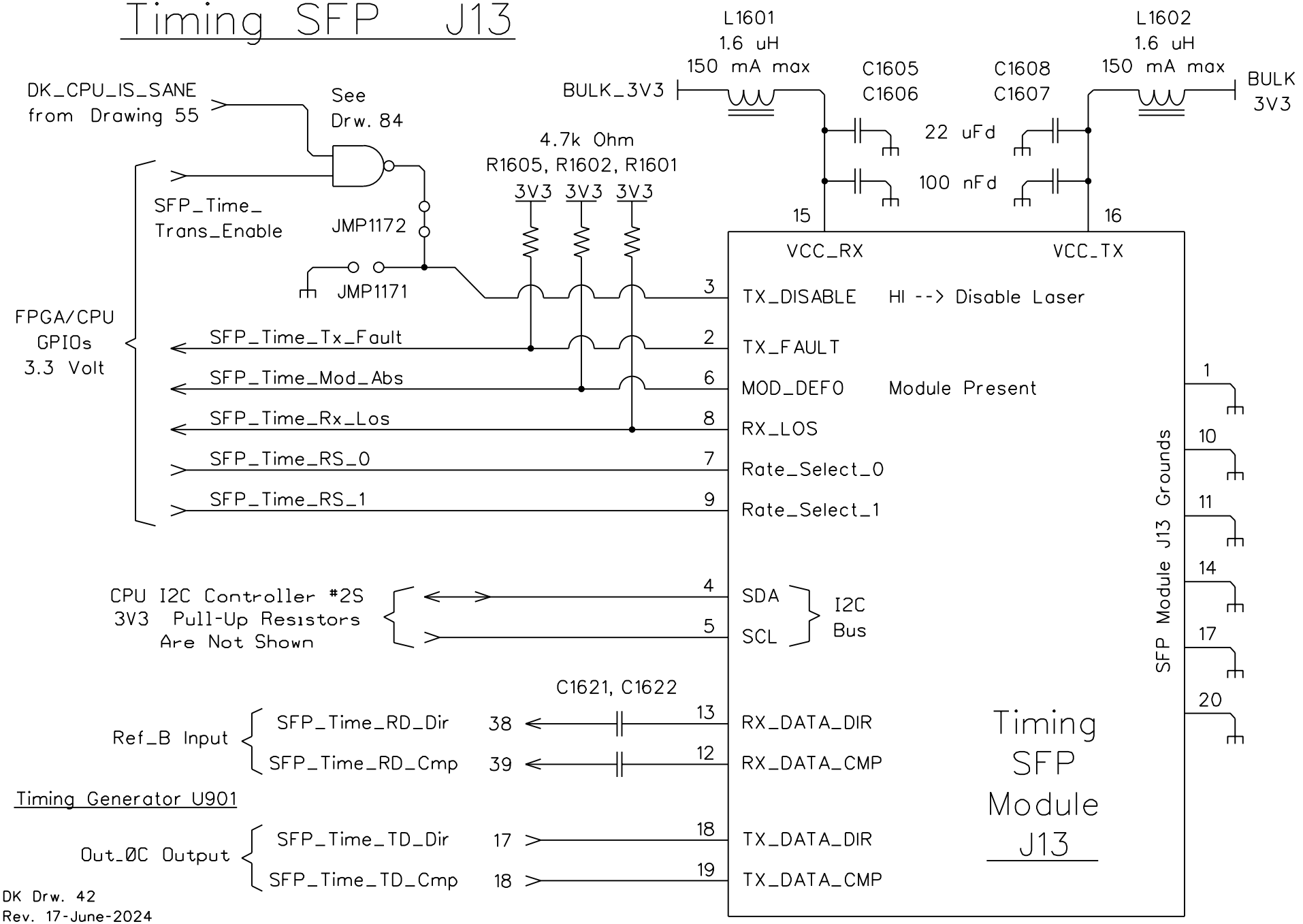
The CPU Bank 6 DDR Memory Controller pins for Rank 2 and for ECC are not used.

Address & Control Bus

2x	Pull-Downs
1x	Pull-Up
25x	Terminators
1x	Differential-Terminator

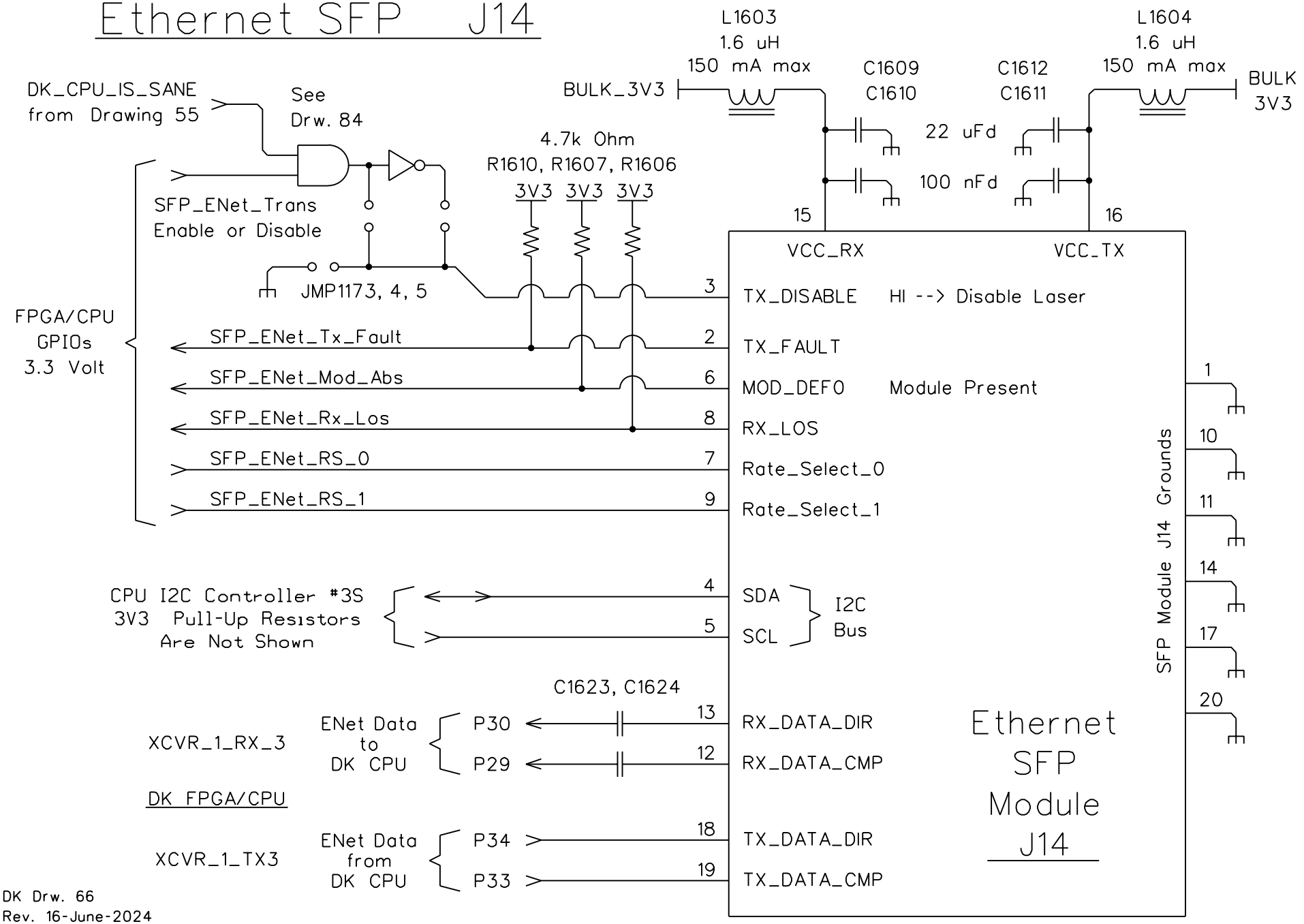
DK Drw. 39
Rev. 12-June-2023

Timing SFP J13



DK Drw. 42
Rev. 17-June-2024

Ethernet SFP J14



DK Drw. 66
Rev. 16-June-2024

High-Speed Serial Transceivers

Serial Transceivers 1 SFP Ethernet

K34, K33	XCVR_1_TX0	Not Used
M34, M33	XCVR_1_TX1	Not Used
N32, N31	XCVR_1_TX2	Not Used
P34, P33	XCVR_1_TX3	Ethernet SFP Transmit Data
K30, K29	XCVR_1_RX0	Not Used
L32, L31	XCVR_1_RX1	Not Used
M30, M29	XCVR_1_RX2	Not Used
P30, P29	XCVR_1_RX3	Ethernet SFP Received Data
L27, L28	XCVR_1A_REFCLK	Not Used
N27, N28	XCVR_1B_REFCLK	Not Used
H29, H30	XCVR_1C_REFCLK	Not Used

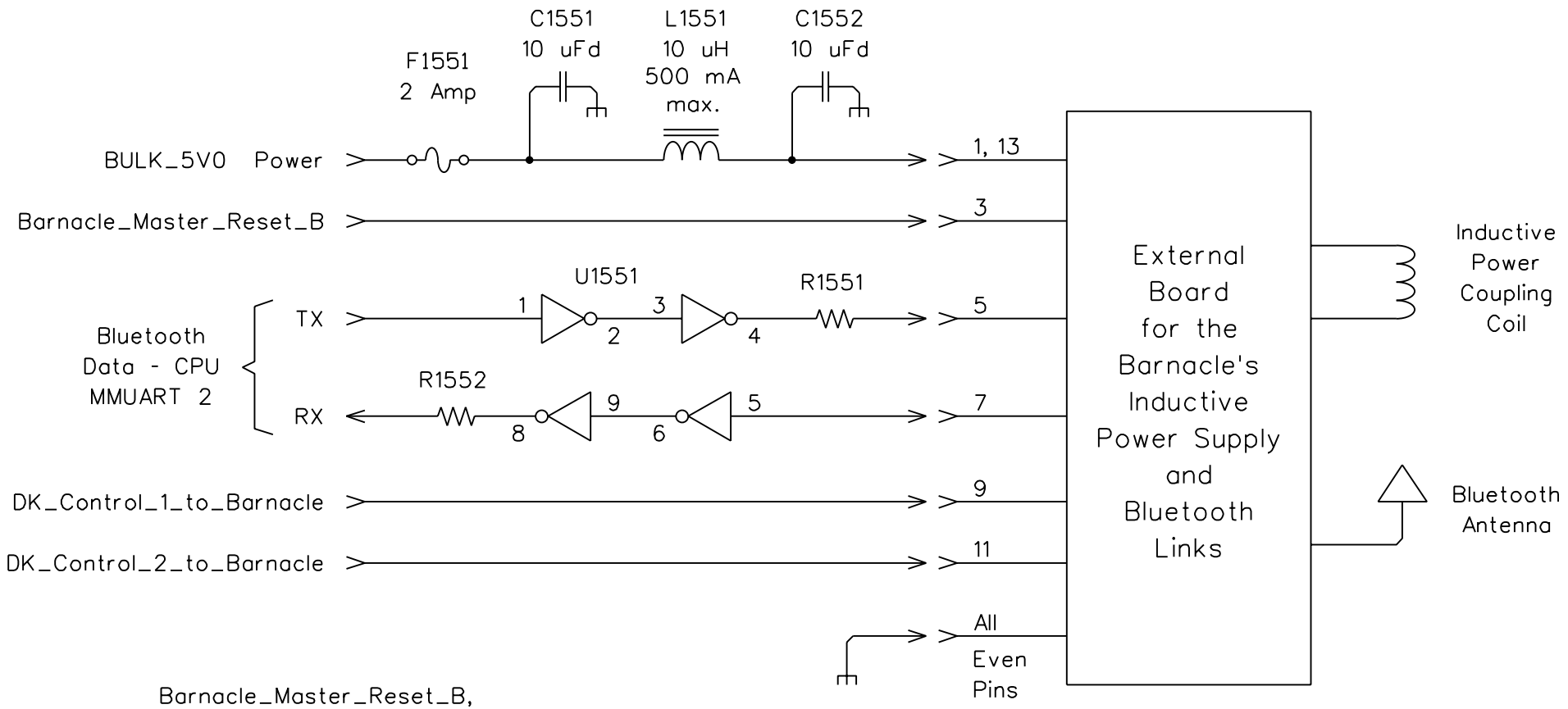
Serial Transceivers 3 PMT ADC Data

B34, B33	XCVR_3_TX0	Not Used
D34, D33	XCVR_3_TX1	Not Used
F34, F33	XCVR_3_TX2	Not Used
H34, H33	XCVR_3_TX3	Not Used
C32, C31	XCVR_3_RX0	ADC Data Lane 0 Inverted
E32, E31	XCVR_3_RX1	ADC Data Lane 1 Inverted
G32, G31	XCVR_3_RX2	ADC Data Lane 2
J32, J31	XCVR_3_RX3	ADC Data Lane 3
F29, F30	XCVR_3A_REFCLK	JESD Ref Clk Timing Gen OUT_1A
D29, D30	XCVR_3C_REFCLK	Not Used

Pin Numbers Listed:
Direct then Complement

XCVR_0 & XCVR_2
Are Not Used by DK

Connection to the Barnacle Board



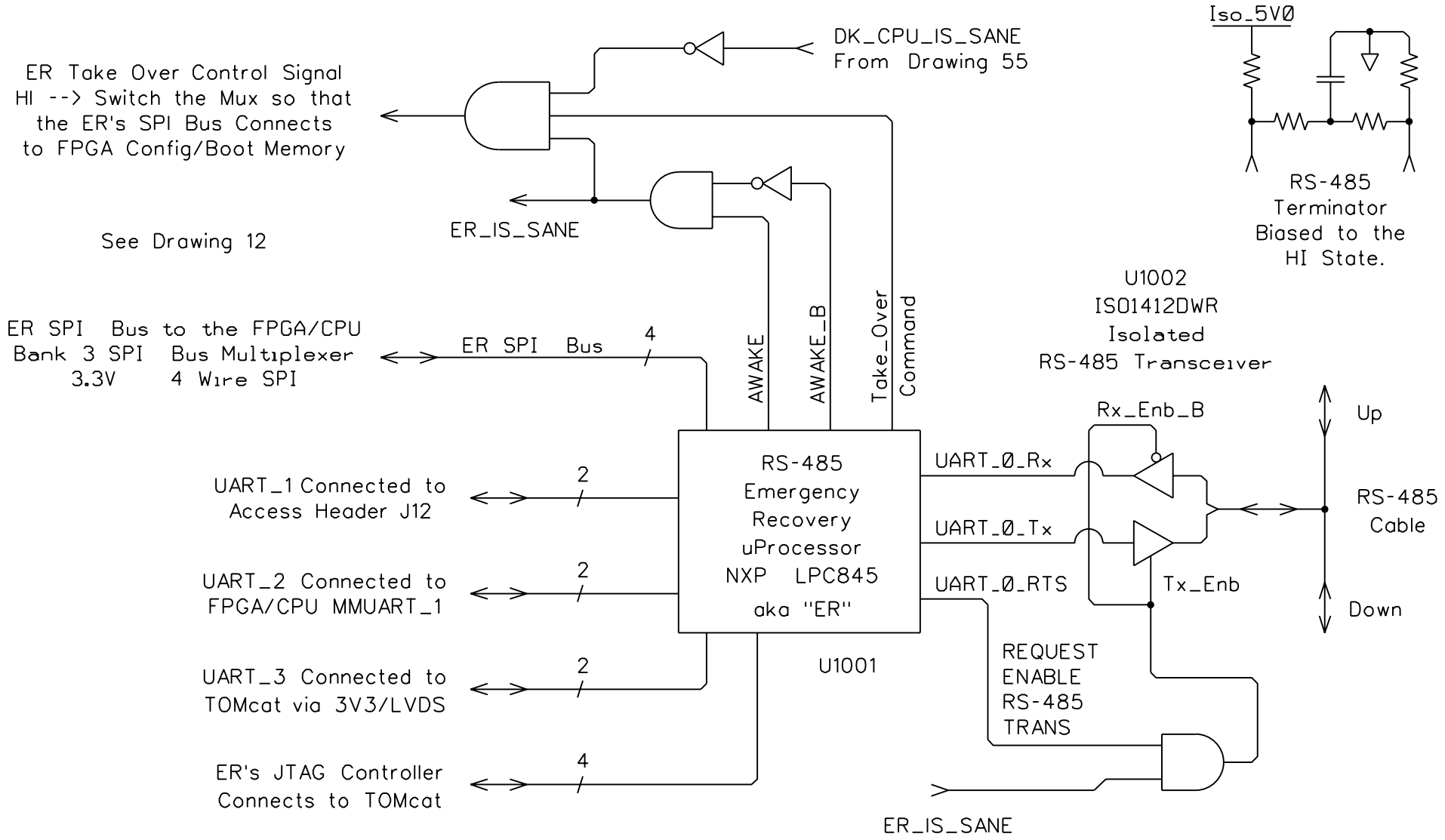
Barnacle_Master_Reset_B, DK_Control_1_to_Barnacle, and DK_Control_2_to_Barnacle, are all Open-Drian signals that will be held Low during Module Power Up. Pull-Up resistors are on the Barnacle. Pull-Up current should be held below 1.5 mA.

Connector J7
14 Pin Header
on the
DK Board

UART data to/from Barnacle is 3.3 Volt.

Asserting Barnacle_Master_Reset_B must Turn OFF most of the power consumption by the Inductive Power Supply and the Bluetooth Transceiver.

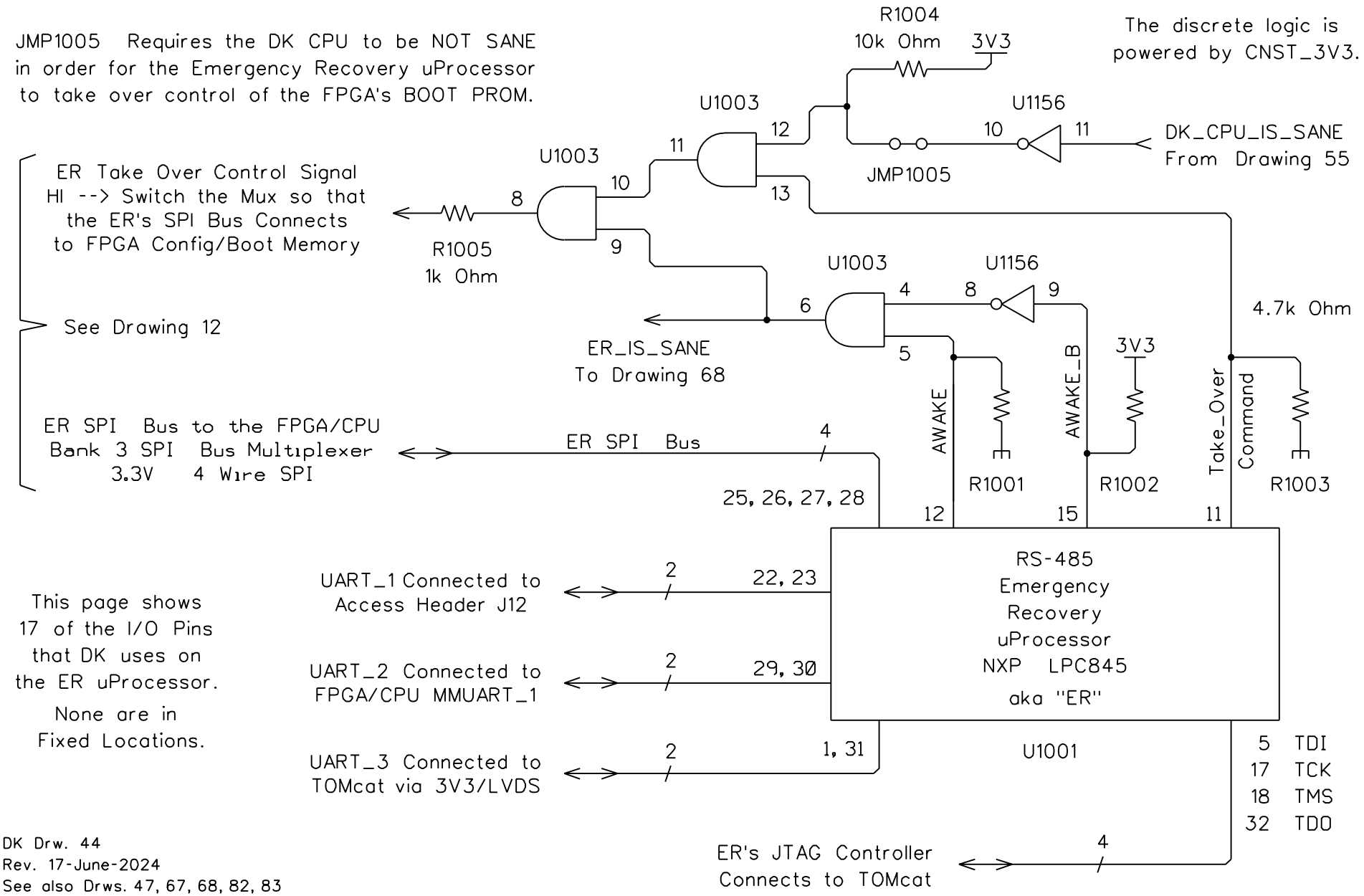
RS-485 Emergency Recovery - Simplified



DK Drw. 67
See also Drws. 44, 47, 68, 82, 83

Rev. 17-June-2024

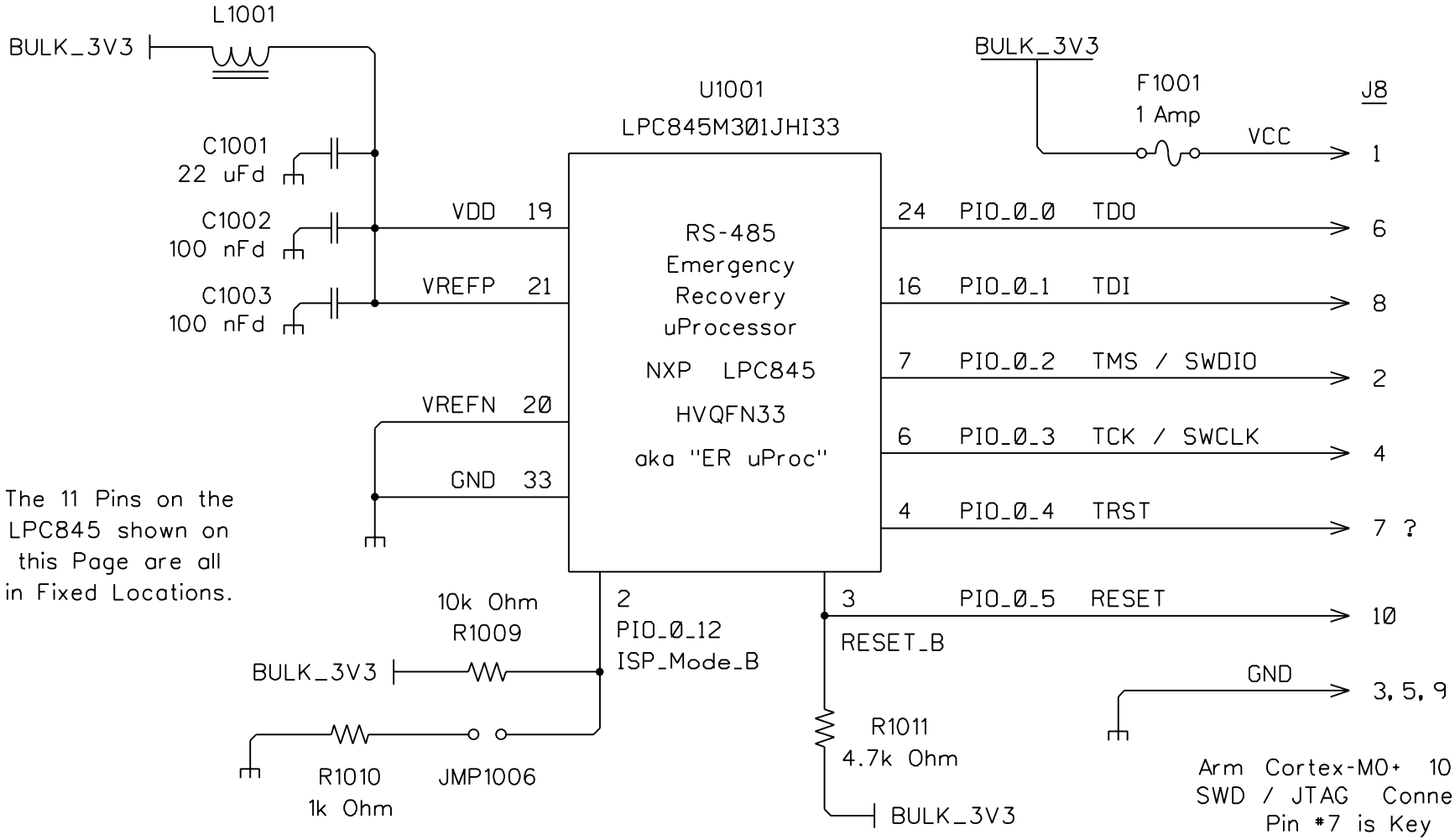
RS-485 Emergency Recovery Page 1



DK Drw. 44
Rev. 17-June-2024
See also Drws. 47, 67, 68, 82, 83

RS-485 Emergency Recovery Page 2

Power, Reset, ISP, SWD, and JTAG



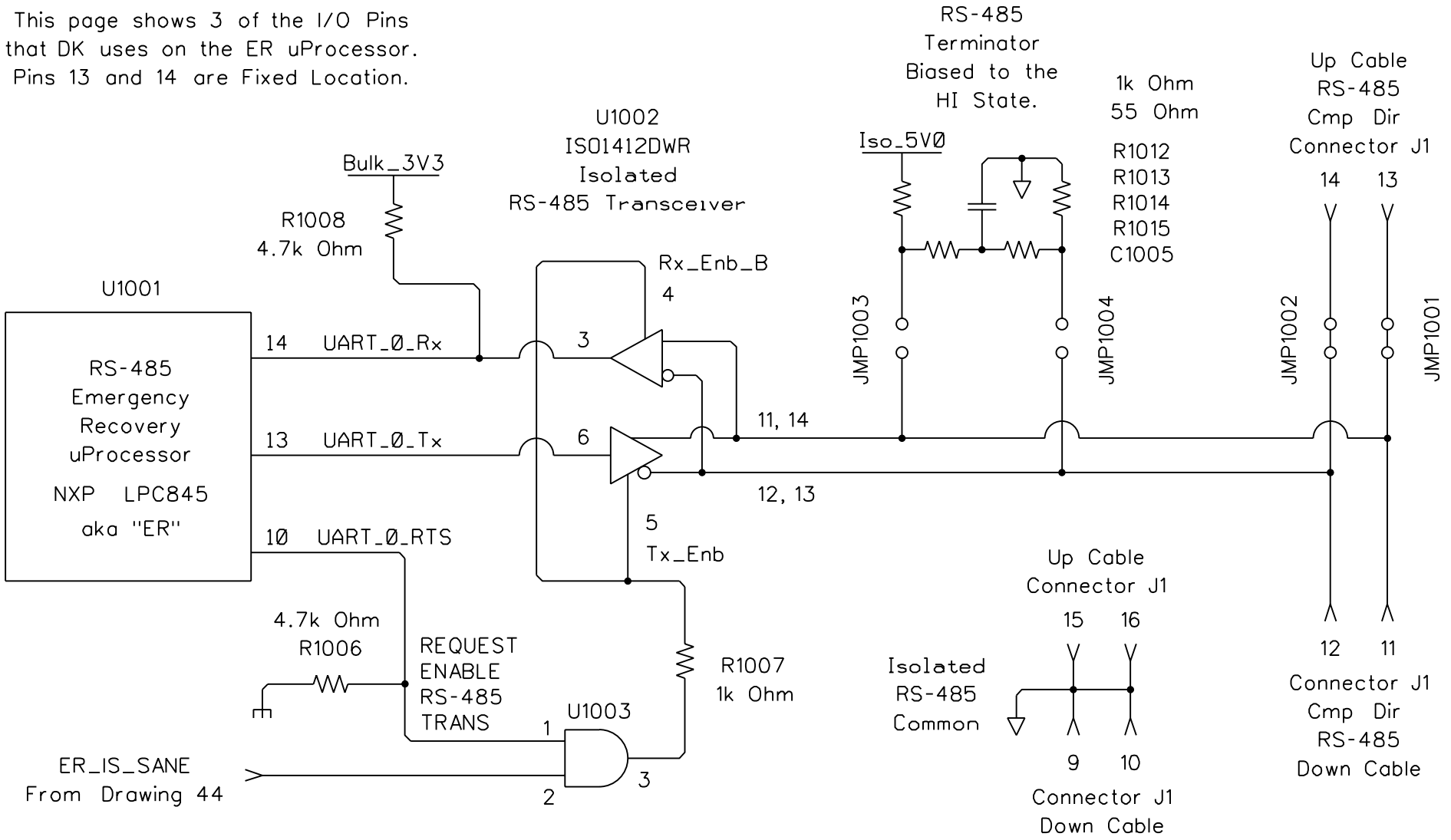
The 11 Pins on the LPC845 shown on this Page are all in Fixed Locations.

JMP1006 is the ISP Mode Jumper
Low during Reset starts the
In System Programming command handler.
Open for normal startup & operation.

Arm Cortex-M0+ 10 Pin
SWD / JTAG Connector
Pin #7 is Key
Board Header: FTSH-105-01
Pull-Ups on: TDI, TMS, TCK, TRST
R1016 : R1019 10k Ohm
See User's Guide Page 505

DK Drw. 47
Rev. 18-Apr-2024
See also Drws. 44, 67, 68, 82, 83

RS-485 Emergency Recovery Page 3

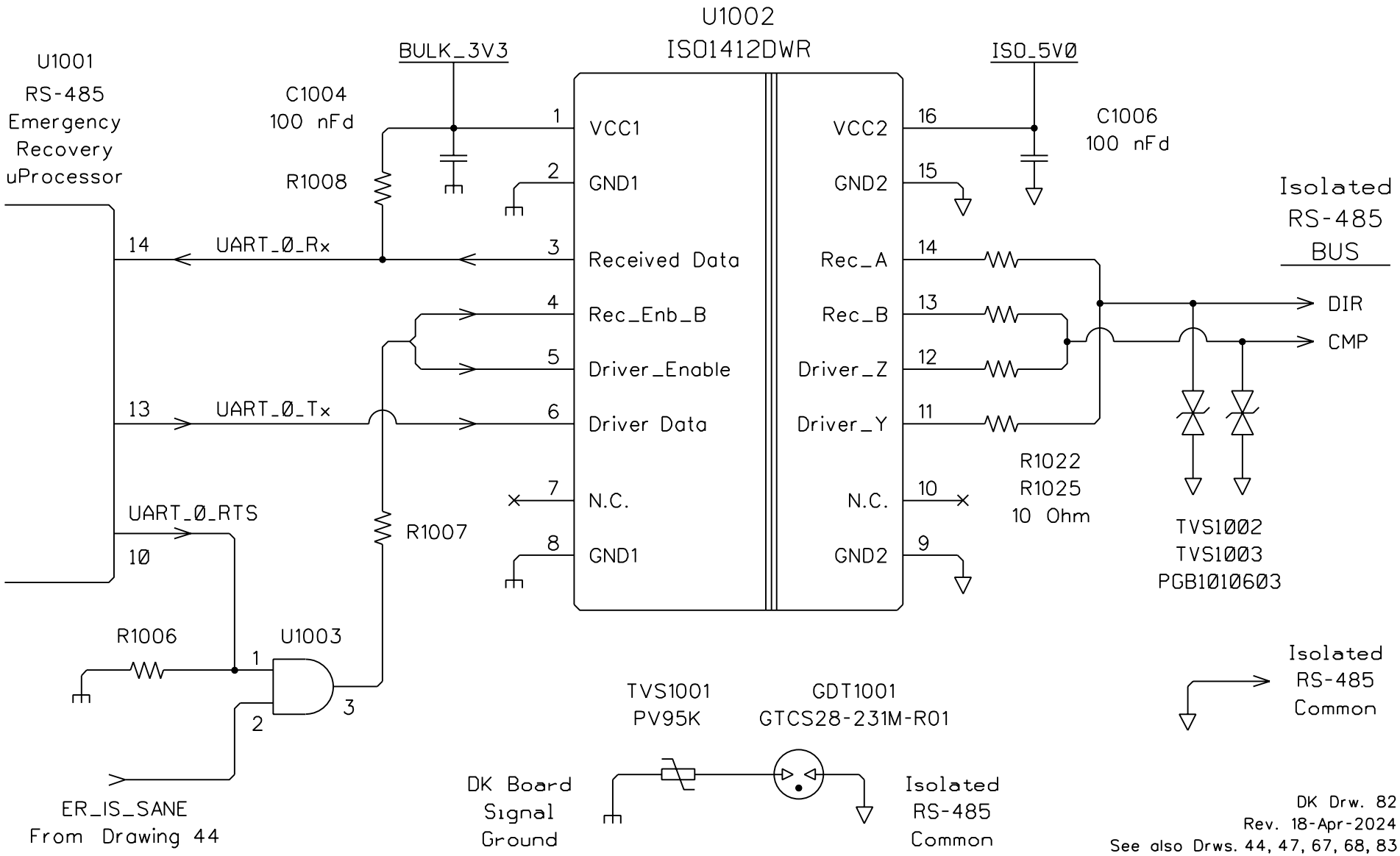


The Emergency Rescue uProcessor and its side
of the RS-485 Transceiver are powered by Bulk_3V3.
The Logic Gate is powered by CNST_3V3.

DK Drw. 68
See also Drws. 44, 47, 67, 82, 83

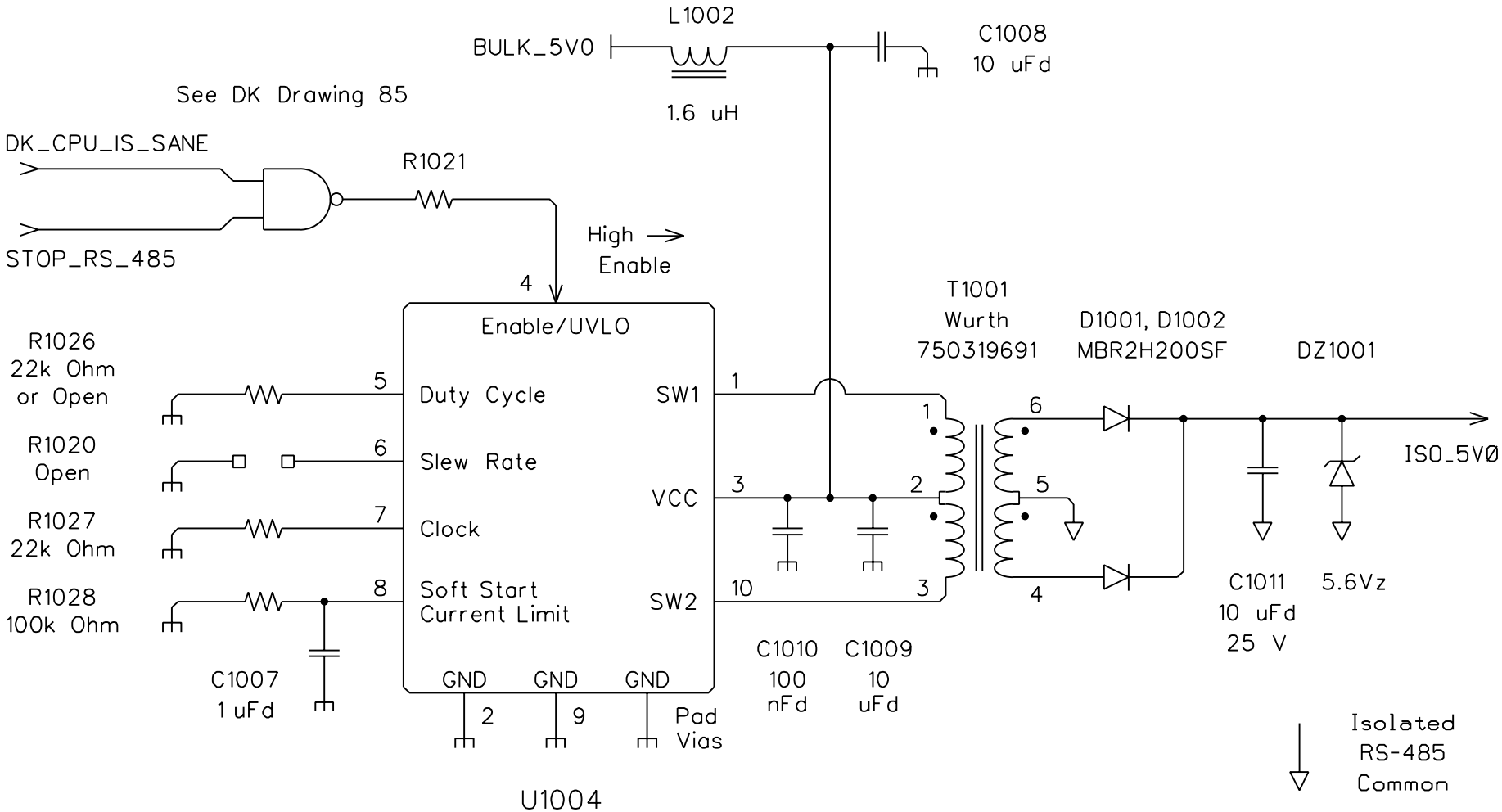
Rev. 19-Apr-2024

Isolated RS-485 Transceiver



DK Drw. 82
Rev. 18-Apr-2024
See also Drws. 44, 47, 67, 68, 83

Isolated RS-485 Power Supply



Power Supply Operation:

518 kHz Switching Frequency
264 mA Current Limit
3.72 msec Soft Start

DK Drw. 83
Rev. 18-Apr-2024
See also Drws. 44, 47, 67, 68, 82

Power Supply Monitor J11 & FPGA Access J12

Power Supply Monitor Connector J11

Pin Num	Function	Pin Num	Function
1	VMon_Bulk_5V0	2	Ground
3	VMon_Bulk_1V00	4	Ground
5	IMon_Pos_Bulk_1V00	6	IMon_Neg_Bulk_1V00
7	VMon_Bulk_1V50	8	Ground
9	IMon_Pos_Bulk_1V50	10	IMon_Neg_Bulk_1V50
11	VMon_Bulk_1V2	12	Ground
13	IMon_Pos_Bulk_1V2	14	IMon_Neg_Bulk_1V2
15	VMon_Bulk_1V8	16	Ground
17	IMon_Pos_Bulk_1V8	18	IMon_Neg_Bulk_1V8
19	VMon_Bulk_2V5	20	Ground
21	IMon_Pos_Bulk_2V5	22	IMon_Neg_Bulk_2V5
23	VMon_Bulk_3V3	24	Ground
25	IMon_Pos_Bulk_3V3	26	IMon_Neg_Bulk_3V3
27	VMon_Cnst_3V3	28	Ground
29	VMon_FPGA_DDR4_Term	30	Ground
31	VMon_CPU_DDR4_Term	32	Ground
33	N.C.	34	N.C.
35	N.C.	36	N.C.
37	N.C.	38	N.C.
39	N.C.	40	N.C.

FPGA/CPU Access Connector J12

Pin Num	Function	Pin Num	Function
1	JTAG_TCLK	2	Gnd
3	JTAG_TDO	4	no-conn
5	JTAG_TMS	6	Power 3V3 5V0
7	no-conn	8	JTAG_TRST
9	JTAG_TDI	10	Gnd
11	Gnd	12	Gnd
13	MMUART *0 Tx	14	MMUART *0 Rx
15	Gnd	16	Gnd
17	ER UART *1 Tx	18	ER UART *1 Rx
19	Gnd	20	Gnd
21	Access_Signal_1	22	Gnd
23	Access_Signal_2	24	Gnd
25	Access_Signal_3	26	Gnd
27	Access_Signal_4	28	Gnd
29	Access_Signal_5	30	Gnd
31	Gnd	32	Gnd
33	Diff_Signal_1_Dir	34	Diff_Signal_1_Cmp
35	Gnd	36	Gnd
37	Diff_Signal_2_Dir	38	Diff_Signal_2_Cmp
39	Gnd	40	Gnd

Pins 1 through 10 of the FPGA/CPU Access Connector match the MicroSemi standard JTAG connector pinout.

Main Cable Connector J1

Main Cable Connector J1

Pin Num	Function	Pin Num	Function
1	Open - Guard	2	Open - Guard
3	+100 VDC Power Feed	4	Open - Guard
5	Open - Guard	6	100V Power Return
7	Open - Guard	8	Open - Guard
9	RS-485 Common Down	10	RS-485 Common Down
11	RS-485_Down_Dir	12	RS-485_Down_Cmp
13	RS-485_Up_Dir	14	RS-485_Up_Cmp
15	RS-485 Common Up	16	RS-485 Common Up

There is Galvanic Isolation between these 3 DK circuit regions:

1. Power Feed/Return, Power Input Filter, 100 V Converter Input
2. Isolated RS-485 Differential Main Cable Bus and its Common
3. DK Board's Signal Ground that services all other DK Board circuits

TOMCat Mezzanine Connector J10

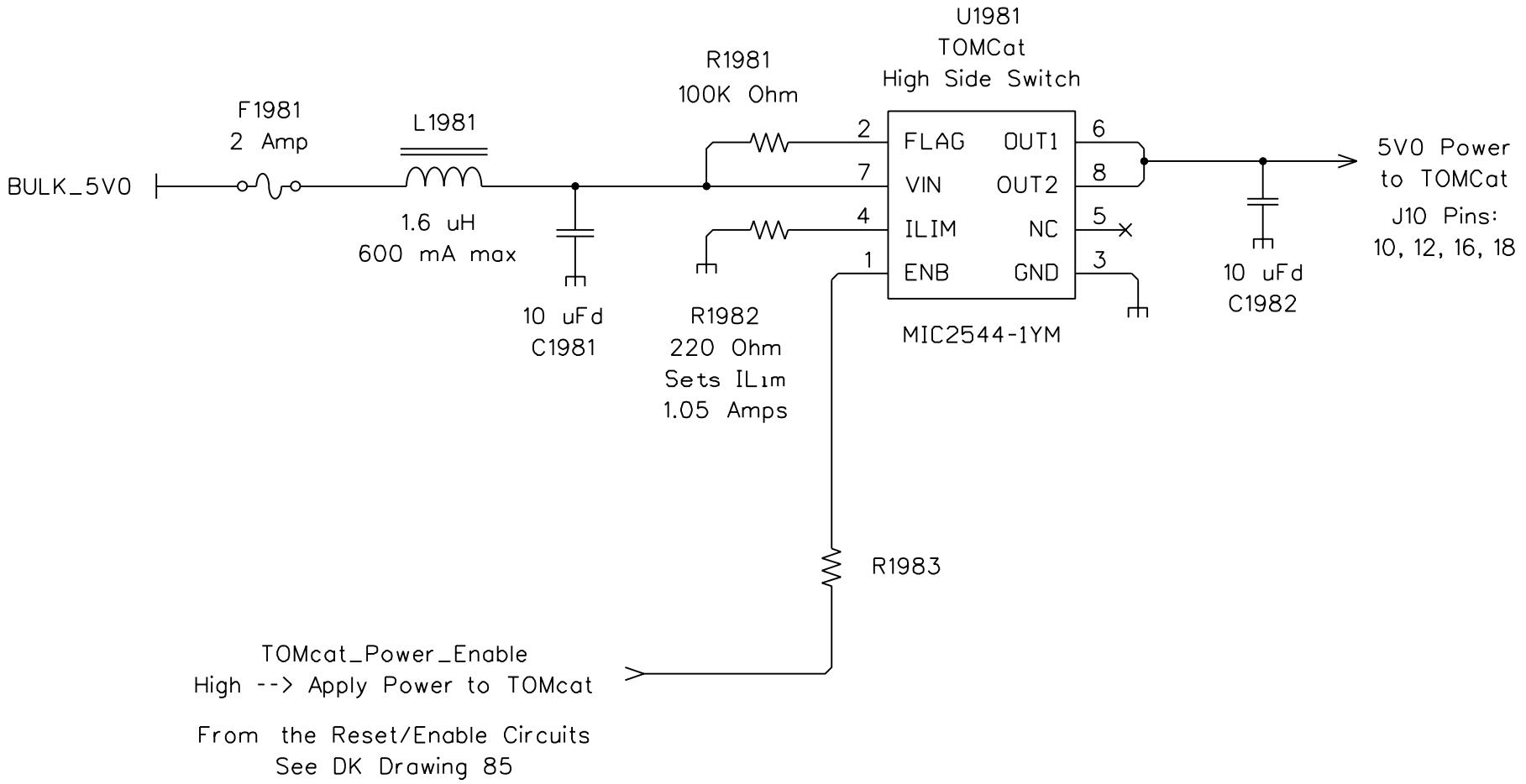
TOMCat Connector J10

		Function	Pin Num	Pin Num	Function		
		Ground	1	2	3V3 for JTAG		
JTAG Controller on ER	←	TDO	3	4	TCK	←	JTAG Controller on ER
	→	TMS	5	6	TDI	←	
		Ground	7	8	Ground		
SGMII Ethernet from DK	→	Rx+	9	10	+5V power		
	→	Rx-	11	12	+5V Power		
		Ground	13	14	Ground		
SGMII Ethernet to DK	←	Tx+	15	16	+5V Power		
	←	Tx-	17	18	+5V Power		
		Ground	19	20	Ground		
1V8 CMOS	× ←	Spare	21	22	CFG1	→	DK FPGA 1V8 CMOS
	× ←	100 Hz	23	24	CFGØ	→	
		Ground	25	26	Ground		
	× ←	100 Hz	27	28	100 Hz-	→	DK FPGA LVDS
AD9546 MØ 1V8 CMOS	←→	PPS	29	30	100 Hz+	→	
		Ground	31	32	Ground		
LVDS	× ←	SPARE-	33	34	125 MHz-	→	DK FPGA LVDS
	× ←	SPARE+	35	36	125 MHz+	→	
		Ground	37	38	Ground		
UART from ER	→	Rx UART-	39	40	PPS-	→ ×	LVDS
	→	Rx UART+	41	42	PPS+	→ ×	
		Ground	43	44	Ground		
UART to ER	←	Tx UART-	45	46	125 MHz-	→	AD9546 REF_A LVDS
	←	Tx UART+	47	48	125 MHz+	→	
		Ground	49	50	Ground		

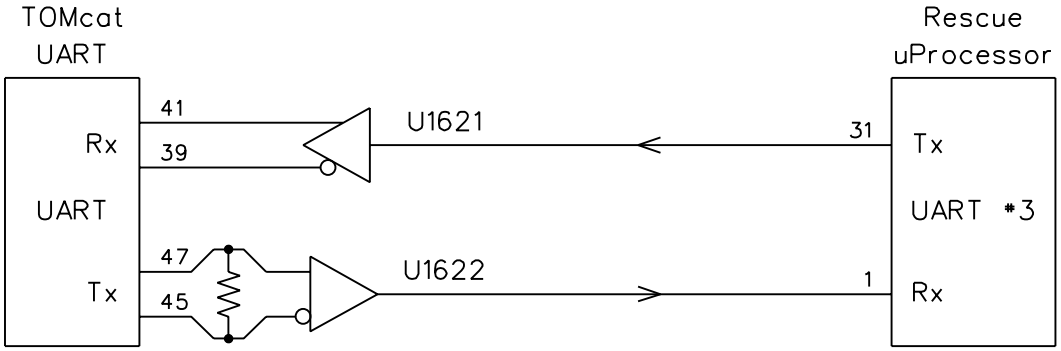
ER = Emergency Rescue uProcessor

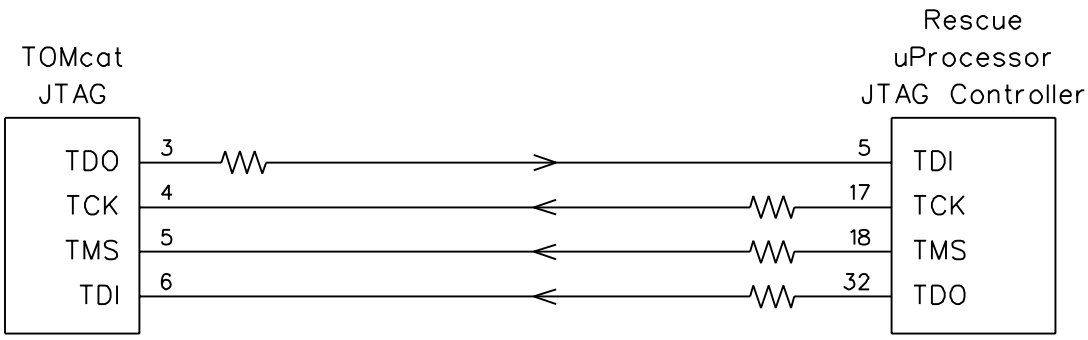
Spare TOMcat pins will be connected to DK FPGA where possible.

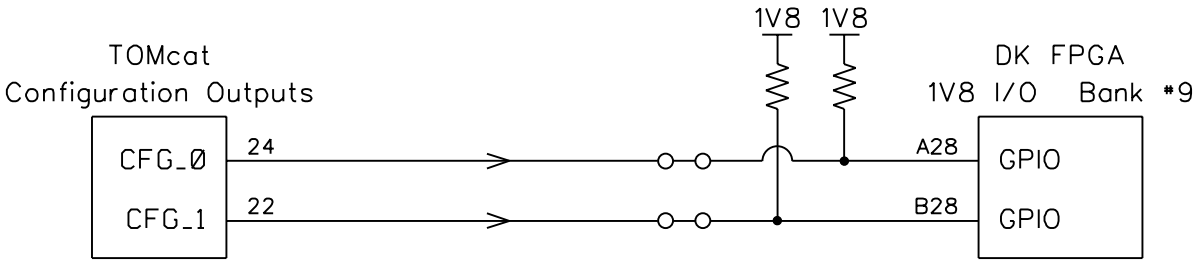
TOMCat Power Switch



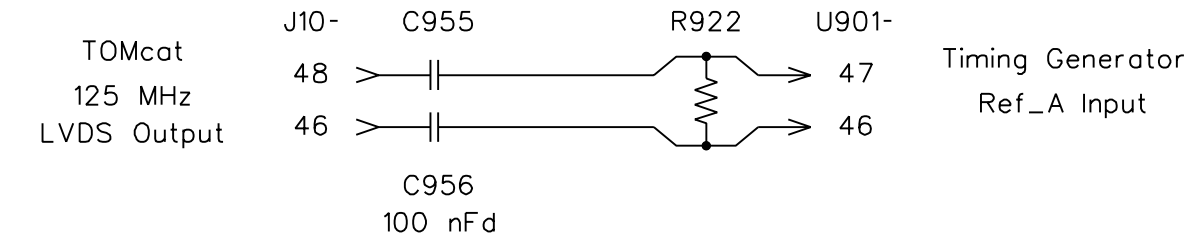
TOMCat Connections to DK Board Pg 1

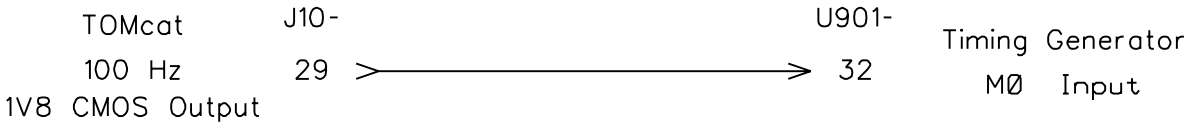


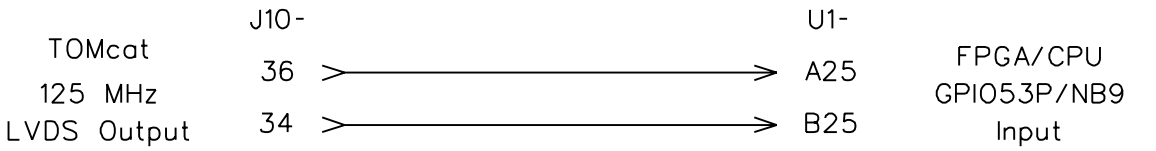


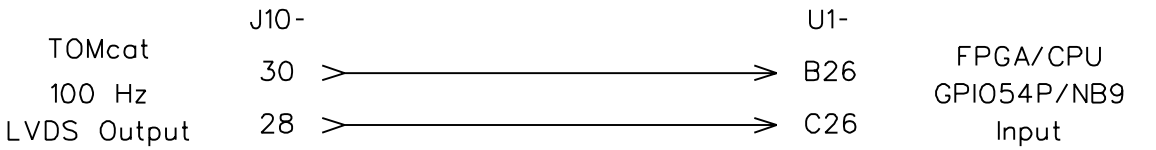


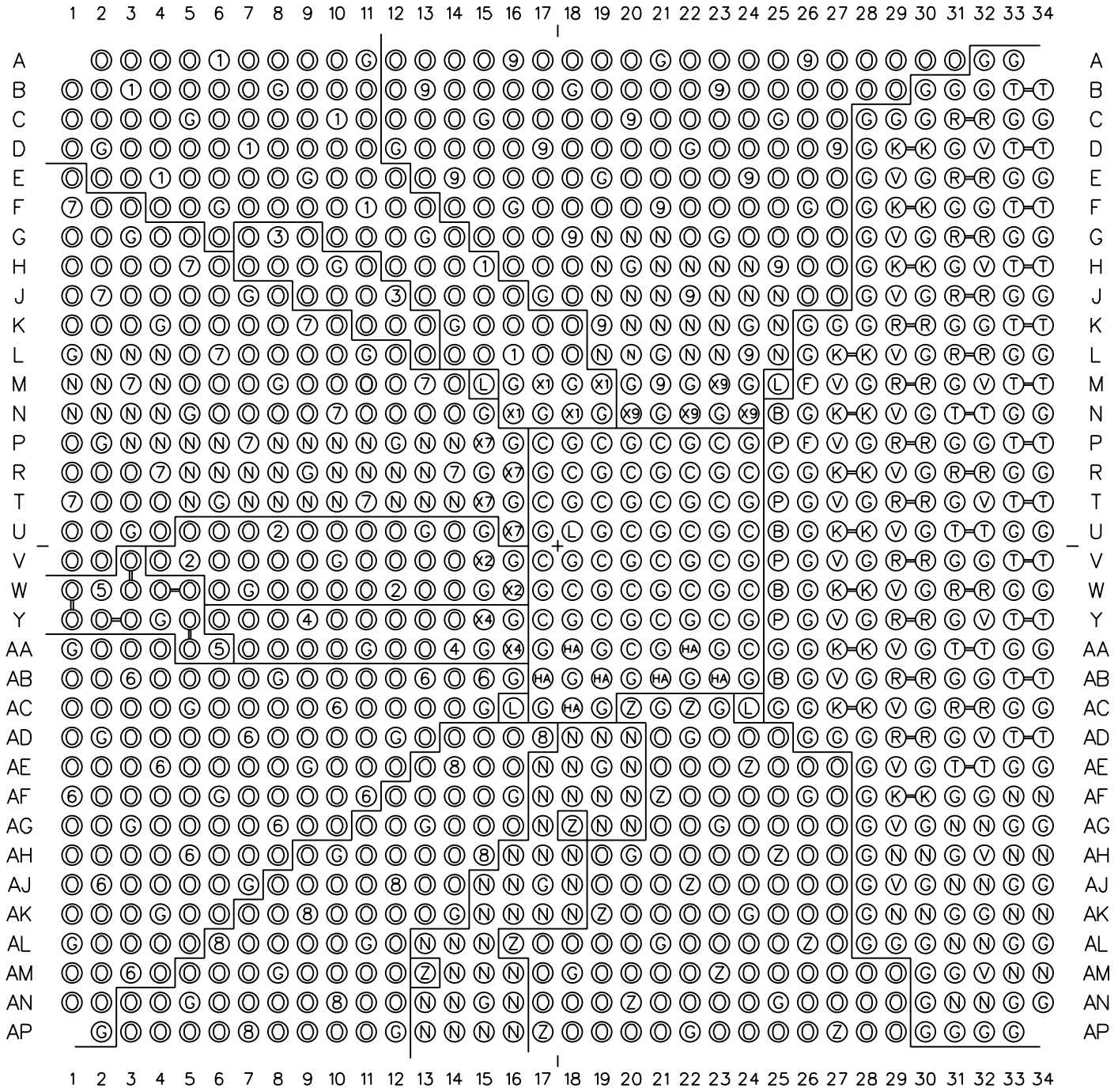
TOMCat Connections to DK Board Pg 2











MPFS250T-1FCG1152I

TOP VIEW

C --> CORE 1V05

L --> PLL & PNVM 2V5

HA --> PROG & HSIO Aux 1V8

V --> XCVR Tx&Rx 1V05

P --> XCVR PLL 2V5

B --> XCVR Clk Buf 2V5

F --> XCVR Clk Ref 10k

K --> XCVR Clk Input

R --> XCVR Rx Input

T --> XCVR Tx Output

N --> No Connection

Z --> Bank 0 VDD

1:9 --> Banks 1:9 VDD

x1, x2, x4, x7, x9 --> Banks 1,2,4,7,9 AUX VDD

DK Drw. 101 Rev. 30-May-2024