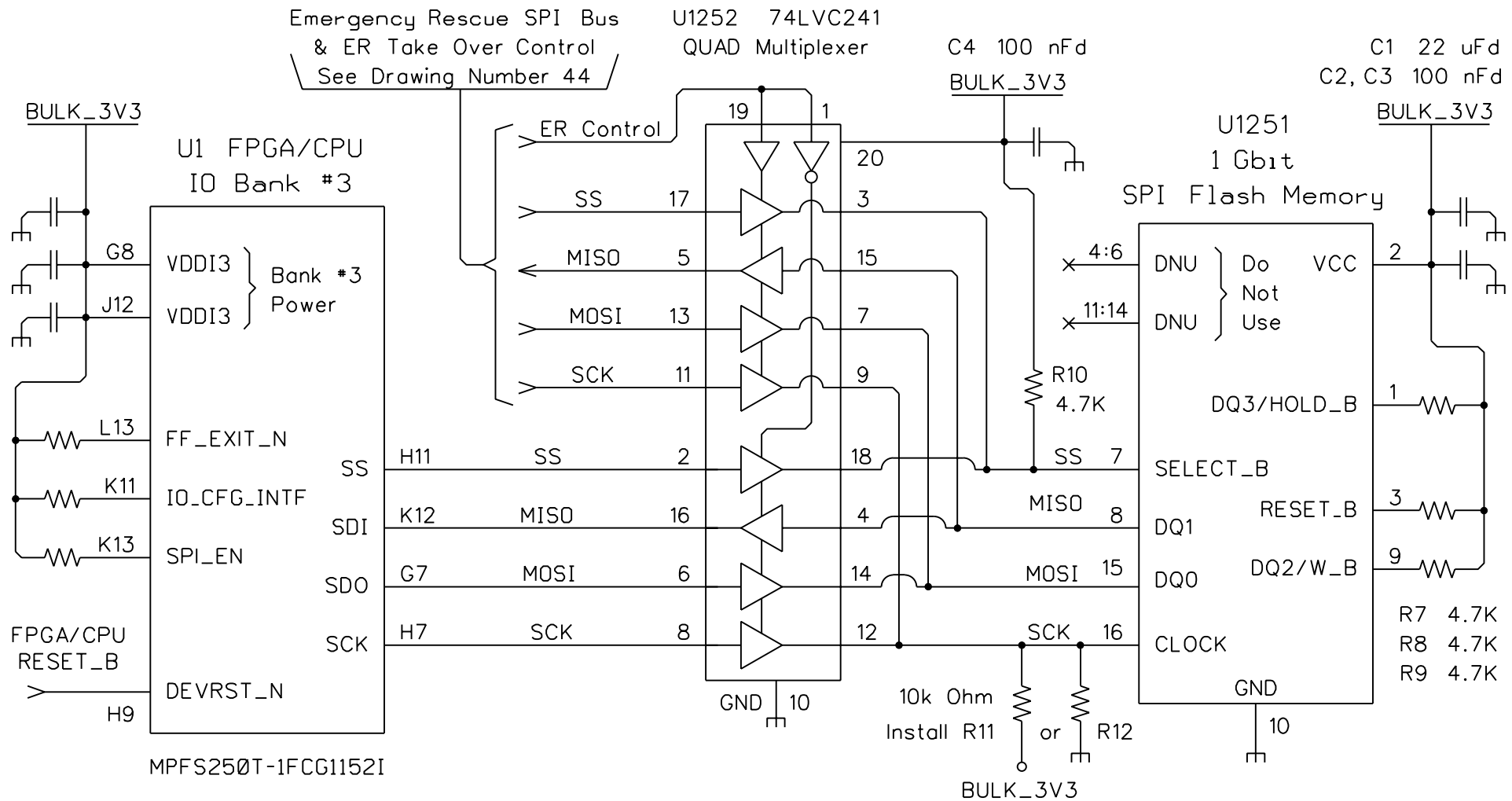


# IO Bank #3 FPGA Boot Memory & Multiplexer



Bank #3  
Pull-Ups

R1351 4.7K  
R1352 4.7K  
R1353 4.7K

DK Drw. 12

ER Control: LOW --> Normal Boot, HI --> Emergency Rescue

Normally the FPGA/CPU System Controller is the SPI Master.

FF\_EXIT\_N is a Reserved Input to the System Controller.

IO\_CFG\_INTF set to 0 for SPI Slave, 1 for SPI Master.

SPI\_EN set to 0 for SPI tri-stated, 1 for SPI Enabled.

Micron  
MT25QL01GBBB8ESF-0SIT

Reference Designators  
Start at 1251

Rev. 19-June-2024