

FPGA Bank 3 JTAG Connection & Buffers

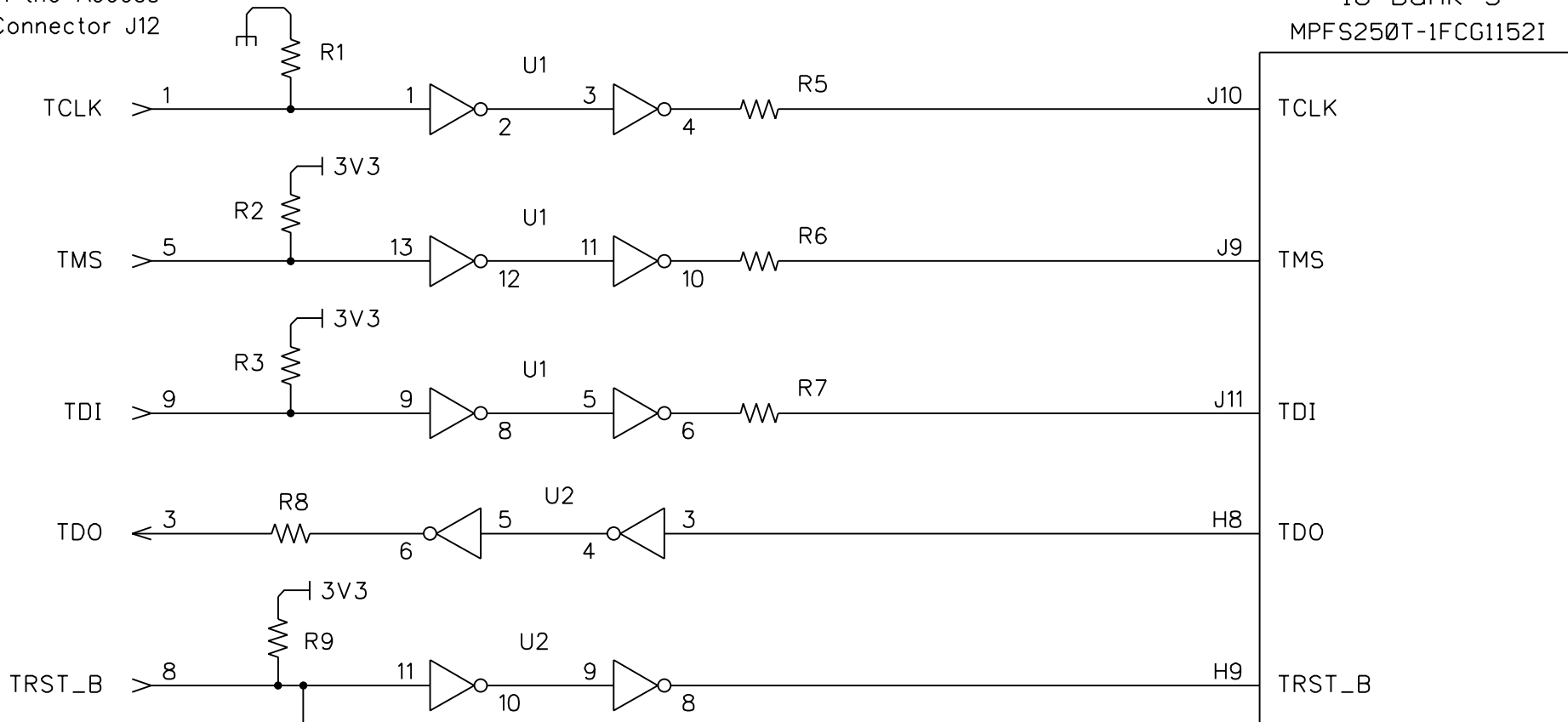
JTAG
First 10 Pins
in the Access
Connector J12

R1 : R4, R9
4.7K Ohm

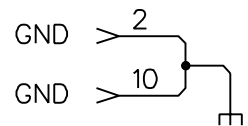
U1401, U1402
74LVC14A

Reference Designators
Start at 1401

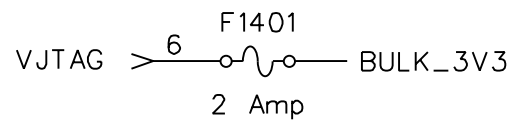
U1 FPGA/CPU
IO Bank 3
MPFS250T-1FCG1152I



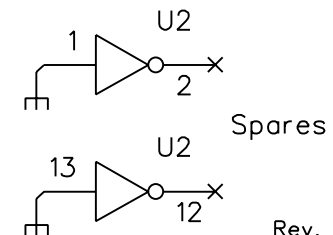
R5 : R8 22 Ohm



No_Conn > 4 x
No_Conn > 7 x



See "Packaging and Pin Descriptions"
page 16 for default signal details.



DK Drw. 13
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