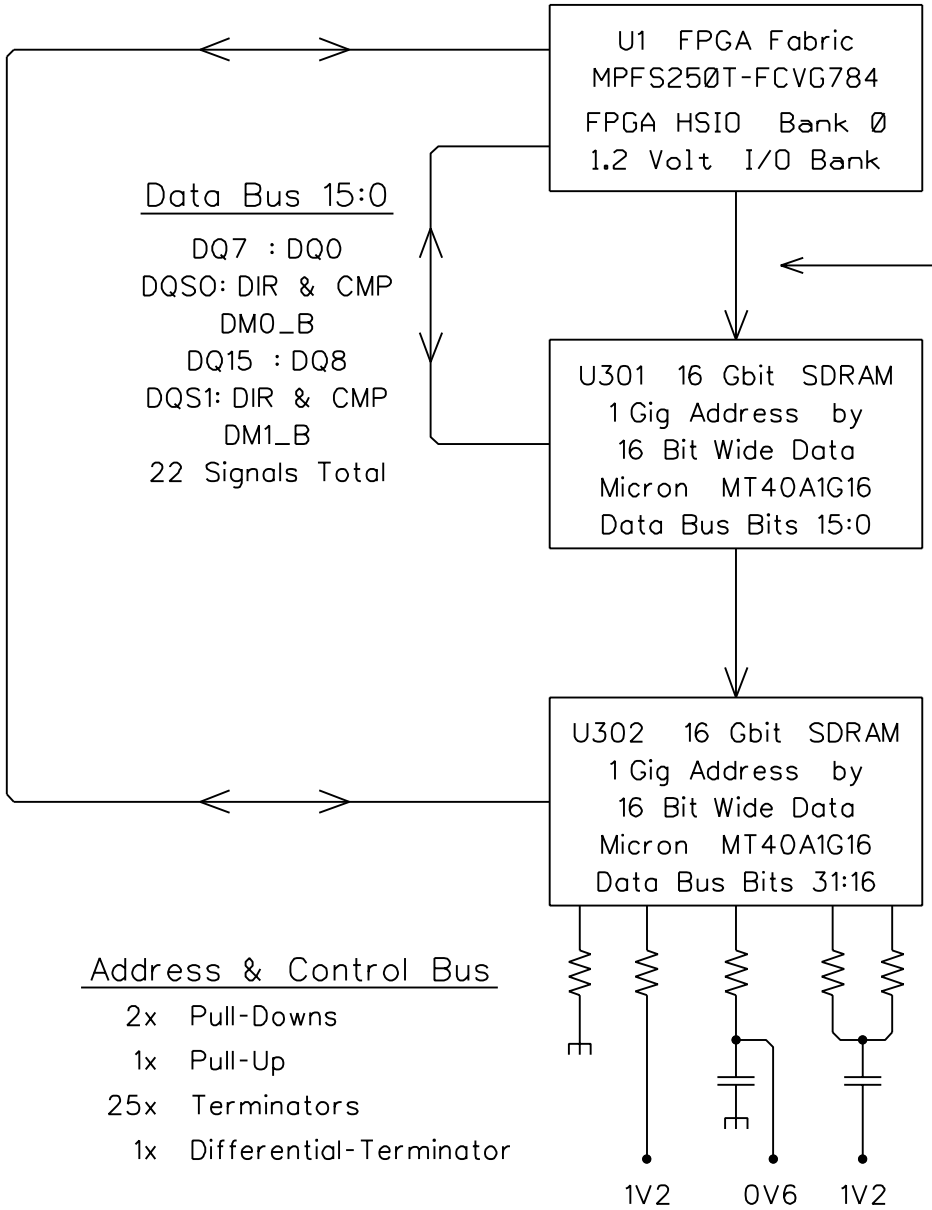
FPGA DDR4 Memory - 4 GBytes - 32 Bit Wide Data



Data Bus 31:16

DQ23 : DQ16
DQS2: DIR & CMP
DM2_B
DQ31 : DQ24
DQS3: DIR & CMP
DM3_B
22 Signals Total

Data Bus 15:0

DQ7 : DQ0
DQS0: DIR & CMP
DM0_B
DQ15 : DQ8
DQS1: DIR & CMP
DM1_B
22 Signals Total

Address & Control Bus

ADRS13 : ADRS0	Term
ADRS14_WE_B	Term
ADRS15_CAS_B	Term
ADRS16_RAS_B	Term
BA1, BA0	Term
BG0	Term
ODT	Term
CLK: DIR & CMP	Diff-Term
CLK_ENB	Term
CS_B	Term
ALERT_B	Pull-Up
PARITY	Term
ACT_B	Term
RESET_B	Pull-Down
TEN	Pull-Down

30 Signals Total

Memory Chip Power Supplies

Core Power	1V2
I/O Power	1V2
Word-Line Power	2V5
Reference Supply	0V6
ZQ Calibration	240 Ohm to GND.

Memory Setup

This is a Rank 1 non-ECC Memory.

The FPGA Bank 0 DDR Memory Controller is used in the Microchip Option North NE-1.

Address & Control Bus

2x	Pull-Downs
1x	Pull-Up
25x	Terminators
1x	Differential-Terminator

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