

# RS-485 Emergency Recovery Page 1

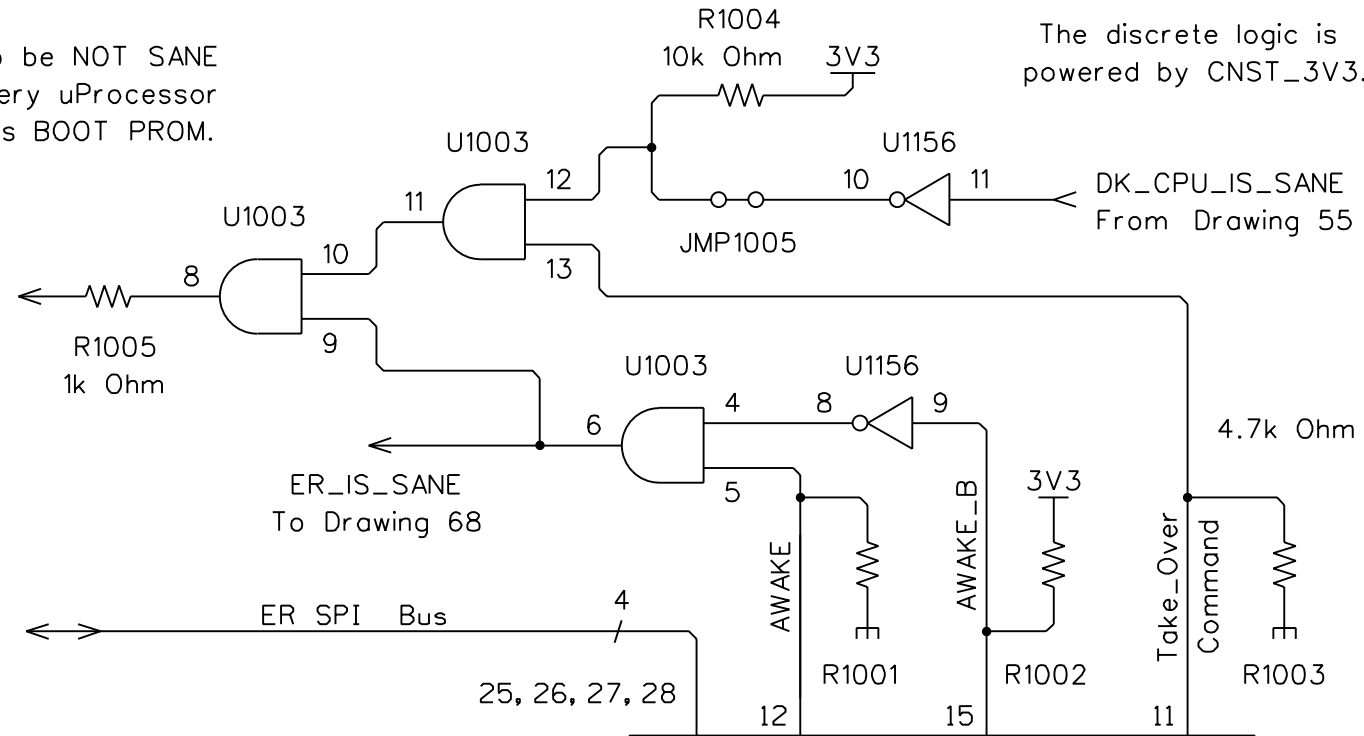
JMP1005 Requires the DK CPU to be NOT SANE in order for the Emergency Recovery uProcessor to take over control of the FPGA's BOOT PROM.

The discrete logic is powered by CNST\_3V3.

ER Take Over Control Signal HI --> Switch the Mux so that the ER's SPI Bus Connects to FPGA Config/Boot Memory

See Drawing 12

ER SPI Bus to the FPGA/CPU Bank 3 SPI Bus Multiplexer 3.3V 4 Wire SPI



This page shows 17 of the I/O Pins that DK uses on the ER uProcessor. None are in Fixed Locations.

