# FPGA/CPU - Power Bus Connections

| DK SUPPLY | Microchip NAME | FUNCTION |
|---|---|---|
| CORE_1V05 | VDD | Core Supply |
| FPGA_1V8 | VDD18 | Prgm & HSIO Aux |
| Analog_2V5 | VDD25 | PLLs and PNVM |
| XCVR_1V05 | VDDA | XCVR Power |
| Analog_2V5 | VDDA25 | XCVR PLLs |
| Analog_2V5 | XCVR_CLK | XCVR Clk Buffers |
| 10k Ohm to Gnd | XCVR_REF | XCVR Clk Ref. |

| DK SUPPLY | | Microchip NAME | FUNCTION |
|---|---|---|---|
| BULK_1V2 | | VDDI0 | I/O Bank 0 FPGA HSIO<br>FPGA DDR4 Memory |
| BULK_3V3<br>BULK_3V3 | * | VDDI1<br>VDDAUX1 | I/O Bank 1 FPGA GPIO<br>DK's 3V3 I/O |
| BULK_3V3<br>BULK_3V3 | * | VDDI2<br>VDDAUX2 | I/O Bank 2 CPU I/O<br>USB UPLI & QSPI |
| BULK_3V3 | | VDDI3 | I/O Bank 3 Controller<br>JTAG & Controller SPI |
| 10k Ohm Gnd<br>10k Ohm Gnd | * | VDDI4<br>VDDAUX4 | I/O Bank 4 CPU I/O<br>Not Used No Power |
| BULK_3V3 | | VDDI5 | I/O Bank 5 CPU SGMII<br>Used only for CPU Clk |
| BULK_1V2 | | VDDI6 | I/O Bank 6 CPU DDR<br>CPU DDR4 Memory |
| BULK_3V3<br>BULK_3V3 | * | VDDI7<br>VDDAUX7 | I/O Bank 7 FPGA GPIO<br>If Used It's 3V3 |
| 10k Ohm Gnd | | VDDI8 | I/O Bank 8 FPGA HSIO<br>Not Used No Power |
| FPGA_1V8<br>DIGITAL_2V5 | * | VDDI9<br>VDDAUX9 | I/O Bank 9 FPGA GPIO<br>DK's 1V8 I/O |

* When an FPGA GPIO Bank or a CPU IO Bank operates from 2V5 or 3V3 power then that Bank's Auxiliary supply must come from the same 2V5 or 3V3 bus.

* When an FPGA GPIO Bank or a CPU IO Bank operates from 1V8 or lower voltage power then that Bank's Auxiliary supply must come from the 2V5 bus.

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Do not confuse VDD18 and VDDI8.

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