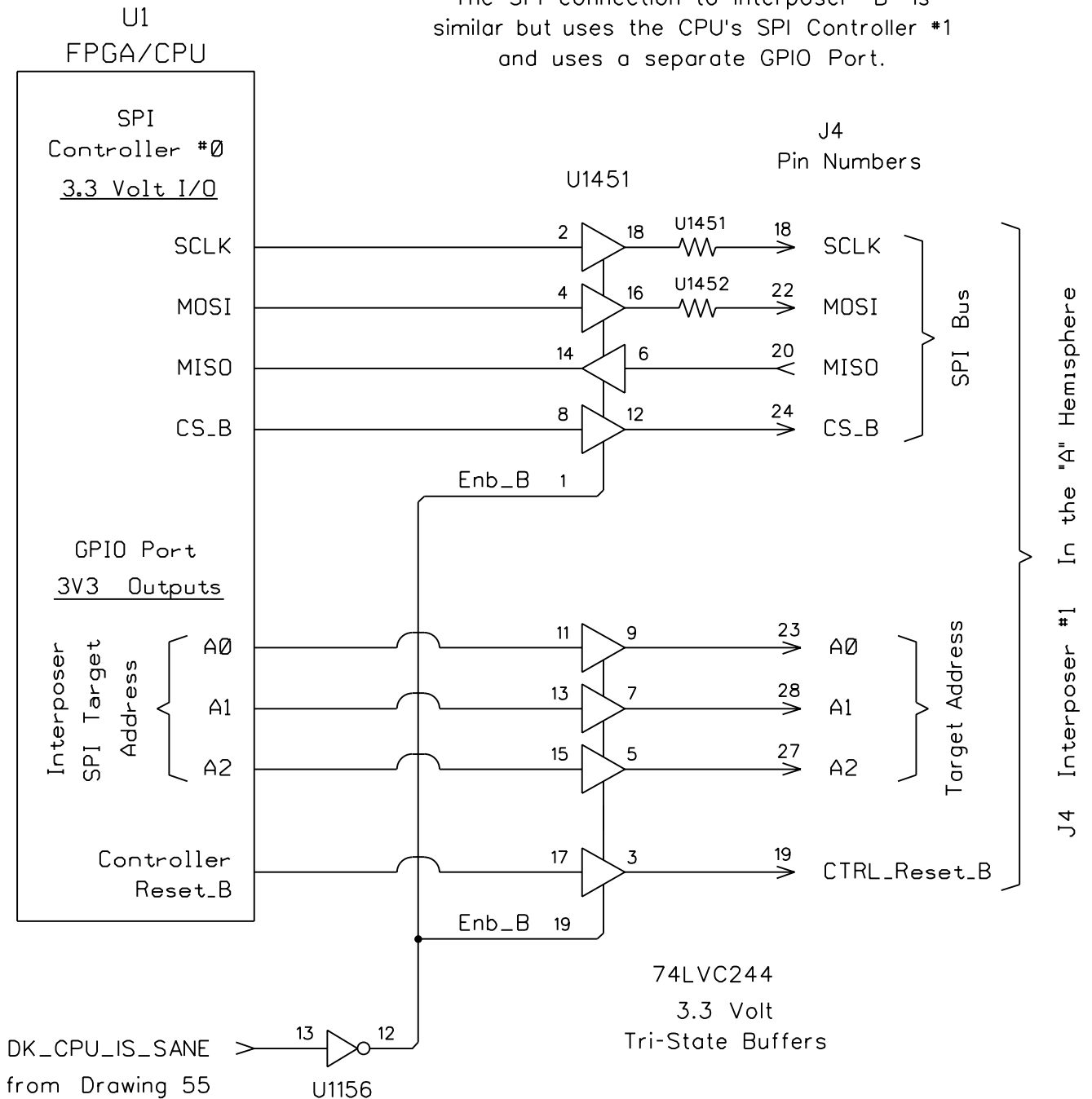


SPI Connection to Interposer "A"

The SPI connection to Interposer "B" is similar but uses the CPU's SPI Controller #1 and uses a separate GPIO Port.



All signals to the Interposer are held in a quiescent state until the DK's CPU is awake and sane.

Not Shown Are the Pull-Up & Pull-Down Resistors:

SCLK & MOSI to the Interposer are Pulled Down: R1461, R1462

MISO to the SPI Controller is Pulled Down: R1463

CS_B to the Interposer is Pulled Up: R1464

Ax & CNTL_Reset_B to the Interposer are Pulled Down: R1465...R1468