

TOMCat Mezzanine Connector J10

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		<u>Function</u>	<u>Pin Num</u>	<u>Pin Num</u>	<u>Function</u>	
		Ground	1	2	3V3 for JTAG	
JTAG Controller on ER	{ ←	TDO	3	4	TCK	← } JTAG Controller on ER
		TMS	5	6	TDI	
		Ground	7	8	Ground	
SGMII Ethernet from DK	{ →	Rx+	9	10	+5V power	
		Rx-	11	12	+5V Power	
		Ground	13	14	Ground	
SGMII Ethernet to DK	{ ←	Tx+	15	16	+5V Power	
		Tx-	17	18	+5V Power	
		Ground	19	20	Ground	
1V8 CMOS	{ ×	Spare	21	22	CFG1	→ } DK FPGA 1V8 CMOS
		100 Hz	23	24	CFG0	
		Ground	25	26	Ground	
AD9546 M0 1V8 CMOS	{ ×	100 Hz	27	28	100 Hz-	→ } DK FPGA LVDS
		PPS	29	30	100 Hz+	
		Ground	31	32	Ground	
LVDS	{ ×	SPARE-	33	34	125 MHz-	→ } DK FPGA LVDS
		SPARE+	35	36	125 MHz+	
		Ground	37	38	Ground	
UART from ER	{ →	Rx UART-	39	40	PPS-	→× } LVDS
		Rx UART+	41	42	PPS+	
		Ground	43	44	Ground	
UART to ER	{ ←	Tx UART-	45	46	125 MHz-	→ } AD9546 REF_A LVDS
		Tx UART+	47	48	125 MHz+	
		Ground	49	50	Ground	

Spare TOMcat pins will be connected to DK FPGA where possible.