ICECUBE DIGITAL OPTICAL MODULE
MAIN BOARD VERSION 5.1

11/19/04

P/N LBNL-ICE3-DOMMB REV 5.1C

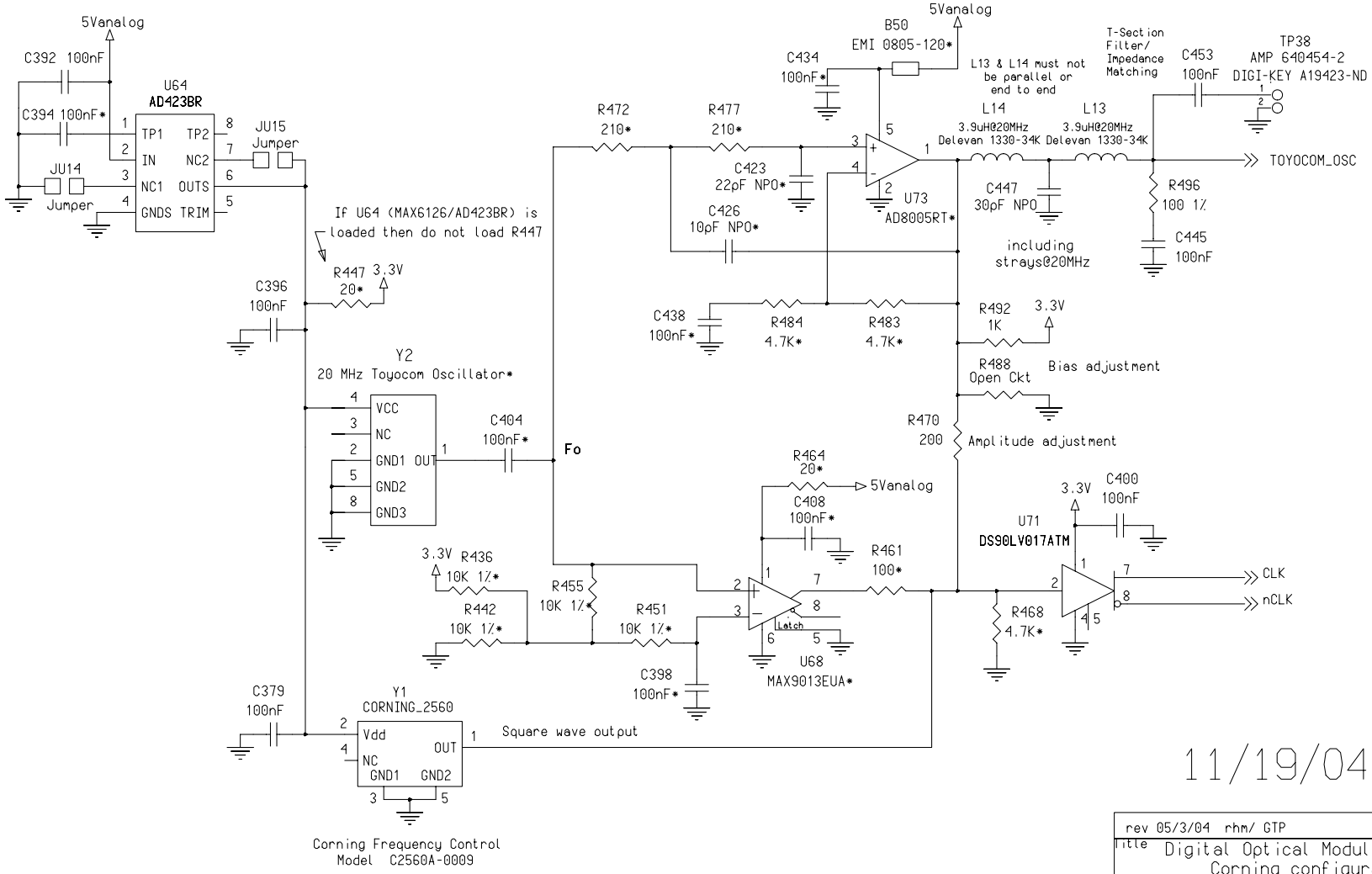
rev 05/3/04 rhm/ GTP		
Title: IceCube - Digital Optical Module - Print List		
Size: B	Document Number: main_board_vsn5.1 31Y083-S1	Vsn.: 5.1
Date:	Sheet of	

ICECUBE DIGITAL OPTICAL MODULE
MAIN BOARD VERSION 5.1

SEE FABRICATION DRAWINGS

11/19/04

Title: IceCube - Digital Optical Module - Layer Stack up			
Size: B	Document Number: main_board_vsn5.1 31Y083-S2		Vsn.: 5.1
Date:		Sheet of	


5Vanalog
C392 100nF
C394 100nF*
U64
AD423BR
TP1
TP2
IN
NC2
NC1
OUTS
GNDS
TRIM
JU14
Jumper
JU15
Jumper
If U64 (MAX6126/AD423BR) is loaded then do not load R447
R447 3.3V
20*
C396
100nF
Y2
20 MHz Toyocom Oscillator*
VCC
NC
GND1
OUT
GND2
GND3
C404
100nF*
Fo
C379
100nF
Y1
CORNING_2560
Vdd
OUT
NC
GND1
GND2
Square wave output
Corning Frequency Control
Model C2560A-0009
B50
EMI 0805-120*
C434
100nF*
R472
210*
R477
210*
C423
22pF NPO*
C426
10pF NPO*
U73
AD8005RT*
L14
3.9uH@20MHz
Delevan 1330-34K
L13
3.9uH@20MHz
Delevan 1330-34K
L13 & L14 must not be parallel or end to end
T-Section Filter/ Impedance Matching
C453
100nF
TP38
AMP 640454-2
DIGI-KEY A19423-ND
TOYOCOM_OSC
C447
30pF NPO
including strays@20MHz
R496
100 1%
C445
100nF
C438
100nF*
R484
4.7K*
R483
4.7K*
R492
1K
3.3V
R488
Open Ckt
Bias adjustment
R470
200
Amplitude adjustment
R464
20*
5Vanalog
C408
100nF*
R461
100*
3.3V R436
10K 1%*
R455
10K 1%*
R442
10K 1%*
R451
10K 1%*
C398
100nF*
Latch
U68
MAX9013EUA*
3.3V
C400
100nF
U71
DS90LV017ATM
CLK
nCLK
R468
4.7K*
* = DNL
11/19/04
rev 05/3/04 rhm/ GTP
Title
Digital Optical Module Crystal
Corning configuration
Size
B
Document Number
main_board_vsn5.1
31Y083-S3
of 14
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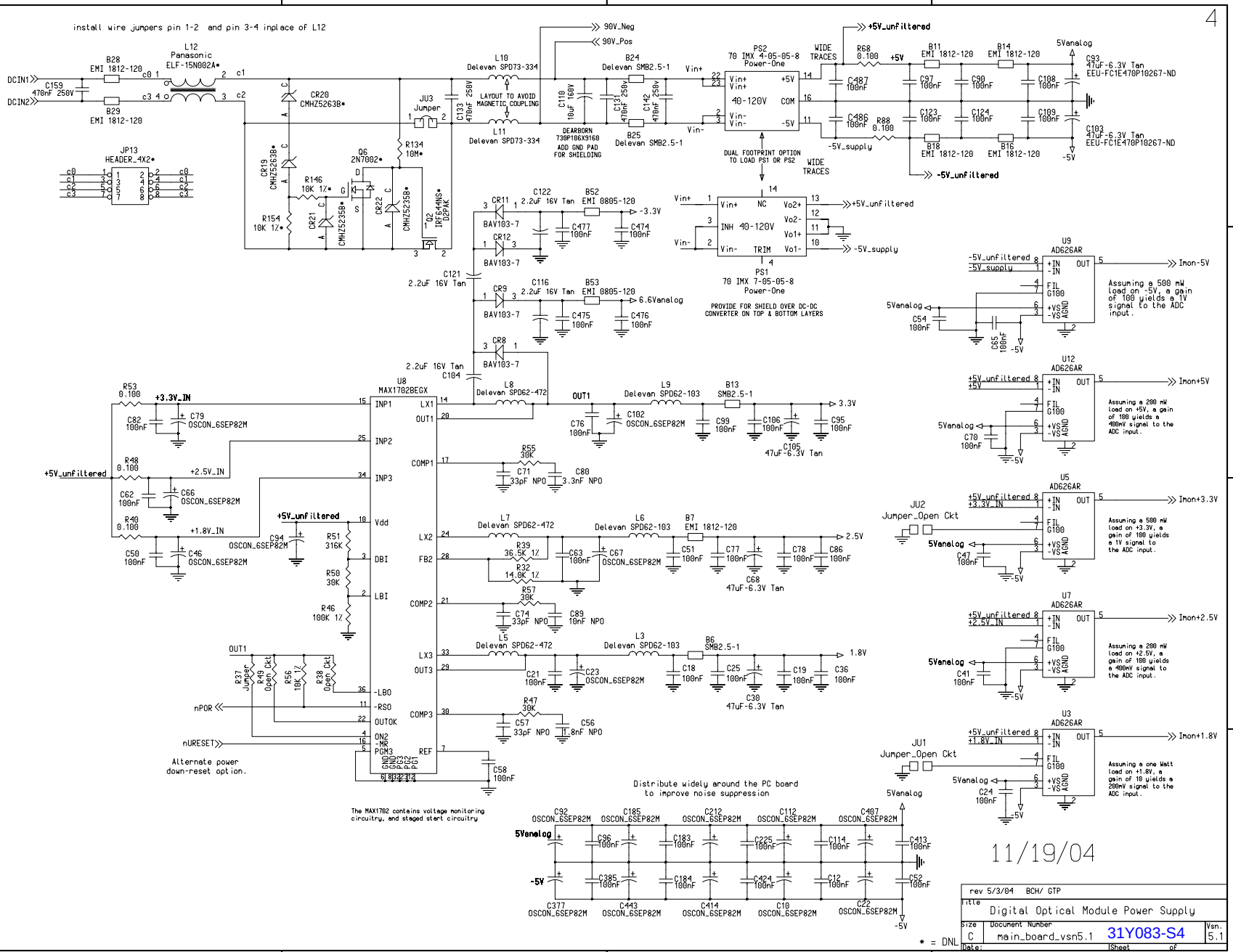
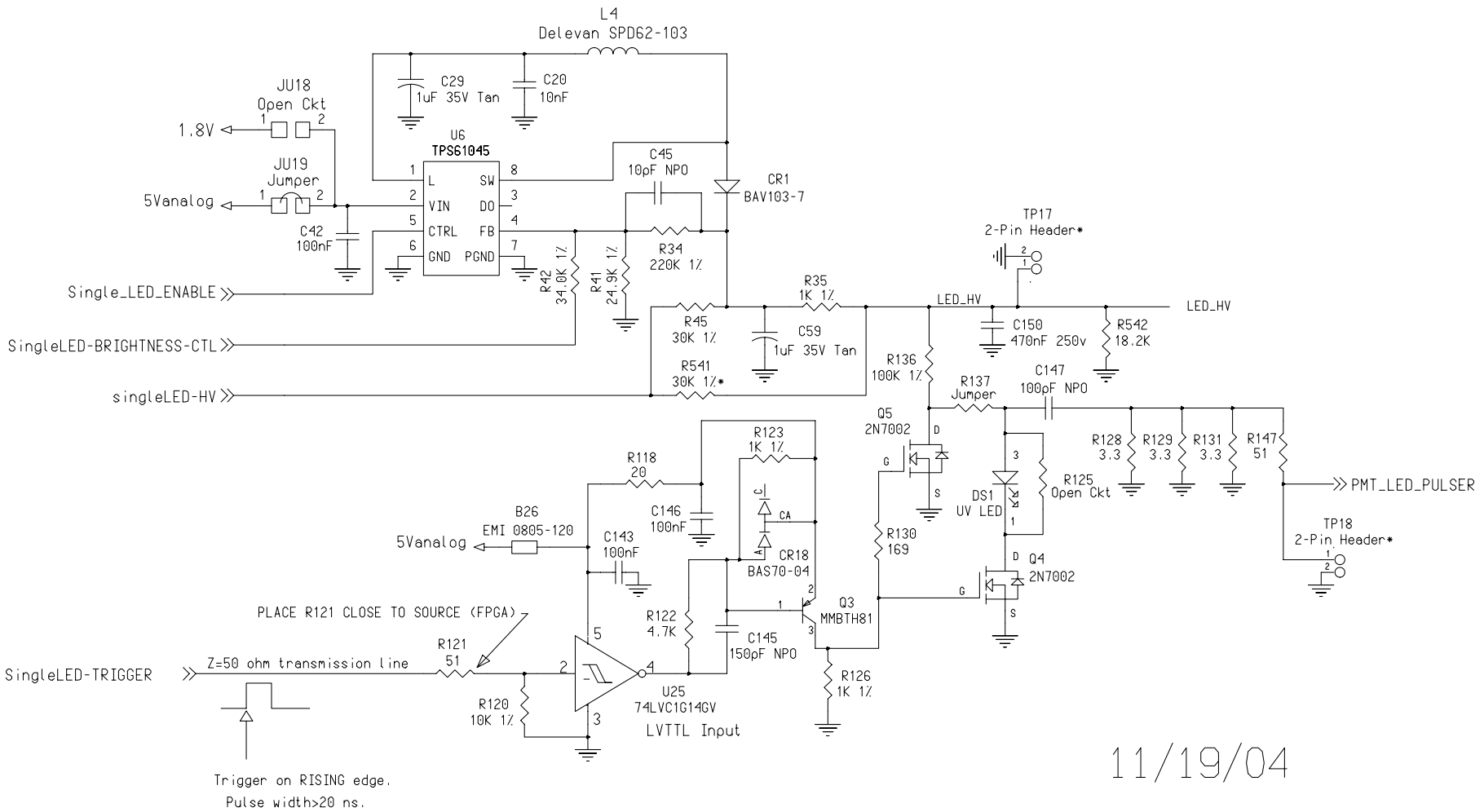

install wire jumpers pin 1-2 and pin 3-4 inplace of L12
L12 Panasonic ELF-15N002A*
DCIN1
DCIN2
C159 470nF 250V
B28 EMI 1812-120
B29 EMI 1812-120
CR20 CMHZ5263B*
JU3 Jumper
JP13 HEADER_4X2*
CR19 CMHZ5263B*
CR21 CMHZ5235B*
CR22 CMHZ5235B*
R146 10K 1%*
R154 10K 1%*
R134 10M*
Q6 2N7002*
Q2 IPE64N8S* D2PAK
L10 Delevan SPD73-334
L11 Delevan SPD73-334
LAYOUT TO AVOID MAGNETIC COUPLING
C133 470nF 250V
C110 10uF 160V
DEARBORN 73GP106X9160 ADD GND PAD FOR SHIELDING
B24 Delevan SMB2.5-1
B25 Delevan SMB2.5-1
C137 470nF 250V
C142 470nF 250V
90V_Neg
90V_Pos
Vin+
Vin-
PS2 70 IMX 4-05-05-8 Power-One
Vin+ +5V
40-120V COM
Vin- -5V
DUAL FOOTPRINT OPTION TO LOAD PS1 OR PS2
WIDE TRACES
+5V_unfiltered
-5V_unfiltered
R68 0.100
R88 0.100
+5V
-5V_supply
C487 100nF
C486 100nF
B11 EMI 1812-120
B14 EMI 1812-120
B18 EMI 1812-120
B16 EMI 1812-120
C97 100nF
C90 100nF
C108 100nF
C123 100nF
C124 100nF
C109 100nF
5Vanalog
-5V
C93 47uF-6.3V Tan EEU-FC1E470P10267-ND
C103 47uF-6.3V Tan EEU-FC1E470P10267-ND
CR11 BAV103-7
CR12 BAV103-7
CR9 BAV103-7
CR8 BAV103-7
C122 2.2uF 16V Tan
C116 2.2uF 16V Tan
C121 2.2uF 16V Tan
C104 2.2uF 16V Tan
B52 EMI 0805-120
B53 EMI 0805-120
-3.3V
6.6Vanalog
C477 100nF
C474 100nF
C475 100nF
C476 100nF
PS1 70 IMX 7-05-05-8 Power-One
Vin+ NC Vo2+
INH 40-120V Vo2-
Vo1+
Vin- TRIM Vo1-
PROVIDE FOR SHIELD OVER DC-DC CONVERTER ON TOP & BOTTOM LAYERS
U9 AD626AR
U12 AD626AR
U5 AD626AR
U7 AD626AR
U3 AD626AR
+IN -IN OUT
FIL G100
+VS -VS AGND
Imon-5V
Imon+5V
Imon+3.3V
Imon+2.5V
Imon+1.8V
Assuming a 500 mW load on -5V, a gain of 100 yields a 1V signal to the ADC input.
Assuming a 200 mW load on +5V, a gain of 100 yields a 400mV signal to the ADC input.
Assuming a 500 mW load on +3.3V, a gain of 100 yields a 1V signal to the ADC input.
Assuming a 200 mW load on +2.5V, a gain of 100 yields a 400mV signal to the ADC input.
Assuming a one Watt load on +1.8V, a gain of 10 yields a 200mV signal to the ADC input.
C54 100nF
C55 100nF
C70 100nF
C47 100nF
C41 100nF
C24 100nF
JU2 Jumper_Open Ckt
JU1 Jumper_Open Ckt
U8 MAX1702BEGX
INP1 INP2 INP3 Vdd DBI LBI -LBO -RSO OUTOK ON2 -M5 PGM3 REF LX1 OUT1 COMP1 LX2 FB2 COMP2 LX3 OUT3 COMP3 GND
R53 0.100
R48 0.100
R40 0.100
R46 100K 1%
R51 316K
R50 30K
R55 30K
R57 30K
R47 30K
R32 14.0K 1%
R39 36.5K 1%
R37 Jumper
R49 Open Ckt
R56 10K 1%
R38 Open Ckt
+3.3V_IN
+2.5V_IN
+1.8V_IN
C82 100nF
C79 OSCON_6SEP82M
C62 100nF
C66 OSCON_6SEP82M
C50 100nF
C46 OSCON_6SEP82M
C94 OSCON_6SEP82M
C71 33pF NPO
C80 3.3nF NPO
C74 33pF NPO
C89 10nF NPO
C57 33pF NPO
C56 1.8nF NPO
C58 100nF
L8 Delevan SPD62-472
L7 Delevan SPD62-472
L6 Delevan SPD62-103
B7 EMI 1812-120
L5 Delevan SPD62-472
L3 Delevan SPD62-103
B6 SMB2.5-1
B13 SMB2.5-1
OUT1
3.3V
2.5V
1.8V
C76 100nF
C102 OSCON_6SEP82M
C99 100nF
C106 100nF
C95 100nF
C105 47uF-6.3V Tan
C63 100nF
C67 OSCON_6SEP82M
C51 100nF
C77 100nF
C78 100nF
C86 100nF
C68 47uF-6.3V Tan
C21 100nF
C23 OSCON_6SEP82M
C18 100nF
C25 100nF
C19 100nF
C36 100nF
C30 47uF-6.3V Tan
nPOR
nURESET
Alternate power down-reset option.
The MAX1702 contains voltage monitoring circuitry, and staged start circuitry
Distribute widely around the PC board to improve noise suppression
C92 OSCON_6SEP82M
C185 OSCON_6SEP82M
C212 OSCON_6SEP82M
C112 OSCON_6SEP82M
C407 OSCON_6SEP82M
C96 100nF
C183 100nF
C225 100nF
C114 100nF
C413 100nF
C385 100nF
C184 100nF
C424 100nF
C12 100nF
C52 100nF
C377 OSCON_6SEP82M
C443 OSCON_6SEP82M
C414 OSCON_6SEP82M
C10 OSCON_6SEP82M
C22 OSCON_6SEP82M
* = DNL
11/19/04
rev 5/3/04 BCH/ GTP
Title
Digital Optical Module Power Supply
Size C
Document Number main_board_vsn5.1
31Y083-S4
Vsn. 5.1
Date:
Sheet of


L4
Delevan SPD62-103
C29
1uF 35V Tan
C20
10nF
JU18
Open Ckt
1.8V
JU19
Jumper
5Vanalog
U6
TPS61045
L
VIN
CTRL
GND
SW
DO
FB
PGND
C45
10pF NPO
CR1
BAV103-7
C42
100nF
R42
34.0K 1%
R41
24.9K 1%
R34
220K 1%
Single_LED_ENABLE
SingleLED-BRIGHTNESS-CTL
singleLED-HV
R45
30K 1%
R541
30K 1%*
C59
1uF 35V Tan
R35
1K 1%
LED_HV
TP17
2-Pin Header*
C150
470nF 250v
R542
18.2K
LED_HV
R136
100K 1%
R137
Jumper
C147
100pF NPO
Q5
2N7002
R123
1K 1%
R118
20
C146
100nF
B26
EMI 0805-120
5Vanalog
C143
100nF
CR18
BAS70-04
R128
3.3
R129
3.3
R131
3.3
R147
51
R125
Open Ckt
DS1
UV LED
PMT_LED_PULSER
TP18
2-Pin Header*
R130
169
Q4
2N7002
Q3
MMBTH81
PLACE R121 CLOSE TO SOURCE (FPGA)
R121
51
SingleLED-TRIGGER
Z=50 ohm transmission line
R122
4.7K
C145
150pF NPO
R126
1K 1%
R120
10K 1%
U25
74LVC1G14GV
LVTTL Input
Trigger on RISING edge.
Pulse width>20 ns.
* = DNL
11/19/04
rev 05/3/04 BCH/ GTP
Title
Digital Optical Module Single LED
Size
B
Document Number
main_board_vsn5.1
31Y083-S5
Vsn.
5.1
Date:
Sheet
of

An address space of 16 registers

DOM SERVICE MODE

Add jumper to identify card as TYPE B

B = Unterminated

Place near outside egde of board

* = DNL

nCE = pull-down
nCEO = open ckt
TRST = pull-up
TDI = pull-up
TMS = pull-up
TCK = pull-up
nSTATUS = pull-up
CONF_DONE = pull-up
nCONFIG = pull-up

Service Connector for the convenience of software programmers. Utilizes multifunction pins.

For bypassing the EPC2, jumper center to bridging position, pin 1 to pin 2. To put EPC2 into circuit, jumper pin1 to pin2, and pin2 to pin 4.

If it is found that the configuration is correct, JU11 and JU12 can be installed during manufacture.

PLACE CPLD AND CPU CONNECTORS AT THE EDGE OF BOARD

11/19/04

rev 05/3/04 rhm/ GTP

Title: Digital Optical Module CPU

Size	Document Number	Rev.
D	main_board_vsn5.1	5.1

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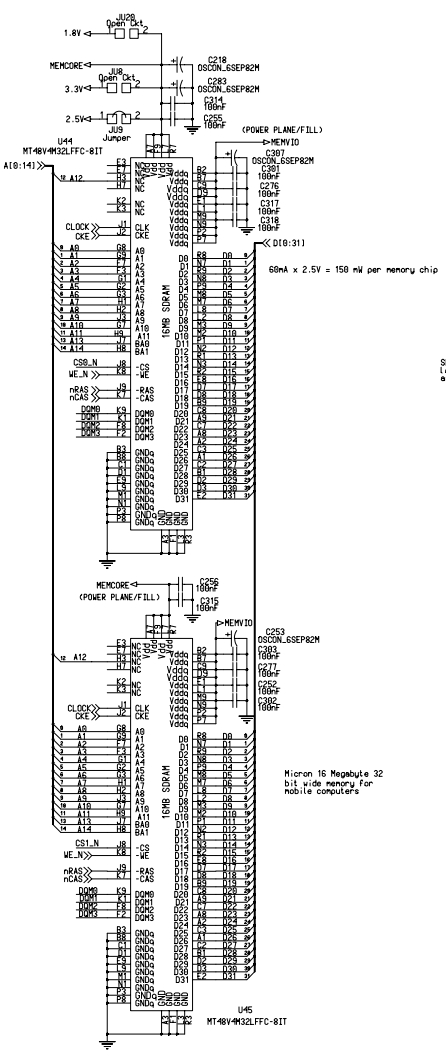
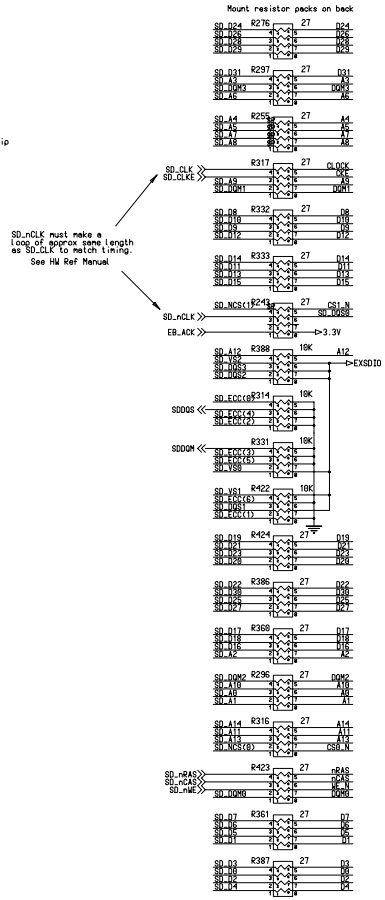
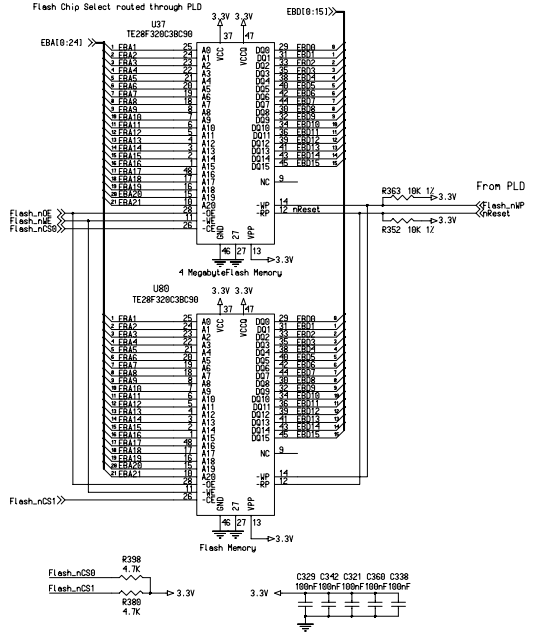
Date: Sheet of





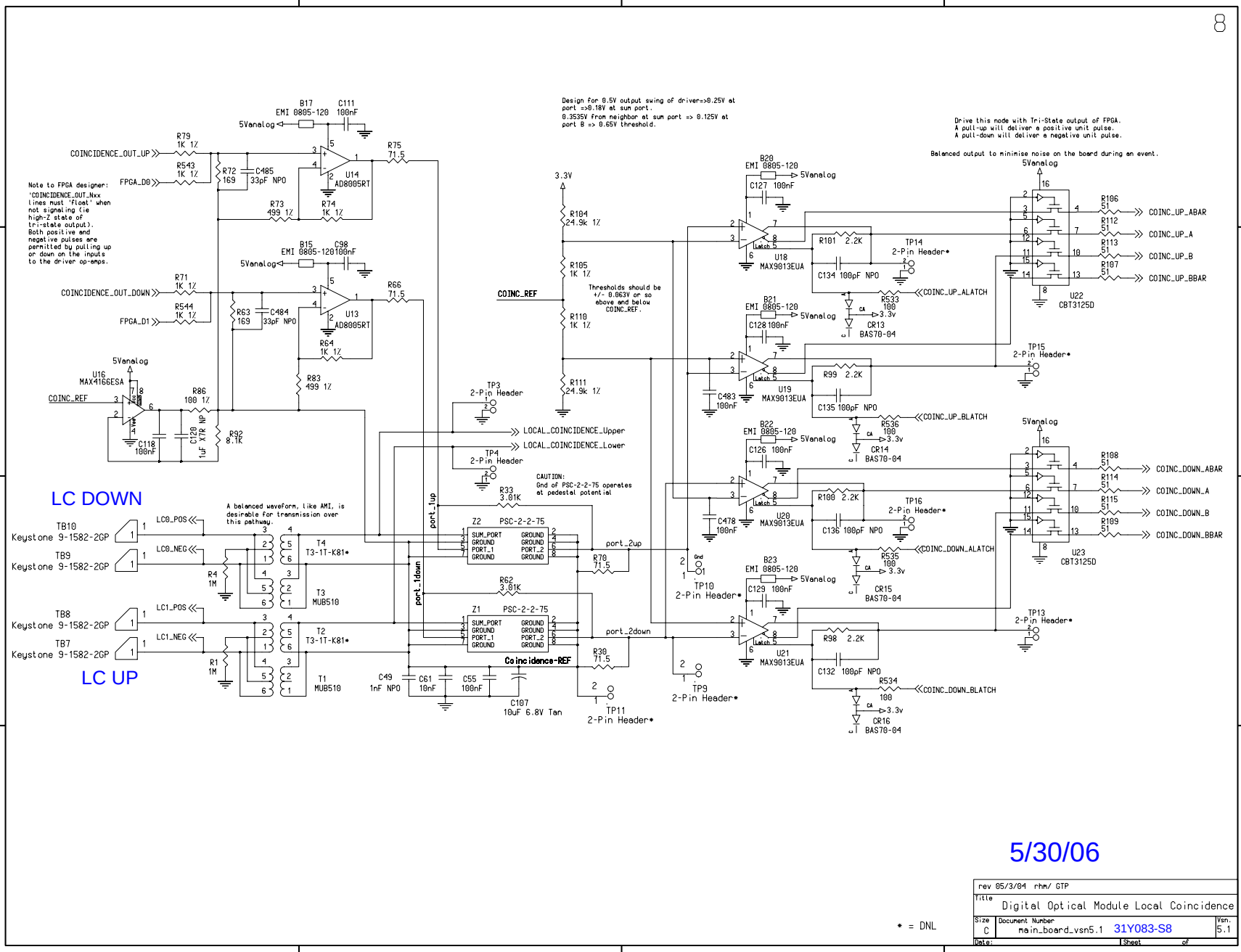


rhm 9/24 changed to EXSDIO for fixed resistors

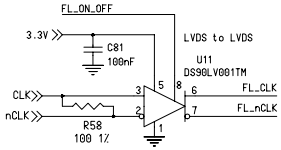
11/19/04

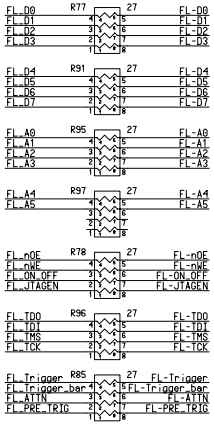
* =DNL

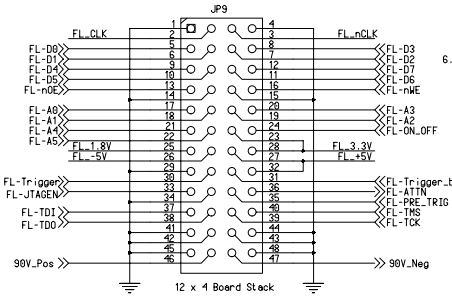
rev 05/3/04 rhm/ GTP		
Title: Digital Optical Module Memory		
Size: D	Document Number: main_board_vsn5.1 31Y083-S7	Vsn.: 5.1
Date:	Sheet of	


8
Design for 0.5V output swing of driver=>0.25V at port =>0.18V at sum port.
0.3535V from neighbor at sum port => 0.125V at port B => 0.65V threshold.
Drive this node with Tri-State output of FPGA.
A pull-up will deliver a positive unit pulse.
A pull-down will deliver a negative unit pulse.
Balanced output to minimise noise on the board during an event.
Note to FPGA designer:
'COINCIDENCE_OUT_Nxx lines must 'Float' when not signaling (ie high-Z state of tri-state output). Both positive and negative pulses are permitted by pulling up or down on the inputs to the driver op-amps.
COINCIDENCE_OUT_UP
COINCIDENCE_OUT_DOWN
FPGA_D0
FPGA_D1
5Vanalog
3.3V
COINC_REF
Thresholds should be +/- 0.063V or so above and below COINC_REF.
LOCAL_COINCIDENCE_Upper
LOCAL_COINCIDENCE_Lower
CAUTION: Gnd of PSC-2-2-75 operates at pedestal potential
A balanced waveform, like AMI, is desirable for transmission over this pathway.
LC DOWN
LC UP
LC0_POS
LC0_NEG
LC1_POS
LC1_NEG
port_1up
port_1down
port_2up
port_2down
Coincidence-REF
COINC_UP_ABAR
COINC_UP_A
COINC_UP_B
COINC_UP_BBAR
COINC_DOWN_ABAR
COINC_DOWN_A
COINC_DOWN_B
COINC_DOWN_BBAR
COINC_UP_ALATCH
COINC_UP_BLATCH
COINC_DOWN_ALATCH
COINC_DOWN_BLATCH
* = DNL
5/30/06
rev 05/3/04 rhm/ GTP
Digital Optical Module Local Coincidence
main_board_vsn5.1
31Y083-S8
5.1

9/24 rhm change flsher pin 32 to +5v and pin 23 to 3.3V

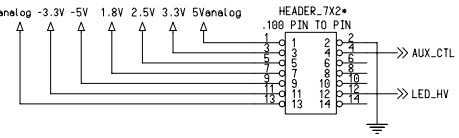




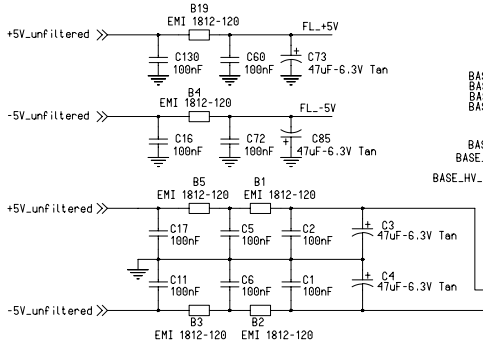


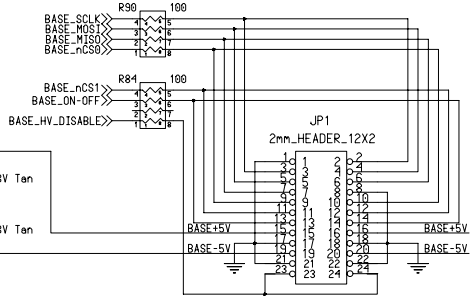
Looking down on the top side of the DOM main PCB the pin pattern will look like the image above

ESQT-112-02-L-Q-078



Mount this connector near the edge of the board.

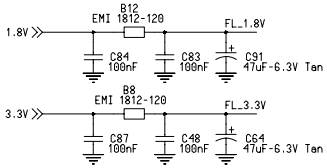


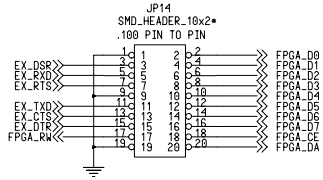


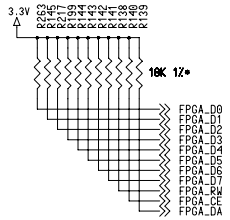
PMT-Power-Supply
2mm header

Should be STMM-112-02-S-D for EMCO base
Should be STMM-110-02-S-D for ISEG base
(24 pin for EMCO, 20 pin for ISEG)

1 GND
2 SCK - Serial clock
3 SCK
4 MOSI -Serial data in
5 MOSI
6 MISO - Serial data out
7 MISO
8 GND
9 CS0 (DAC) - Chip select for DAC
10 CS0
11 CS1 (ADC) - Chip select for ADC
12 CS1
13 ON/OFF - Power supply enable/disable
14 ON/OFF
15 +5V - Main power
16 +5V
17 GND
18 GND
19 -5V - Main power
20 -5V
20 GND
21 GND
23 BASE_HV_DISABLE
24 BASE_HV_DISABLE







* = DNL

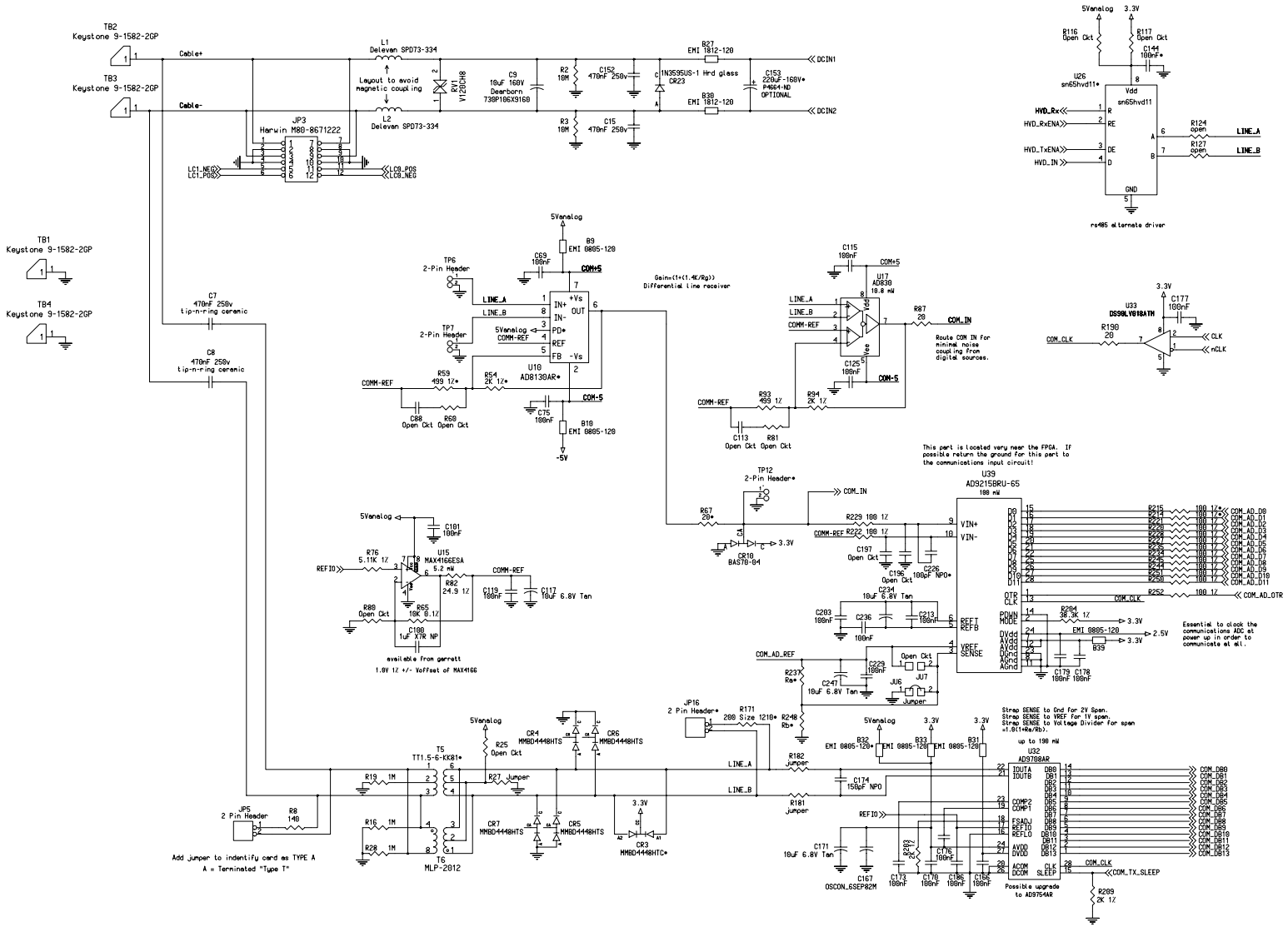
11/19/04

rev 05/3/04 rhm/ GTP

Title: Off-Board Subsystems

Size: C | Document Number: main_board_vsn5.1 31Y083-S9 | Vsn.: 5.1

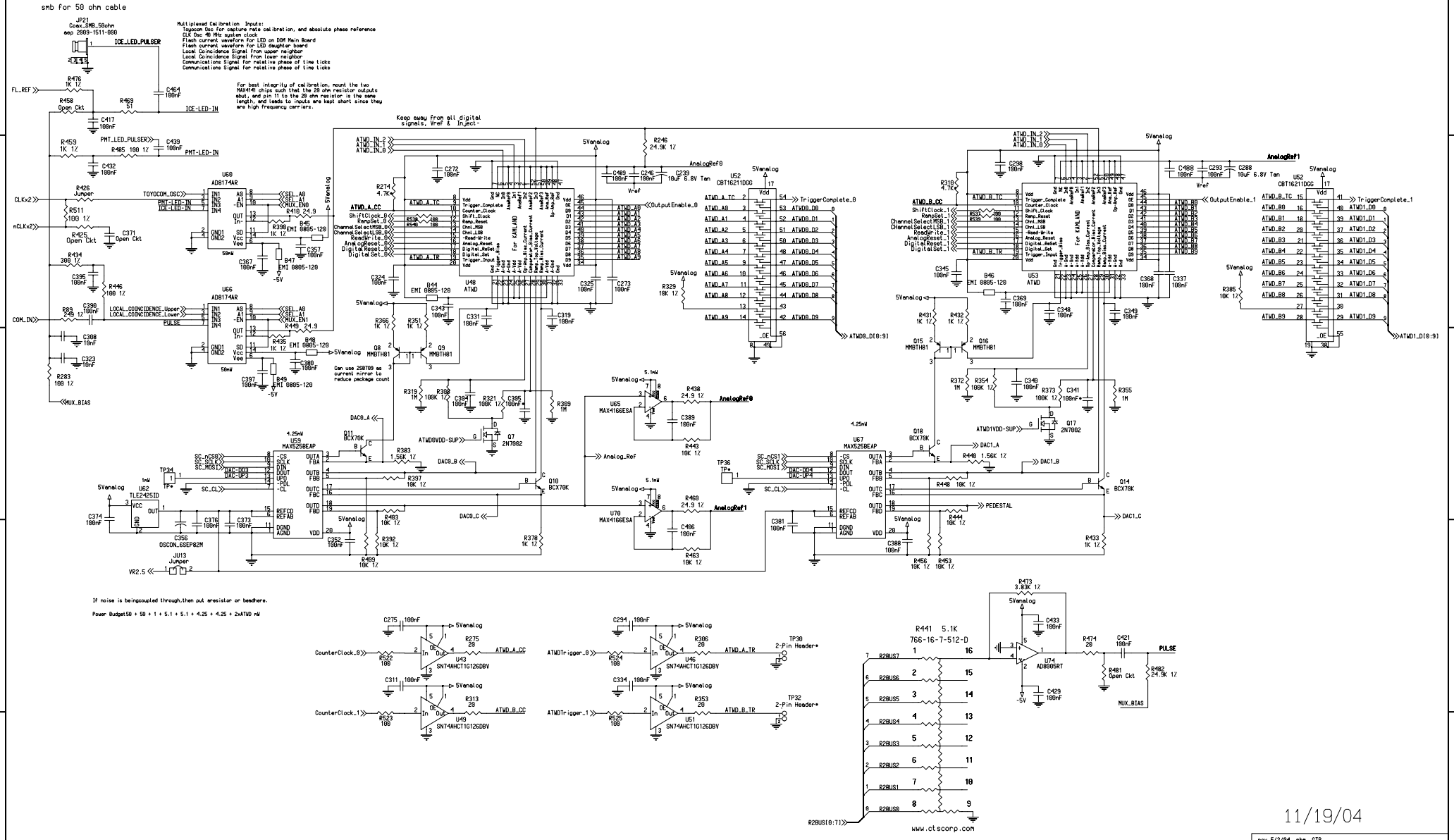
Date: | Sheet of

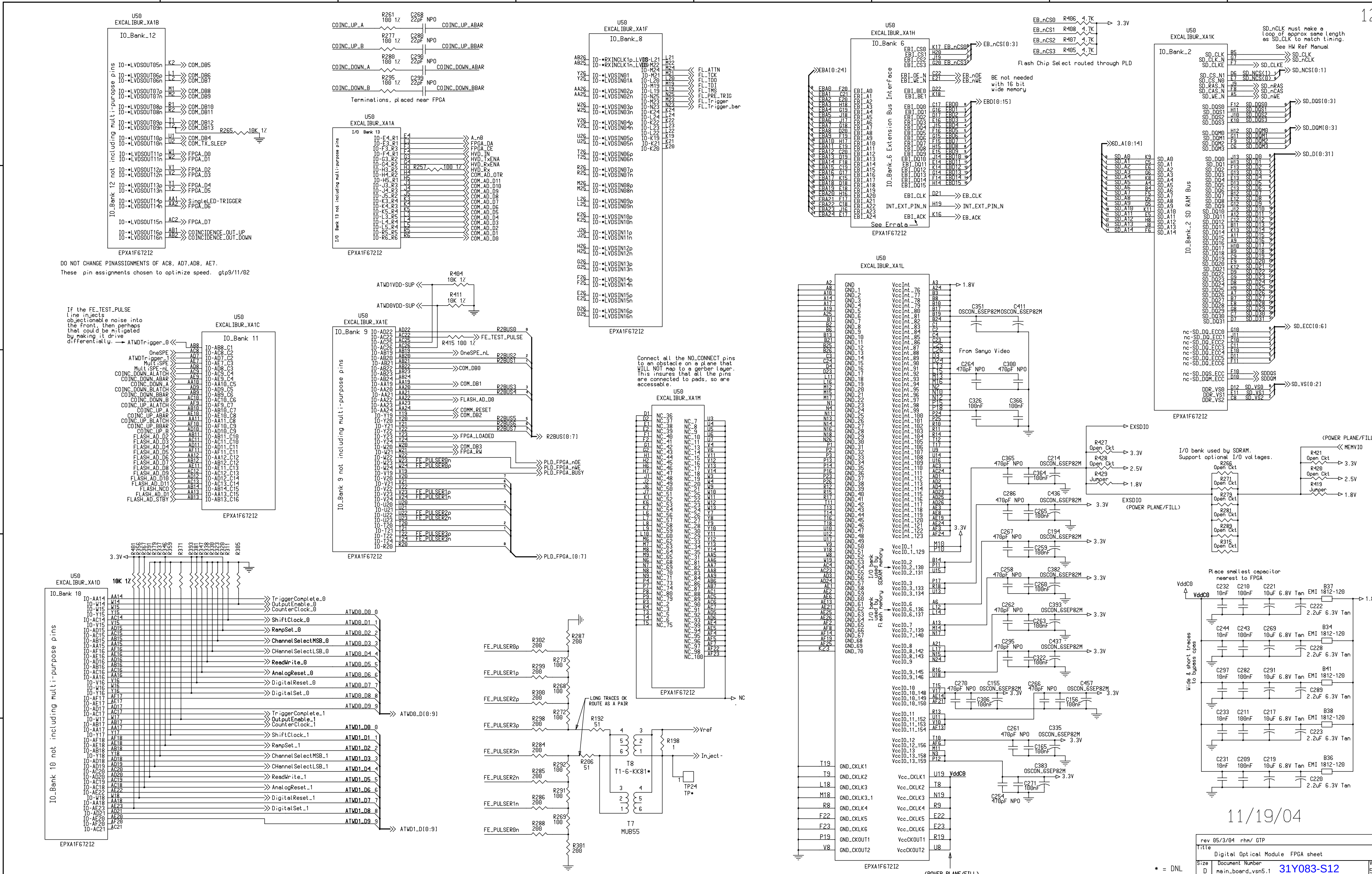


12/4/04

* = DNL

rev 05/3/04 BCH/ GTP			
Title: Digital Optical Module Communication			
Size: C	Document Number: main_board_vsn5.1	31Y083-S10	Vsn.: 5.1
Date:	Sheet of		


smb for 50 ohm cable
JP21
Coax_SMB_50ohm
eep 2009-1511-000
ICE_LED_PULSER
Multiplexed Calibration Inputs:
Tagacom Osc for capture rate calibration, and absolute phase reference
CLK Osc 40 MHz system clock
Flash current waveform for LED on DOM Main Board
Flash current waveform for LED daughter board
Local Coincidence Signal from upper neighbor
Local Coincidence Signal from lower neighbor
Communications Signal for relative phase of time ticks
Communications Signal for relative phase of time ticks
For best integrity of calibration, mount the two MAX4141 chips such that the 20 ohm resistor outputs abut, and pin 11 to the 20 ohm resistor is the same length, and leads to inputs are kept short since they are high frequency carriers.
Keep away from all digital signals, Vref & Inject-
FL_REF
R476 1K 1Z
R458 Open Ckt
R469 51
C464 100nF
C417 100nF
ICE-LED-IN
PMT_LED_PULSER
R459 1K 1Z
R485 100 1Z
PMT-LED-IN
C439 100nF
C432 100nF
CLKx2
R426 Jumper
R511 100 1Z
nCLKx2
C425 Open Ckt
C371 Open Ckt
R434 300 1Z
C395 100nF
R446 100 1Z
COM_IN
R83 249 1Z
C390 100nF
C308 10nF
C323 10nF
R283 100 1Z
MUX_BIAS
U66
AD8174AR
LOCAL_COINCIDENCE_Upper
LOCAL_COINCIDENCE_Lower
PULSE
SEL_A0
SEL_A1
MUX_EN1
R449 24.9
R435 1K 1Z
EMI 0805-120
B48
B49
C397 100nF
C389 100nF
-5V
U69
TOYOCOM_OSC
PMT-LED-IN
ICE-LED-IN
R410 24.9
R396 1K 1Z
B45
B47
C367 100nF
C357 100nF
U48
ATWD
ATWD_A_TC
ATWD_A_CC
ATWD_A_TR
ShiftClock_0
RampSet_0
ChannelSelectMSB_0
ChannelSelectLSB_0
ReadWrite_0
AnalogReset_0
DigitalReset_0
DigitalSet_0
R274 4.7K
R538 499
R540 100
ATWD_IN_2
ATWD_IN_1
ATWD_IN_0
C272 100nF
C324 100nF
C343 100nF
C331 100nF
C319 100nF
C325 100nF
C273 100nF
B44
R366 1K 1Z
R351 1K 1Z
Q8 MMBTH81
Q9 MMBTH81
Can use 298709 as current mirror to reduce package count
R319 1M
R308 100K 1Z
C304 100nF
R321 100K 1Z
C305 100nF
R309 1M
DAC0_A
DAC0_B
DAC0_C
ATWD0VDD-SUP
Q7 2N7002
Q11 BCX70K
Q10 BCX70K
R383 1.56K 1Z
R397 10K 1Z
U59
MAX5258EAP
4.25mW
SC_nCS0
SC_SCLK
SC_MOSI
DAC-DP3
SC_CL
TP34
TP*
1mW
U62
TLE2425ID
VCC
OUT
GND
C374 100nF
C376 100nF
C373 100nF
C356
OSCON_6SEP82M
JU13
Jumper
VR2.5
R403 10K 1Z
R392 10K 1Z
R409 10K 1Z
C352 100nF
R378 1K 1Z
5Vanalog
R246 24.9K 1Z
C489 100nF
C246 100nF
C239 10uF 6.8V Tan
AnalogRef0
Vref
U52
CBT16211DGG
OutputEnable_0
TriggerComplete_0
ATWD0_D[0:9]
R329 10K 1Z
U65
MAX4166ESA
5.1mW
R438 24.9 1Z
C389 100nF
R443 10K 1Z
Analog_Ref
U70
MAX4166ESA
R469 24.9 1Z
C406 100nF
R463 10K 1Z
AnalogRef1
U67
MAX5258EAP
SC_nCS1
SC_SCLK
SC_MOSI
DAC-DP4
SC_CL
TP36
TPe
C381 100nF
R456 10K 1Z
R453 10K 1Z
C388 100nF
R433 1K 1Z
Q18 BCX70K
Q14 BCX70K
DAC1_A
DAC1_B
DAC1_C
R448 1.56K 1Z
R447 10K 1Z
R444 10K 1Z
PEDESTAL
ATWD1VDD-SUP
Q17 2N7002
R372 1M
R354 100K 1Z
C340 100nF
R373 100K 1Z
C341 100nF*
R355 1M
R431 1K 1Z
R432 1K 1Z
Q15 MMBTH81
Q16 MMBTH81
R310 4.7K
C298 100nF
C488 100nF
C293 100nF
C288 10uF 6.8V Tan
C345 100nF
C369 100nF
C348 100nF
C349 100nF
C368 100nF
C337 100nF
B46
U53
ATWD
ATWD_B_TC
ATWD_B_CC
ATWD_B_TR
ChannelSelectMSB_1
ChannelSelectLSB_1
ReadWrite_1
AnalogReset_1
DigitalReset_1
DigitalSet_1
R537 100
R539 100
OutputEnable_1
TriggerComplete_1
ATWD1_D[0:9]
R385 10K 1Z
If noise is beingcoupled through,then put aresistor or beadhere.
Power Budget5B + 5B + 1 + 5.1 + 5.1 + 4.25 + 4.25 + 2xATWD mW
C275 100nF
R522 100
R275 20
ATWD_A_CC
U43
SN74AHCT1G126DBV
C311 100nF
R523 100
R313 20
ATWD_B_CC
U49
SN74AHCT1G126DBV
C294 100nF
R524 100
R306 20
ATWD_A_TR
U46
SN74AHCT1G126DBV
C334 100nF
R525 100
R353 20
ATWD_B_TR
U51
SN74AHCT1G126DBV
TP30
TP32
2-Pin Header*
R473 3.83K 1Z
C433 100nF
U74
AD8005RT
C429 100nF
R474 20
C421 100nF
PULSE
R481 Open Ckt
R482 24.9K 1Z
MUX_BIAS
R441 5.1K
766-16-7-512-D
R2BUS7
R2BUS6
R2BUS5
R2BUS4
R2BUS3
R2BUS2
R2BUS1
R2BUS8
R2BUS[0:7]
www.ctscorp.com
* = DNL
11/19/04
rev 5/3/04 rhm, GTP
Title
Digital Optical Module ATWD
Size
D
Document Number
main_board_vsn5.1
31Y083-S11
Vsn.
5.1
Date:
Sheet
of


U50
EXCALIBUR_XA1B
IO_Bank_12
DO NOT CHANGE PINASSIGNMENTS OF AC8, AD7,AD8, AE7.
These pin assignments chosen to optimize speed. gtp9/11/02
Terminations, placed near FPGA
U50
EXCALIBUR_XA1A
U50
EXCALIBUR_XA1F
IO_Bank_8
If the FE_TEST_PULSE line injects objectionable noise into the front, then perhaps that could be mitigated by making it drive differentially.
U50
EXCALIBUR_XA1C
IO_Bank 11
U50
EXCALIBUR_XA1E
IO_Bank 9
Connect all the NO_CONNECT pins to an obstacle on a plane that WILL NOT map to a gerber layer. This insures that all the pins are connected to pads, so are accessable.
U50
EXCALIBUR_XA1M
U50
EXCALIBUR_XA1H
IO_Bank 6
See Errata
BE not needed with 16 bit wide memory
Flash Chip Select routed through PLD
U50
EXCALIBUR_XA1L
From Sanyo Video
U50
EXCALIBUR_XA1K
IO_Bank_2
SD_nCLK must make a loop of approx same length as SD_CLK to match timing. See HW Ref Manual
I/O bank used by SDRAM. Support optional I/O voltages.
(POWER PLANE/FILL)
EXSDIO (POWER PLANE/FILL)
Place smallest capacitor nearest to FPGA
Wide & short traces to bypass caps
U50
EXCALIBUR_XA1D
IO_Bank 10
LONG TRACES OK ROUTE AS A PAIR
T8 T1-6-KK81•
T7 MUB55
EPXA1F672I2
11/19/04
* = DNL
rev 05/3/04 rhm/ GTP
Title
Digital Optical Module FPGA sheet
Size D
Document Number main_board_vsn5.1
31Y083-S12
Vsn. 5.1
Date:
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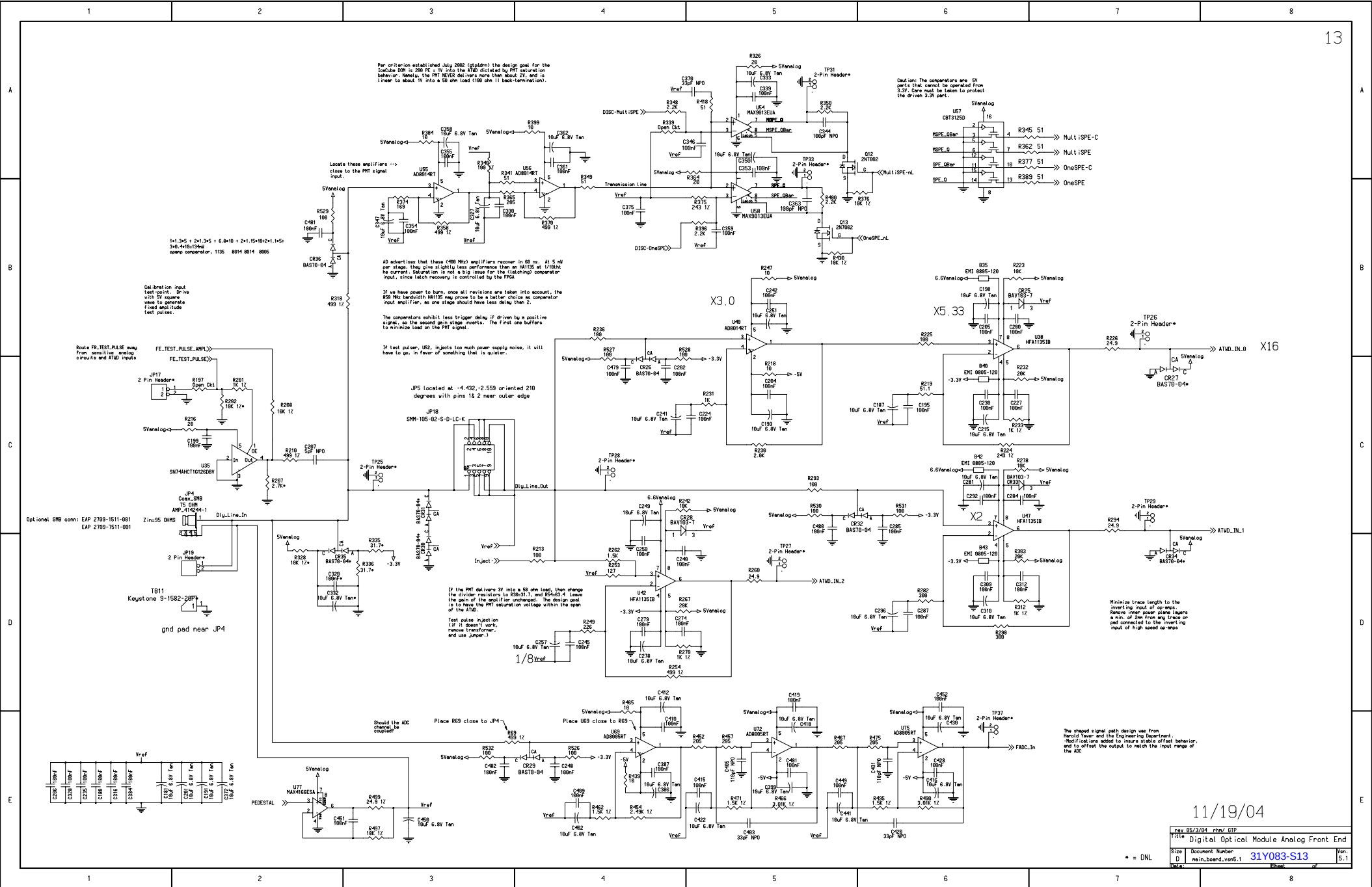
13
Per criterion established July 2002 (gtp&drm) the design goal for the IceCube DOM is 200 PE = 1V into the ATWD clipped by PMT saturation behavior. Namely, the PMT NEVER delivers more than about 2V, and is linear to about 1V into a 50 ohm load (100 ohm II back-termination).
Caution: The comparators are 5V parts that cannot be operated from 3.3V. Care must be taken to protect the driven 3.3V part.
Locate these amplifiers --> close to the PMT signal input.
1+1.3+5 + 2+1.3+5 + 6.8+10 + 2+1.15+10+2+1.1+5+ 3+0.4+10+134+W
opamp comparator, 1135 8814 8914 8905
AD advertises that these (400 MHz) amplifiers recover in 60 ns. At 5 mV per stage, they give slightly less performance than an HA1135 at 1/10th the current. Saturation is not a big issue for the (latching) comparator input, since latch recovery is controlled by the FPGA
Calibration input test-point. Drive with 5V square wave to generate fixed amplitude test pulses.
If we have power to burn, once all revisions are taken into account, the 850 MHz bandwidth HA1135 may prove to be a better choice as comparator input amplifier, as one stage should have less delay than 2.
The comparators exhibit less trigger delay if driven by a positive signal, so the second gain stage inverts. The first one buffers to minimize load on the PMT signal.
If test pulser, U52, injects too much power supply noise, it will have to go, in favor of something that is quieter.
JP5 located at -4.432,-2.559 oriented 210 degrees with pins 1& 2 near outer edge
Route FE_TEST_PULSE away from sensitive analog circuits and ATWD inputs
Optional SMB conn: EAP 2709-1511-001 EAP 2709-7511-001
gnd pad near JP4
If the PMT delivers 3V into a 50 ohm load, then change the divider resistors to R3=31.7, and R5=63.4. Leave the gain of the amplifier unchanged. The design goal is to have the PMT saturation voltage within the span of the ATWD.
Test pulse injection (if it doesn't work, remove transformer, and use jumper.)
Should the ADC channel be coupled?
Place R69 close to JP4
Place U69 close to R69
Minimize trace length to the inverting input of op-amps. Remove inner power plane layers a min. of 2mm from any trace or pad connected to the inverting input of high speed op-amps
The shaped signal path design was from Harold Tever and the Engineering Department. -Modifications added to insure stable offset behavior, and to offset the output to match the input range of the ADC
* = DNL
11/19/04
rev 05/3/04 rhm/ GTP
Title Digital Optical Module Analog Front End
Size D
Document Number 31Y083-S13
Vsn. 5.1
Date: main_board_vsn5.1
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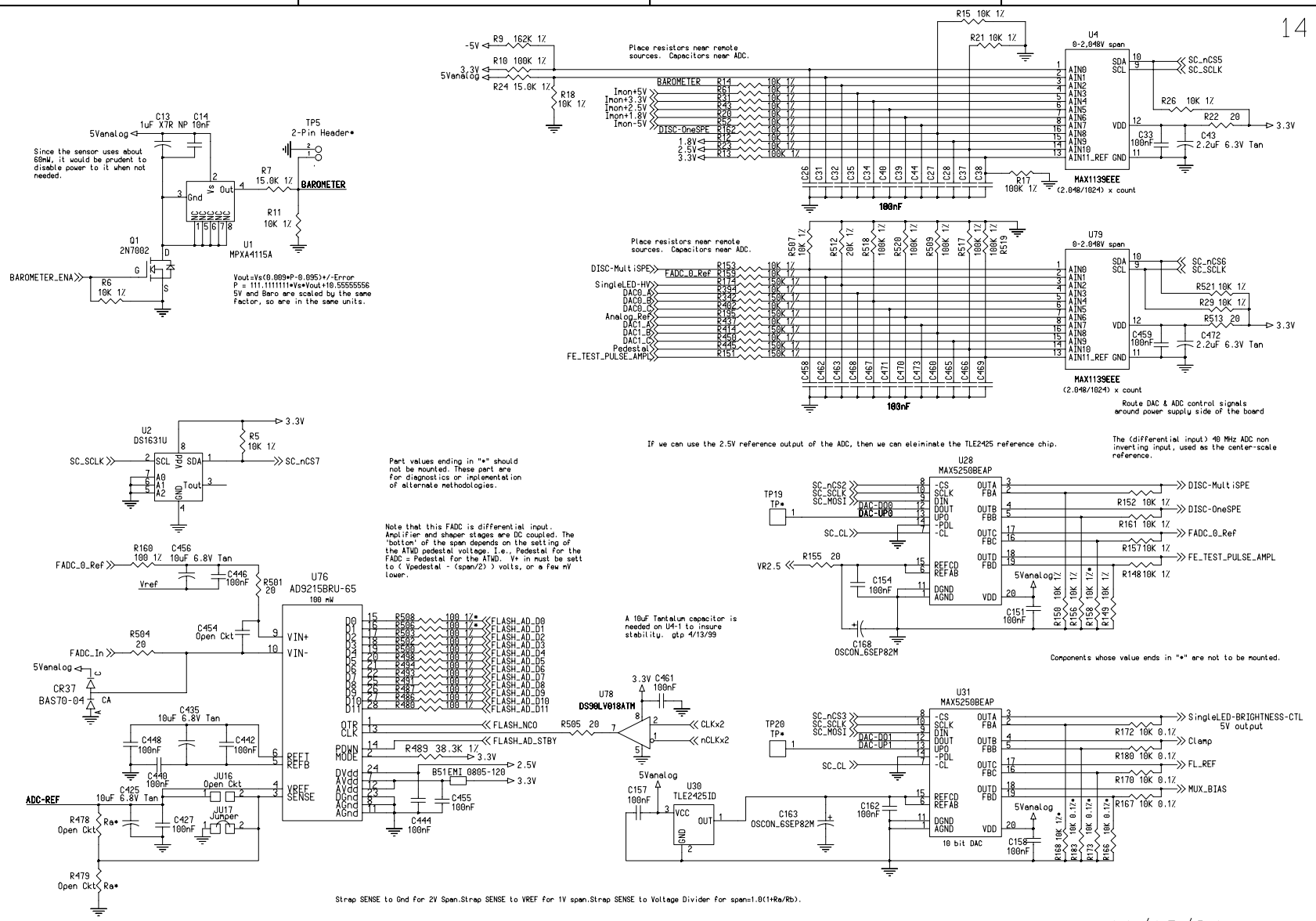
14
Since the sensor uses about 60mW, it would be prudent to disable power to it when not needed.
Vout=Vs(0.009*P-0.095)+/-Error
P = 111.1111111*Vs+Vout+10.55555556
5V and Baro are scaled by the same factor, so are in the same units.
Place resistors near remote sources. Capacitors near ADC.
MAX1139EEE
(2.048/1024) x count
Route DAC & ADC control signals around power supply side of the board
If we can use the 2.5V reference output of the ADC, then we can eleiminate the TLE2425 reference chip.
The (differential input) 40 MHz ADC non inverting input, used as the center-scale reference.
Part values ending in "*" should not be mounted. These part are for diagnostics or implementation of alternate methodologies.
Note that this FADC is differential input. Amplifier and shaper stages are DC coupled. The 'bottom' of the span depends on the setting of the ATWD pedestal voltage. I.e., Pedestal for the FADC = Pedestal for the ATWD. V+ in must be sett to (Vpedestal - (span/2)) volts, or a few mV lower.
A 10uF Tantalum capacitor is needed on U4-1 to insure stability. gtp 4/13/99
Components whose value ends in "*" are not to be mounted.
Strap SENSE to Gnd for 2V Span.Strap SENSE to VREF for 1V span.Strap SENSE to Voltage Divider for span=1.0(1+Ra/Rb).
* = DNL
11/19/04
rev 05/3/04 BCH/ GTP
Title
Digital Optical Module AD/DA
Size C
Document Number main_board_vsn5.1
31Y083-S14
Vsn. 5.1
Date:
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